SESSION 17 – TAPA II
Advanced CMOS III

Thursday, June 17, 10:25 a.m.
Chairpersons: T. Skotnicki, STMicroelectronics
Y. Akasaka, Tokyo Electron Ltd.

17.1 - 10:25 a.m.
Comprehensive Study and Control of Oxygen Vacancy Induced Effective Work Function Modulation in Gate-First High-k/Metal Inserted Poly-Si Stacks, T. Hosoi, M. Saeki, Y. Oku, H. Arimura, N. Kitano, K. Shiraishi*, K. Yamada**, T. Shimura^, H. Watanabe^, ^Osaka University, *University of Tsukuba, **Waseda University, Japan

We report the crucial impact of "Reductant Controlled MIPS (RC-MIPS) process" to obtain a high effective work function (EWF) of poly-Si/TiN/HfSiON stacks in the gate-first process. It was found that carbon impurity, the strongest reductant element in the gate stack, dominates oxygen vacancy formation kinetics and markedly enhances Fermi level pinning phenomenon. We designed a high EWF gate-first RC-MIPS technology that uses both in situ metal/high-k fabrication and reduction suppressing processes, improving EOT-Jg characteristics and EWF stability.

17.2 - 10:50 a.m.
8Å Tinv Gate-First Dual Channel Technology Achieving Low-V_t High Performance CMOS, L. Witters, S. Takeoka, S. Yamaguchi, A. Hikavyy, D. Shamiryan, M.J. Cho, T. Chiarella, L.-Å. Ragnarsson, R. Loo, C. Kerner, Y. Crabbe, J. Franco, J. Tseng, W.-E. Wang, E. Rohr, T. Schram, O. Richard, H. Bender, S. Biesemans, P. Absil, T. Hoffmann, IMEC, Belgium

We report low Vt high performance CMOS devices with ultra-scaled Tinv down to Tinv~8Å using a gate-first dual Si/SiGe channel low-complexity integration approach. Compared to a dual dielectric cap gate-first integration scheme, the devices show for the same high-k/metal gate stack (1) 3Å reduction in nMOS and pMOS Tinv (2) 220mV lower pMOS Vt (3) 21%/12% pMOS/nMOS drive current increase and (4) 50% improvement in pMOS Vt variability. For a fixed Tinv of 12Å, a 4 times higher hole mobility and 350mV increase in NBTI 10years lifetime operating voltage are obtained.

17.3 - 11:15 a.m.
Dipole Controlled Metal Gate with Hybrid Low Resistivity Cladding for Gate-Last CMOS with Low Vt, C. Hinkle, R. Galatage, R. Chapman, E. Vogel, H. Alshareef*, C. Freeman**, E. Wimmer**, H. Niimi^, A. Li-Fatou^, J. Shaw^, J. Chambers, University of Texas at Dallas, USA, King Abdullah University of Science and Technology, Saudi Arabia, ** Materials Design Inc., USA, ^ Texas Instruments, USA

NMOS and PMOS band edge effective work function and correspondingly low Vt are demonstrated using standard fab materials and processes in a gate-last scheme employing low-temperature anneals and selective cladding layers. Al migration from the cladding to the TiN/HfO2 interface during FGA together with low O concentration in the TiN enables low NMOS Vt. The use of non-migrating W cladding along with N-induced dipoles, produced by increased oxygen in the TiN, facilitates low PMOS Vt.

17.4 - 11:40 a.m.
Ion-Implantation-Based Low-Cost Hk/MG Process for CMOS Low-Power Application, C. Ortolland, S. Sahhaf, V. Srividya, R. Degraeve, K. Saino, C.-S. Kim^, M. Gilbert, T. Kauerauf, M.J.Cho, M. Dehan, T. Schram, M. Togo, N. Horiguchi, G. Groeseneken, S. Biesemans, P. Absil, W. Vandervorst, D. Gealy, T. Hoffmann, IMEC, Belgium

This paper demonstrates for the first time a low cost, low complexity process CMOS Hk/MG for low-power applications with Vth controlled by gate Ion-Implantation (I/I) and High-k capping for NMOS and PMOS,

respectively. Novel advanced electrical and physical characterizations provide unique insights about the underlying mechanism of Vth adjust induced by I/I into the metal. Improved RO performance, with excellent uniformity and matching characteristics have been achieved without reliability degradation.