SESSION 18 – TAPA III
Characterization and Modeling

Thursday, June 17, 10:25 a.m.
Chairpersons: E. Kan, Cornell University
E. Morifuji, Toshiba Corporation Semiconductor Company

18.1 - 10:25 a.m.
Direct Observation of RTN-induced SRAM Failure by Accelerated Testing and Its Application to Product Reliability Assessment, K. Takeuchi, T. Nagumo, K. Takeda, S. Asayama, S. Yokogawa, K. Imai, Y. Hayashi, NEC Electronics Corporation, Japan

A new accelerated testing scheme for detecting SRAM bit failure caused by random telegraph noise (RTN) is proposed. By repeatedly monitoring the fail bit count (FBC) under a reduced margin operation condition, increasing trend of FBC along time was clearly observed, which is believed to be caused by RTN. In addition, physics-based ultra-fast Monte Carlo RTN simulation program has been developed, which quantitatively reproduces the test results. By using the simulation calibrated by the test, product reliability against RTN can be accurately predicted.

18.2 - 10:50 a.m.
Direct Measurements, Analysis, and Post-Fabrication Improvement of Noise Margins in SRAM Cells Utilizing DMA SRAM TEG, M. Suzuki, T. Saraya, K. Shimizu, A. Nishida*, S. Kamohara*, K. Takeuchi*, S. Miyano**, T. Sakurai, T. Hiramoto, University of Tokyo, *MIRAI-Selete, **STARC, Japan

A special device-matrix-array (DMA) TEG of 16k bit SRAM cells has been designed. Static noise margins (SNM) and 6 transistors in cells are directly measured and their fluctuations are examined. It is found for the first time that one-side SNM follows the normal distribution up to ±4σ. It is also found that the cell stability is worse than circuit simulation using Vth of measured 6 transistors. Furthermore, the post-fabrication self-convergence scheme by NBTI stress is applied to DMA SRAM TEG and the cell stability improvement is demonstrated experimentally for the first time.

18.3 - 11:15 a.m.
Single Dopant Impact on Electrical Characteristics of SOI NMOSFETs with Effective Length Down to 10nm, R. Wacquez, M. Vinet, M. Pierre, B. Roche, X. Jehl, O. Cueto, J. Verduijn*, G.C. Tettamanzi*, S. Rogge*, V. Deshpande, B. Previtali, C. Vizioz, S. Pauliac-Vaujour, C. Comboroure, N. Bove, O. Faynot, M. Sanquer, CEA Grenoble, France, *TU Delft, Netherlands

For the first time, we provide an in-depth understanding of single dopant influence on NMOSFETs characteristics by linking low and room temperature transport. We demonstrate that, for gate length of 30 nm and below (channel length down to 10 nm), the presence of a single dopant dramatically alters the subthreshold behaviour when the dopant is located in the middle of the channel. Moving the dopants away from the channel leads to enhanced variability above Vt.

18.4 - 11:40 a.m.
Dopant and Carrier Profiling in FinFET-Based Devices with Sub-Nanometer Resolution, J. Mody*, A. K. Kambham*, G. Zschaetzsch*, P. Schatzer, T. Chiarella, N. Collaert, L. Witters, M. Jurczak, N. Horiguchi, M. Gilbert*, P. Eyben, S. Koelling*, A. Schulze*, T.Y. Hoffmann, W. Vandervorst, IMEC, *KU Leuven, Belgium

Atom probe tomography (APT) in conjunction with scanning spreading resistance microscopy (SSRM) is demonstrated for the first time to profile dopant and carrier distributions in FinFET-based devices with sub-nanometer resolution. These two techniques together provide information on the degree of conformality, the dose retention and the dopant activation. These results are also compared with a

methodology involving secondary ion mass spectrometry (SIMS). Ion implantation for increased conformality of source/drain extensions is demonstrated for tilted implants, which clearly leads to improved device performance.