SESSION 19 – TAPA II
PCRAM

Thursday, June 17, 1:30 p.m.
Chairpersons: K. Parekh, Micron
H. Miyake, Elpida Memory, Inc.

19.1 - 1:30 p.m.
Programming Disturbance and Cell Scaling in Phase Change Memory : For up to 16nm Based $4F^2$ Cell, S.H. Lee, M.S.Kim, G.S. Do, S.G. Kim, H.J. Lee, J.S. Sim, N.G. Park, S.B. Hong, Y.H. Jeon, K.S. Choi, H.C. Park, T.H. Kim, J.U. Lee, H.W. Kim, M.R. Choi, S.Y. Lee, Y.S. Kim, H.J. Kang, J.H. Kim, H.J. Kim, Y.S. Son**, B.H. Lee, J.H. Choi, S.C. Kim, J.H. Lee, S.J. Hong, S.W. Park, Hynix Semiconductor Inc., Korea

We focus here on the promising solutions to overcome thermal-induced erase failure of the unselected neighbor cell while a selected cell is being programmed to reset state with a high-current pulse. Our physical analysis and systematic approaches compatible with disturbance-free are addressed to achieve a highly scalable architecture, which can provide the physical and electrical criteria for phase change memory (PCM) up to 16nm technology node.

19.2 - 1:55 p.m.
MLC PRAM with SLC Write-Speed and Robust Read Scheme, Y. Hwang, C. Um, J. Lee, C. Wei, H.-R. Oh, G. Jeong, H. Jeong, C. Kim, C. Chung, Samsung Electronics Co., LTD, Korea

We have proposed an integrated method to realize MLC PRAM at 45nm technology node and beyond. It includes reset initialization, Toff skew write, and 2bit write to enhance write-and-verify speed, and 3-cell reference scheme to cope with cell variation due to resistance drift and temperature change. Based on the proposed methods, write throughput can be increased up to SLC level with robust read operation.

19.3 - 2:20 p.m.
High Performance PRAM Cell Scalable to Sub-20nm Technology with Below $4F^2$ Cell Size, Extendable to DRAM Applications, I.S. Kim, S. Cho, D.-H. Im, E.-H. Cho, D. Kim, G. Oh, D.H. Ahn, S.O. Park, S.W. Nam, J.-T. Moon, C. Chung, Samsung Electronics Co., LTD, Korea

We fabricated a confined PRAM cell with 7.5nmx17nm of below 4F2. In particular, Sb-rich Ge-Sb-Te phase change material was employed for high speed operation below 30nsec. The excellent writing endurance performance was predicted to maintain up to 6.5E15cycles by reset program energy acceleration. Its data retention was 4.5 years at 85oC. This has the meaning of the potential applicable to the technology area of scaling limitation of DRAM cell.

19.4 - 2:45 p.m.
Highly-Scalable Novel Access Device Based on Mixed Ionic Electronic Conduction (MIEC) Materials for High Density Phase Change Memory (PCM) Arrays, K. Gopalakrishnan, R. Shenoy, C. Rettner, K. Virwani, D. Bethune, R. Shelby, G. Burr, A. Kellock, R. King, K. Nguyen, A. Bowers, M. Jurich, B. Jackson, A. Friz, T. Topuria, P. Rice, B. Kurdi, IBM Almaden Research Center, USA

Phase Change Memory could potentially achieve high density with large, 3D-stacked crosspoint arrays, but not without a BEOL-friendly Access Device capable of high current densities and large ON/OFF ratios. We demonstrate that novel ADs based on Cu-ion motion in Mixed Ionic Electronic Conduction (MIEC) materials provide the ultra-high current densities needed for PCM, exhibit high ON/OFF ratios with excellent uniformity, are highly scalable, and are compatible with <400degC fabrication.