SESSION 2 – TAPA I
Advanced CMOS I

Tuesday, June 15, 10:20 a.m.
Chairpersons: O. Faynot, CEA LETI
M. Masahara, AIST

2.1 - 10:20 a.m.
Enhanced Performance in SOI FinFETs with Low Series Resistance by Aluminum Implant as a Solution Beyond 22nm Node, I. Ok, C. Young, W.-Y. Loh, T. Ngai, S. Lian, J. Oh, M. Rodgers^, S. Bennett^, H. Stamper^, D. Franca^, S. Lin*, K. Akarvardar**, C. Smith, C. Hobbs, P. Kirsch, R. Jammy, Sematech, ^CNSE, *UMC, **GLOBALFOUNDRIES, USA

We present an approach to scale Rext while maintaining control of short channel effects in scaled finFETs. For FETs with fins <20nm, an enhancement of 19% in drain current was achieved in nFETs by incorporating Al at silicide-Si interface. This Al implantation while reducing the schottky barrier height for n-Si contact, does not degrade the integrity of the junction extensions or gate stacks. These attributes constitute non-planar CMOS integration for future high performance technology nodes

2.2 - 10:45 a.m.
A 0.063 μm^2 FinFET SRAM Cell Demonstration with Conventional Lithography Using a Novel Integration Scheme with Aggressively Scaled Fin and Gate pitch, V. Basker, T. Standaert, H. Kawasaki**, C.-C. Yeh, K. Maitra*, T. Yamashita, J. Faltermeier, H. Adhikari*, H. Jagannathan, J. Wang, H. Sunamura^, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada^, C.-H. Lin, P. Kulkarni, Y. Zhu^^, J. Kuss, T. Yamamoto^, A. Kumar^^, J. Wahl*, A. Yagashita**, L.F. Edge, R.H. Kim*, E. Mclellan, S.J. Holmes, R.C. Johnson, T. Levin, J. Demarest, M. Hane^, M. Takayanagi**, M. Colburn, V.K. Paruchuri, R.J. Miller*, H. Bu, B. Doris, D. McHerron, E. Leobandung and J. O'Neill, IBM Research, *GLOBALFOUNDRIES Inc., **Toshiba America Electronic Components Inc, ^NEC Electronics, ^^IBM T.J. Watson Research Center, USA

We report the smallest FinFET SRAM cell size of 0.063 μm2 using optical lithography. The cell is fabricated with gate pitch scaled to 80 nm and fin pitch scaled to 40 nm for the first time. A novel double-expose, double-etch (DE2) sidewall image transfer (SIT) process is used to form fins with differential pitch. Epitaxy is then used to merge only the tight pitch fins. The epitaxial films also conformally dope the devices, reducing the external resistance significantly.

2.3 - 11:10 a.m.
Gate-all-around Silicon Nanowire 25-Stage CMOS Ring Oscillators with Diameter Down to 3 nm, S. Bangsaruntip, A. Majumdar, G. Cohen, S. Engelmann, Y. Zhang, M. Guillorn, L. Gignac, S. Mittal, W. Graham, E. Joseph, D. Klaus, J. Chang, E. Cartier, J. Sleight, IBM T.J. Watson Research Center, USA

We demonstrate the world's first top-down CMOS ring oscillators (ROs) fabricated with gate-all-around (GAA) silicon nanowire (NW) FETs having diameters as small as 3 nm. NW capacitance shows size dependence in good agreement with that of a cylindrical capacitor. AC characterization shows enhanced self-heating below 5 nm.

2.4 - 11:35 a.m.
High Yield Sub-0.1μm^2 6T-SRAM Cells, Featuring High-k/Metal-Gate Finfet Devices, Double Gate Patterning, a Novel Fin Etch Strategy, Full-Field EUV Lithography and Optimized Junction Design & Layout, N. Horiguchi, S. Demuynck, M. Ercken, S. Locorotondo, F. Lazzarino, E. Altamirano, C. Huffman, S. Brus, M. Demand, H. Struyf, J. De Backer, J. Hermans, C. Delvaux, T. Vandeweyer, C. Baerts, G. Mannaert, V. Truffert, J. Verluijs, W. Alaerts, H. Dekkers, P. Ong, N. Heylen, K. Kellens, H.

Volders, A. Hikavvy, C. Vrancken, M. Rakowski, S. Verhaegen, G. Vandenberghe, G. Beyer, A. Lauwers, P. Absil, T. Hoffman, K. Ronse, and S. Biesemans, IMEC, Belgium

We report high yield sub-0.1μm2 SRAM cells using high-k/metal gate finfet devices. Key features are (1) novel fin patterning strategy, (2) double gate patterning (3) new SRAM cell layout and (4) EUV lithography and robust etch/fill/CMP for contact/metal1. 0.099μm2 finfet 6T-SRAM cells show good yield. And smaller cells (0.089μm2) are functional. Further yield improvement is possible by junction optimization using extension less junction approach and further cell layout optimization.