SESSION 21 – TAPA II
Design Enablement II

Thursday, June 17, 3:25 p.m.
Chairpersons: K. Schruefer, Infineon Technologies
C. Wann, Taiwan Semiconductor Manufacturing Company, Ltd.

21.1 - 3:25 p.m.
World's First Monolithic 3D-FPGA with TFT SRAM over 90nm 9 Layer Cu CMOS, T. Naito, T. Ishida, T. Onoduka*, M. Nishigoori, T. Nakayama, Y. Ueno, Y. Ishimoto, A. Suzuki, W. Chung, R. Madurawe**, S. Wu**, S. Ikeda^, H. Oyamatsu, Toshiba Corporation, *Covalent Materials Corp., **Tier Logic Inc., ^tei Technology, Japan

World's first monolithically integrated TFT-SRAM configuration circuits over 9-layers of Cu-interconnect CMOS is successfully fabricated for 3D-FPGA. This novel technology built over the 9th layer of Cu metal features aggressively scaled a-Si TFT having 180nm gate, 20nm EOT, FUSI gate, S/D, all below 400C processing. TFT devices show excellent transistor characteristics, E-field scalable, and are stable for SRAM configuration circuits. This 3D-technology is a major breakthrough innovation to overcome the conventional CMOS shrinking limitation.

21.2 - 3:50 p.m.
New Cost-Effective Integration Schemes Enabling Analog and High-Voltage Design in Advanced CMOS SOC Technologies, K. Benaissa, G. Baldwin, S. Liu, P. Srinivasan, F. Hou, B. Obradovic, S. Yu, H. Yang, R. McMullan, V. Reddy, C. Chancellor, S. Venkataraman, H. Lu, S. Dey, C. Cirba, Texas Instruments Inc., USA

We present novel and cost-effective integration schemes with high-performance analog and high voltage components to enable SOC designs in advanced CMOS technologies. The new transistors have superior analog performance resulting in greater analog functionality. The new high-voltage transistors enable reliable 6V capability. Additional cost-free components include fully isolated CMOS; ppoly-pwell capacitors; and high-gain bipolar transistors. These schemes do not require mask adders like deep-nwell, silicide-block, or dedicated high-voltage transistor implants commonly used in the industry.

21.3 – 4:15 p.m.
Multi-Design of Architecture, Circuit/Device/Process and Package for Cost-effective Smart Mobile Devices: An Integrated Fabless Manufacturer (IFM)'s Perspective (Invited), G.C-F Yeap, Qualcomm, Inc., USA

Smart Mobile Devices as Complex System: Advanced mobile devices such as smartphones and smartbooks are complex systems [1] with the overriding objective of providing the best user-experience value by harnessing all the technology innovations (Fig.1). Most critical system drivers are better system performance/power efficiency, cost effectiveness [2], and smaller form factors, which, in turns, drive the need of system design and solution with More-than-Moore (MtM) innovations. A consistent hardware/software co-design leads to the choice of integrated approach (SoC and/or SiP) over discrete application processor (AP) approach. Smartphones with integration approach is driving affordability and winning in the market place (Fig. 2). In this paper, we highlight how the multi-design strategy influenced architecture, device/circuit and package, in the face of growing process cost.

21.4 – 4:40 p.m.
Design Challenges and Enablement for 28nm and 20nm Technology Nodes (Invited), C.Y-C Hou, Taiwan Semiconductor Manufacturing Company, Taiwan

This paper presents technology and design challenges at 28nm and 20nm technology nodes, and provides solutions as key enablement for designers to effectively overcome those challenges.

21.5 – 5:05 p.m.
High Performance Design with Advanced Features in 22nm and Beyond (Invited), S. Borkar, Intel Corporation, USA

This paper describes design challenges in utilizing advanced features, such as fully depleted transistors, compound semiconductors, embedded memory, and 3D integration, and evaluates their benefits