SESSION 22 – TAPA III
Exploratory Research

Thursday, June 17, 3:25 p.m.
Chairpersons: A. Seabaugh, Notre Dame University
S. Takagi, The University of Tokyo

22.1 - 3:25 p.m.
Study of Channel Length Scaling in Large-Scale Graphene FETs, S.-J. Han, Y. Sun, A. Bol, W. Haensch, Z. Chen, IBM T.J. Watson Research Center, USA

This work presents a detailed study of transport in field effect transistors using transferred graphene grown by chemical vapor deposition. For the first time, we observe a shift of Dirac point in graphene deviecs as a consequence of gate length scaling. This shift has been identified as one of the signatures of short channel effects in graphene. In addition, an electron-hole asymmetry observed in short channel devices suggests a strong impact from graphene/metal contacts.

22.2 - 3:50 p.m.
III-V MOSFETs with New Self-Aligned Contact, X. Zhang, H. Guo, C.-H. Ko*, C.H. Wann*, C.-C. Cheng*, H.-Y. Lin*, H.-C. Chin, X. Gong, P. Lim, G.-L. Luo**, C.-Y. Chang^, C.-H. Chien**, Z.-Y. Han^, S.-C. Huang**, Y.-C. Yeo, National University of Singapore, *TSMC, **National Nano Device Laboratory, ^National Chiao-Tung University, Taiwan

We report the first demonstration of III-V n-MOSFETs with self-aligned contact technology. The self-aligned contact was formed using a salicide-like process which is compatible with CMOS process flow.

22.3 - 4:15 p.m.
High Mobility III-V-On-Insulator MOSFETs on Si with ALD-Al_2O_3 BOX Layers, M. Yokoyama, Y. Urabe*, T. Yasuda*, H. Takagi*, H. Ishii*, N. Miyata*, H. Yamada**, N. Fukuhara**, M. Hata**, M. Sugiyama, Y. Nakano, M. Takenaka, S. Takagi, The University of Tokyo, *National Institute of Advanced Industrial Science and Technology, **Sumitomo Chemical Co. Ltd., Japan

We have successfully demonstrated III-V-semiconductor-on- insulator (III-V-OI) MOSFETs with ALD-Al2O3 buried oxide (BOX) layers under front-gate operation, for the first time. The high electron mobilities of ~3000 and ~2000 cm2/Vs were achieved for i-InGaAs and p-InGaAs channels, respectively, formed on Al2O3/Si. Also, we have found that the InGaAs-OI channel bottom condition (the InGaAs-OI/BOX interface) is quite important for the device performance through improvements by adapting ALD-Al2O3 and S passivation, resulting in high electron mobility of ~4000 cm2/Vs under back-gate operation.

22.4 - 4:40 p.m.
Efficient Metallic Carbon Nanotube Removal Readily Scalable to Wafer-Level VLSI CNFET Circuits, H. Wei, N. Patil, J. Zhang, A. Lin, H.-Y. Chen, H.-S.P. Wong, S. Mitra, Stanford University, USA

We experimentally demonstrate a new metallic carbon nanotube (CNT) removal technique that can be readily scaled to full-wafer-scale. Existing metallic CNT removal techniques either do not remove enough metallic CNTs, or are not VLSI-compatible or impose very large area costs when applied to wafer-scale VLSI (up to 200%). Our new technique retains VLSI-compatibility, achieves high Ion/Ioff of up to 10^6 and, at the same time, is readily scalable to full-wafer-level with < 1% area cost.