SESSION 3 – TAPA II
Reliability and Stability

Tuesday, June 15, 10:20 a.m.
Chairpersons: J. Cheek, Freescale
S. Chung, National Chiao Tung University

3.1 - 10:20 a.m.
Highly Accurate Product-Level Aging Monitoring in 40nm CMOS, K. Hofmann, H. Reisinger, K. Ermisch, C. Schlünder, W. Gustin, T. Pompl, G. Georgakos, K. von Arnim, J. Hatsch, T. Kodytek, T. Baumann, C. Pacha, Infineon Technologies AG, Germany

A product-level aging monitor replicating a 40nm CMOS ARM1176 critical path is presented. The monitor enables a separation of the dominating negative bias instability (NBTI) stress, including speed recovery, and the switching-activity dependent hot carrier stress (HCS). The comprehensive analysis comprises transistor and circuit level measurements as well as simulations. The monitor results demonstrate that the overall circuit performance degradation, even at high frequencies and large switching activities, is 2% for wireless-typical operating conditions.

3.2 - 10:45 a.m.
New Insight on V_T Stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology, L. Brunet*, X. Garros, M. Casse, O. Weber, F. Andrieu, C. Fenouillet-Béranger, P. Perreau, F. Martin, M. Charbonnier, D. Lafond, C. Gaumer*, S. Lhostis*, V. Vidal, L. Brévard, L. Tosti, S. Denorme*, S. Barnola, J. Damlencourt, V. Loup, G. Reimbold, F. Boulanger, O. Faynot, Alain Bravaix, CEA-Leti Minatec, *STMicroelectronics, France

In this paper it is shown that HfO2 and HfZrO oxides suffer from large VT instabilities, up to 230mV, when the device width (W) is scaled down to 80nm. It is explained by undesirable lateral oxygen diffusion through the spacers, which mainly modifies the metal workfunction in narrow transistors. HfSiO(N) oxides exhibit a much better immunity to this effect, attributed to a different crystallinity of the HK layer. Moreover, Al incorporation in the gate stack hardly changes the VT stability.

3.3 - 11:10 a.m.
Suppression of NBTI-Induced V_{MIN} Shifts Using Hafnium Doping to Gate Poly/SiON Interface and Optimized NiPt Process for 40nm Node SRAM Cell, Y.Kitamura, T. Sanuki, K. Matsuo, T. Shimizu, A. Ohta, Y. Arayashiki, H. Fukui, T. Hoshino, Y. Ueki, A. Yasumoto, H. Yoshimura, T. Asami, H. Oyamatsu, Toshiba Corporation, Japan

Hafnium introduction to poly/SiON interface has been found effective to suppress the increase of minimum operating voltage (VMIN) caused by NBTI-induced VT shift in 40nm node low power SRAM. In addition, the distribution tail of N+ node junction leakage current has been identified as enhancing VMIN failure due to NBTI, and has been improved by optimizing NiPt silicide process. Finally, operation of 32Mbit 0.24um2 low power SRAM with VMIN less than 0.9V has been demonstrated.

3.4 - 11:35 a.m.
Suppression of Anomalous Threshold Voltage Increase with Area Scaling for Mg- or La-Incorporated High-k/Metal Gate nMISFETs in Deeply Scaled Region, T. Morooka, M. Sato, T. Matsuki, T. Suzuki, K. Shiraishi*, A. Uedono*, S. Miyazaki**, K. Ohmori^, K. Yamada^, T. Nabatame^^, T. Chikyow^^, J. Yugami, K. Ikeda, Y. Ohji, Semiconductor Leading Edge Technologies, Inc, *Tsukuba University, **Hiroshima University, ^Waseda University, ^^National Institute for Material Science, Japan

This paper reveals that much amount of Mg or La capping effects for Vt reduction was disappeared with the increase of electron mobility in narrow channel nMISFETs. The key to suppress the area scaling dependency is pilling Mg/La atoms up near high-k/IFL interface. Combination of processing for high-k gate dielectrics and device structure with the high-k dielectrics under offset spacers was found to effectively suppress the Vt increase at the 100 nm channel width.