SESSION 4 – TAPA I
Advanced CMOS II

Tuesday, June 15, 1:30 p.m.
Chairpersons: M. Khare, IBM
H. Kurata, Fujitsu Microelectronics Ltd.

4.1 - 1:30 p.m.
20nm Gate Length Trigate pFETs on Strained SGOI for High Performance CMOS, L. Hutin, M. Cassé, C. Le Royer, J.-F. Damlencourt, A. Pouydebasque, C. Xu, C. Tabone, J.-M. Hartmann, V. Carron, H. Grampeix, V. Mazzocchi, R. Truche, O. Weber, P. Batude, X. Garros, L. Clavelier, M. Vinet, O. Faynot, CEA LETI Minatec, France

We demonstrate trigate <110> uniaxially compressively strained SGOI pFETs (Ge content enriched up to 25%, 35%) scaled for the first time down to Lg=20nm, W=30nm. The state-of-the-art performance, good electrostatic integrity and NBTI as well as Vth,p lowering confirm the interest of this approach for sub-22nm nodes high-performance CMOS with single-metal gate.

4.2 - 1:55 p.m.
SiGe CMOS on (110) Channel Orientation with Mobility Boosters: Surface Orientation, Channel Directions, and Uniaxial Strain, J. Oh, S.-H.Lee*, K.-S. Min, J. Huang, B.G. Min, B. Sassman, K. Jeon**, W.-Y. Loh, J. Barnett, I. Ok, C.-Y. Kang, C. Smith, D.-H. Ko^, P. Kirsch, R. Jammy, SEMATECH, *University of Texas at Austin, **University of California, Berkeley, ^Yonsei University, Seoul Korea

On (110) surface, SiGe nMOS demonstrates higher electron mobility than Si nMOS. The hole mobility of SiGe pMOS also is greater on (110) surface than on (100) surface. Both electron and hole mobility on SiGe (110) surfaces are further enhanced in <110> direction with appropriate uniaxial strain. Results obtained in this work allow the integration of high mobility SiGe CMOS on single (110)<110> to enhance overall performance without process complexity associated with hybrid channel approaches.

4.3 - 2:20 p.m.
High-Mobility $Si_{1-x}Ge_x$-Channel PFETs: Layout Dependence and Enhanced Scalability, Demonstrating 90% Performance Boost at Narrow Widths, G. Eneman, S. Yamaguchi*, C. Ortolland, S. Takeoka**, L Witters, T. Chiarella, P. Favia, A. Hikavvy, J. Mitard, M. Kobayashi^, R. Krom, H. Bender, J. Tseng^^, W.-E. Wang, W. Vandervorst, R. Loo, P. Absil, S. Biesemans, T. Hoffmann, IMEC, *Sony. **Panasonic, ^Stanford University, ^^TSMC

This paper is the first to provide a comprehensive study on the layout dependence of scaled Si1-xGex-channel pFETs. Drive current enhancement up to 90% is demonstrated for Si0.55Ge0.45-channel pFETs with LG=35nm and EOT=0.9nm when the transistor width (W) is scaled from 10µm to 110nm. This is attributed to a change in channel stress. Moreover, LG=35nm Si0.55Ge0.45 pFETs show 20% linear current enhancement for Length-Of-Diffusion (LOD) scaling below 200nm.

4.4 - 2:45 p.m.
FDSOI CMOS with Dielectrically-Isolated Back Gates and 30nm L_G High-k/Metal Gate, M. Khater, J. Cai, R. Dennard, J.-B. Yau, C. Wang, L. Shi, M. Guillorn, J. Ott, Q. Ouyang, W. Haensch, IBM Research, USA

We present a novel fully-depleted SOI CMOS technology with dielectrically-isolated polysilicon back gates, achieved by a double BOX substrate combined with dual-depth shallow trench isolation. CMOS devices down to 30nm gate length are fabricated with high-k/metal gates. A novel isolation structure with

liners is shown to achieve robust isolation between devices and back gates. Effective back gate control of CMOS VT is demonstrated, which enables dual-VT design with power gating capability.