SESSION 5 – TAPA II
MRAM and X-Point RRAM

Tuesday, June 15, 1:30 p.m.
Chairpersons: K. Parekh, Micron
B.H. Lee, Gwangju Institute of Science and Technology

5.1 - 1:30 p.m.
A Multi-Level-Cell Spin-Transfer Torque Memory with Series-Stacked Mangetotunnel Junctions, T. Ishigaki, T. Kawahara, R. Takemura, K. Ono, K. Ito, H. Matsuoka, Hideo Ohno*, Hitachi, Ltd., *Tohoku University, Japan

We first report a multi-level-cell (MLC) spin-transfer torque memory (SPRAM) with series-connected magnetotunnel junctions (MTJs). The series MTJs (with different areas) show multi-level resistances by a combination of their magnetization directions. A four-level operation by spin-transfer-torque writing was experimentally demonstrated. A scheme for the write/read operation of the MLC SPRAM was also presented.

5.2 - 1:55 p.m.
Highly Scalable STT-MRAM with MTJs of Top-pinned Structure in 1T/1MTJ Cell, Y. M. Lee, C.Yoshida, K. Tsunoda, S. Umehara, M. Aoki, T. Sugii, Fujitsu Laboratories, Ltd, Japan

We report on spin transfer torque magnetoresistance random access memory with magnetic tunnel junctions that have a top-pinned stacking structure. By adopting the top-pinned structure, we can relieve the current limitation caused by driving power asymmetry of the transistor in a 1T/1M structure without an additional current path to make a reverse connection between the transistor and the top side of the MTJs, resulting in the cell area being reduced by about half.

5.3 - 2:20 p.m.
Non-volatile Spin-Transfer Torque RAM (STT-RAM): Data, Analysis and Design Requirements for Thermal Stability, A. Driskill-Smith, S. Watts, Vl. Nikitin, D. Apalkov, D. Druist, R. Kawakami, X. Tang, X. Luo, A. Ong, E. Chen, Grandis Inc., USA

The thermal stability of STT-RAM is measured by multiple techniques and compared with theory. The read disturb rate is found to be determined by the standby thermal stability, but the error rate at target read currents is higher than expected. The implication for the design of 1 Gb STT-RAM is that 10 year room temperature data retention as well as 1000 FIT read disturb error rate requires thermal stability of greater than 75.

5.4 - 2:45 p.m.
Novel Cross-point Resistive Switching Memory with Self-formed Schottky Barrier, M. Jo, D.-J.Seong, S. Kim, J. Lee, W. Lee, J.-B. Park, S. Park, S. Jung, J. Shin, D. Lee, H. Hwang, Gwangju Institute of Science and Technology, Korea

By characterizing the resistive switching state in Al/PCMO device, we propose, for the first time, the feasibility of cross-point memory without any selection device. Self-formed Schottky barrier by redox reaction at Al/PCMO interface can be used as a selection device. Using self-formed Schottky barrier, we can build simple 4F2 cross-point memory array without additional process steps.