SESSION 6 – TAPA I
Ultra Thin Body FDSOI

Tuesday, June 15, 3:35 p.m.
Chairpersons: W. Xiong, Texas Instruments
T. Iwamatsu, Renesas Technology Corp.

6.1 - 3:25 p.m.
Low Leakage and Low Variability Ultra-Thin Body and Buried Oxide (UT2B) SOI Technology for 20nm Low Power CMOS and Beyond, F. Andrieu, O. Weber, J. Mazurier, O. Thomas, J.-P. Noel, C. Fenouillet-Beranger, J.-P. Mazellier, P. Perreau, T. Poiroux, Y. Morand*, T. Morel, S. Allegret*, V. Loup, S. Barnola, F. Martin, J.-F. Damlencourt, I. Servin, M. Cassé, X. Garros, O. Rozeau, M.-A. Jaud, G. Cibrario, J. Cluzel, A. Toffoli, F. Allain, R. Kies, D. Lafond, V. Delaye, C. Tabone, L. Tosti, L. Brévard, P. Gaud, V. Paruchuri**, K. Bourdelle^, W. Schwarzenbach^, O. Bonnin^, B.-Y. Nguyen^, B. Doris**, F. Boeuf*, T. Skotnicki*, O. Faynot, CEA-LETI Minatec, *STMicroelectronics, **IBM Research, ^SOITEC

We fabricated CMOS devices on Ultra-Thin Boby and Buried Oxide SOI wafers using a single mid-gap gate. Excellent global, local and intrinsic VT-variability performances are obtained (AVT=1.45mV.µm). This leads to 6T-SRAM cells with good characteristics down to 0.5V supply voltage and with excellent Static Noise Margin (SNM) dispersion across the wafer (σSNM<SNM/6) down to VDD=0.7V. We also demonstrate ultra-low leakage (<0.5pA/micron) on UT2B devices at LG=30nm by source/back biasing thanks to a low gate current and GIDL.

6.2 - 3:50 p.m.
Hybrid Localized SOI/Bulk Technology for Low Power System-on-Chip, J.-L. Huguenin, S. Monfray, G. Bidal, S. Denorme, P. Perreau**, S. Barnola**, M.-P. Samson, C. Arvet, K. Benotmane**, N. Loubet, Q. Liu, Y. Campidelli, F. Leverd, F. Abbate, L. Clement, C. Borowiak, A. Cros, A. Bajolet, S. Handler, D. Marin-Cudraz, T. Benoist, P. Galy, C. Fenouillet-Beranger**, O. Faynot**, G. Ghibaudo*, F. Boeuf, T. Skotnicki, STMicroelectronics, *IMEP-LAHC, **CEA-LETI Minatec

This paper highlights the successful co-integration of Localized Silicon-On-Insulator (LSOI) devices and of bulk-Si I/O devices on the same chip. LSOI devices present good logic performances and very low mismatch values down to 1.2mV/µm. In addition, we show the backbiasing impact on LSOI SRAM bit-cells for stability improvement. This work also presents the co-integration of LSOI with bulk devices as a solution for the devices that are not compatible with thin-body technology. In particular, we demonstrate for the first time competitive bulk co-integrated ElectroStatic Discharge (ESD) protections.

6.3 - 4:15 p.m.
Ultra-Thin-Body and BOX (UTBB) Fully Depleted (FD) Device Integration for 22nm Node and Beyond, Q. Liu, A. Yagishita*, N. Loubet, A. Khakifirooz**, P. Kulkarni**, T. Yamamoto^, K. Cheng**, M. Fujiwara*, J. Cai**, D. Dorman**, S. Mehta**, P. Khare, K. Yako^, Y. Zhu**, S. Mignot, S. Kanakasabapathy**, S. Monfray, F. Boeuf, C. Koburger**, H. Sunamura^, S. Ponoth**, A. Reznicek**, B. Haran**, A. Upham**, R. Johnson**, L.F. Edge**, J. Kuss**, T. Levin**, N. Berliner**, E. Leobandung**, T. Skotnicki, M. Hane^, H. Bu**, K. Ishimaru*, W. Kleemeirer, M. Takayanagi*, B. Doris**, R. Sampson, STMicroelectronics, *Toshiba, **IBM, ^NEC Electronics

We present ultra-thin-body and BOX (UTBB) devices with a gate length of 25nm, featuring high-k/metal gate and raised source/drain, and demonstrate competitive drive current, large Vt modulation by back bias and extremely low Avt. The impact of ground plane, BOX thickness and back bias on local Vt variability is explored for the first time. A simulation study of electrostatic behavior shows better device scalability of UTBB, which enables reduced gate leakage and external resistance.

6.4 - 4:40 p.m.

Scalability Study of Ultra-Thin-Body SOI-MOSFETs Using Full-band and Quantum Mechanical Based Device Simulation, H. Takeda, K. Takeuchi, Y. Hayashi, NEC Electronics Corporation, Japan

Scaling limit of ultra-thin-body SOI-MOSFETs is quantitatively evaluated using device simulation, which takes into account full-band structure, quantum mechanical effects and quasi-ballistic effects. It was found that the SOI thickness cannot be decreased less than 3nm due to severe surface roughness scattering. Further considering substrate bias optimization for both On- and Off- performance, minimum attainable channel length is clarified.

6.5 - 5:05 p.m.
Efficient Multi-V_T FDSOI Technology with UTBOX for Low Power Circuit Design, C. Fenouillet-Beranger, O. Thomas, P. Perreau, J.-P. Noel, A. Bajolet*, S. Haendler*, L. Tosti, S. Barnola, R. Beneyton*, C. Perrot*, C. de Buttet, F. Abbate*, F. Baron*, B. Pernet*, Y. Campidelli*, L. Pinzelli*, P. Gouraud*, M. Cassé, C. Borowiak*, O. Weber, F. Andrieu, K. Bourdelle**, F. Boeuf*, O. Faynot, T. Skotnicki*, CEA/LETI, *STMicroelectronics, **Soitec

For the first time, Multi-VT UTBOX-FDSOI technology for low power applications is demonstrated. We highlight the effectiveness of back biasing for short devices in order to achieve ION current improvement by 45% for LVT options at an IOFF current of 23nA/µm and a leakage reduction by 2 decades for the HVT one. We also demonstrate on ring oscillators and 0.299µm² SRAM bitcells the effectiveness (ΔVT versus Vb ~ 208mV/V) of the conventional bulk reverse and forward back biasing approaches to manage the circuit static power and the dynamic performances.