SESSION 7 – TAPA II
Process Technology

Tuesday, June 15, 3:25 p.m.
Chairpersons: C.-P. Chang, Applied Materials, Inc.
S. Hayashi, Panasonic Corporation

7.1 - 3:25 p.m.
Direct Contact of High-k/Si Gate Stack for EOT below 0.7 nm using LaCe-silicate Layer with V_{fb} Controllability, K. Kakushima, T. Koyanagi, D. Kitayama, M. Kouda, J. Song, T. Kawanago, M. Mamatrishat, K. Tachi, M.K. Bera, P. Ahmet, H. Nohira**, K. Tsutsui, A. Nishiyama, N. Sugii, K. Natori, T. Hattori, K. Yamada*, H. Iwai, Tokyo Institute of Technology, *Waseda University, ** Tokyo City University

A direct high-k/Si gate stack has been proposed for gate oxide scaling. With LaCe-silicate, an EOT of 0.64 nm with an average dielectric constant (kav) of 17.4 has been obtained and an extremely low gate leakage current (Jg) of 0.65 A/cm2. The flatband voltage (Vfb) can be controlled by the compositional ratio of La in the LaCe-silicate layer. Furthermore, incorporation of Ge atom into the silicate layer can effectively shift the Vfb to positive direction.

7.2 - 3:50 p.m.
Minimization of Threshold Voltage Variation to A_{vt}=1.3mVμm in Bulk High-k/Metal Gated Devices by Dopant-Diffusion Control Using Integrated FSP-FLA Technology, S. Kato, T. Aoyama, T. Onizawa, K. Ikeda, Y. Ohji, Semiconductor Leading Edge Technologies, Inc, Japan

We have successfully suppressed threshold voltage variations due to pattern effect problems and random dopant fluctuation (RDF) using an integrated FSP-FLA. The serious problem of the pattern effect in FLA can be solved by using a light-absorber process, together with FSP-FLA. The diffusion-less feature of FLA reduces the RDF of NMOS down to the same level as with PMOS. By applying several optimized processes, we achieved Avt as 1.3mVum for NMOS and 1.2mVum for PMOS.

7.3 - 4:15 p.m.
Laser Annealed Junctions: Pocket Profile Analysis Using an Atomistic Kinetic Monte Carlo Approach, T. Noda, C. Ortolland*, W. Vandervorst*, C. Vrancken*, E. Rosseel*, T. Clarysse*, P. Absil*, S. Biesemans*, T. Hoffmann*, Panasonic Corporation, Japan, *IMEC, Belgium

We report on the device impact related to B pocket diffusion/deactivation using an atomistic kinetic Monte Carlo (KMC) diffusion modeling. Spike-RTA scaling down to 1000°C for shallow extension induces about 10% of B pocket deactivation. KMC reveals that the dominant B-clusters in nFET channel are BI2, B3I, B3I2. Laser annealing (LA) before spike-RTA improves the pocket effectiveness. This understanding of the LA impact on B pocket clustering enables us to improve the SCE/Vth variation.

7.4 - 4:40 p.m.
New Methods for the Direct Extraction of Mobility and Series Resistance from a Single Ultra-Scaled Device, J.P. Campbell, K.P.Cheung, L.C. Yu, J.S. Suehle, K. Sheng*, A Oates**, NIST, *Rutgers University, USA, **TSMC, Taiwan

A Reliable extraction methodology for both quantities directly from a single ultra-scaled device is extremely important and urgently needed. In this work, we demonstrate (1) a wafer level geometric magnetoresistance methodology for mobility extraction which is free from the influence of series resistance and (2) an elegantly simple series resistance extraction methodology with verifiable accuracy. Both methodologies are applicable to ultra-scaled silicon nMOSFETs and require only a single device.

7.5 - 5:05 p.m.

Evidence of Correlation Between Surface Roughness and Interface States Generation in Unstrained and Strained-Si MOSFETs, Y. Zhao, M. Takenaka, S. Takagi, The University of Tokyo, Japan

We experimentally demonstrate the correlation between the surface roughness and interface states (Nit) generation in Si and s-Si. It is found that s-Si exhibits a smaller Nit generation rate. This more robust SiO2/Si interfaces in s-Si devices is attributable to the smaller interface roughness. Furthermore, it is found that Nit generation causes roughness-scattering-like mobility reduction, which is less pronounced in s-Si. This phenomenon is attributable to scattering potential due to spatially non-uniform Nit generation.