SESSION 9 – TAPA II
Variability

Wednesday, June 16, 10:25 a.m.
Chairpersons: R. Jammy, SEMATECH
S. Yamakawa, Sony Corp.

9.1 - 10:25 a.m.
Application of a Statistical Compact Model for Random Telegraph Noise to Scaled-SRAM Vmin Analysis, M. Tanizawa, S. Ohbayashi, T. Okagaki, K. Sonoda, K. Eikyu, Y. Hirano, K. Ishikawa, O. Tsuchiya, Y. Inoue, Renesas Technology Corp., Japan

A statistical compact RTN (Random Telegraph Noise) model with a fixed Vth shift and Vgs dependent trap time constant is proposed. It accurately reproduces the experimental observation of larger Vth fluctuation at higher |Vgs|. The model is also applied to analysis of SRAM Vmin fluctuation and finds out the distribution follows a log-normal statistics.

9.2 - 10:50 a.m.
Analysis and Prospect of Local Variability of Drain Current in Scaled MOSFETs by a New Decomposition Method, T. Tsunomura, A. Kumar*, T. Mizutani*, C. Lee*, A. Nishida, K. Takeuchi, S. Inaba, S. Kamohara, K. Terada**, T. Hiramoto, T. Mogami, MIRAI-Selete, *The University of Tokyo, **Hiroshima City University

Causes of drain current local variability are analyzed by decomposing into current variability components. Besides VTH and Gm components, it is newly found that effects of “current onset” variability caused by channel potential fluctuations largely contribute to the current variability and that Gm component is relatively small in the saturation region. It is shown that both VTH and current onset components decreases with reducing channel dopants, indicating that intrinsic channel is very effective to reduce current variability.

9.3 - 11:15 a.m.
Statistical Evaluation for Trap Energy Level of RTS Characteristics, A. Teramoto, T. Fujisawa, K. Abe, S. Sugawa, T. Ohmi, Tohoku University, Japan

The energy distributions of traps which cause RTS noise using the array test pattern having a large number MOSFETs are investigated. The more traps located near the conduction band. The phenomena in p-MOS are almost the same as n-MOS. However, the number of traps in p-MOS is less than that in n-MOS. The tendency of the energy distribution of the traps near the conduction band edge is different from that near the valence band edge.

9.4 - 11:40 a.m.
On the Gate-Stack Origin Threshold Voltage Variability in Scaled FinFETs and Multi-FinFETs, Y. Liu, K. Endo, S. Ouchi, T. Kamei*, J. Tsukada, H. Yamauchi, Y. Ishikawa, T. Hayashida*, K. Sakamoto, T. Matsukawa, A. Ogura*, M. Masahara, AIST, *Meiji University, Japan

The Vt variation in scaled FinFETs with Lg down to 25 nm and multi-FinFETs was comprehensively investigated. The net work function variation was successfully obtained by investigating the AVt dependence of CET. Also, It was found that the Vt of multi-FinFETs with the same gate area reduces with increas-ing the number of fins. We experimentally confirmed that the wet-processed Si-fin sidewall channels contribute to, not only, the reduction of TSi fluctuations, but also, the reduction of gate-stack origin VTV.