2010 VLSI Technology Short Course

Emerging Logic and Memory Technologies for VLSI Implementation

Monday, June 14, 2010, 8:00 a.m.

Organizers: Raj Jammy, SEMATECH
Satoshi Inaba, Toshiba Corp.

8:15 a.m.	**High Performance Device Options: High Mobility Non-Si Channels** Prashant Majhi, SEMATECH (Intel Assignee)
9:20 a.m	**Options for Low Power Technologies and SOC Implementation** Klaus von Arnim, Infineon Technologies
10:25 a.m	**Break**
10:40 a.m	**Design Enablement for New Scaling Options in HP and LP Devices** James Hayden, GLOBALFOUNDARIES
11:45 a.m	**Q&A**
11: 55 a.m	**Lunch**
1:20 p.m.	**Emerging Disruptive Scaling Options: 3D I Interconnects / Implications** Sitaram Arkalgud, SEMATECH
2:25 p.m.	**Technology Outlook for Group IV CMOS and Beyond-CMOS Semiconductor Devices** Akira Toriumi, Tokyo University
3:30 p.m.	**Break**
3:45 p.m.	**Memory Technologies: Scaling Outlook for Flash and Emerging Memories** Rich Liu, Macronix
4:50 p.m.	**Q&A**
5:00 p.m.	**Adjourn**