2011 Symposia on VLSI Technology and Circuits June 14th (Tuesday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
7:30-17:00	Registration				
8:30-10:05	Circuits Short Course (8:10-11:30)		Circuits Workshop (8:10-11:30)	**T1 "Welcome and Plenary Session"** T1-1 8:30-8:45 Welcome and Opening Remarks T1-2 8:45-9:25 University of Toyama: Computer-Assisted Biofabrication: The challenges on manufacturing 3-D biological tissues for tissue and organ engineering T1-3 9:25-10:05 AMD: Technology Impacts from the New Wave of Architectures for Media-Rich Workloads	
10:40-12:20				**T2A "FinFETs"** T2A-1 10:40-11:05 IBM: Scaling of SOI FinFETs Down to Fin Width of 4 nm for the 10nm Technology Node T2A-2 11:05-11:30 IBM: Sub-25nm FinFET with Advanced Fin Formation and Short Channel Effect Engineering T2A-3 11:30-11:55 IBM: Modeling of Width-Quantization-Induced Variations in Logic FinFETs for 22nm and Beyond T2A-4 11:55-12:20 SEMATECH: Critical Discussion on (100) and (110) Orientation Dependent Transport: nMOS Planar and FinFET	**T2B "RRAM I"** T2B-1 10:40-11:05 Stanford University: Forming-Free Nitrogen-Doped AlOx RRAM with Sub-μA Programming Current T2B-2 11:05-11:30 IMEC: Evidences of Anodic-Oxidation Reset Mechanism in TiN/NiO/Ni RRAM Cells T2B-3 11:30-11:55 Stanford University: Resistive Switching AlOx-Based Memory with CNT Electrode for Ultra-Low Switching Current and High Density Memory Application T2B-4 11:55-12:20 IMEC: Deterministic and Stochastic Component in RESET Transient of HfSiO/FUSI Gate RRAM Stack
13:40-15:45	Circuits Short Course (13:15-17:30)		Circuits Workshop (13:15-16:30)	**T3A "Advanced CMOS "** T3A-1 13:40-14:05 Samsung: Aggressively Scaled High-k Last Metal Gate Stack with Low Variability for 20nm Logic High Performance and Low Power Applications T3A-2 14:05-14:30 IMEC: Gate-Last vs . Gate-First Technology for Aggressively Scaled EOT Logic/RF CMOS T3A-3 14:30-14:55 IBM: Full Metal Gate with Borderless Contact for 14 nm and Beyond T3A-4 14:55-15:20 United Microelectronics Corporation: A 28nm Poly/SiON CMOS Technology for Low-Power SoC Applications T3A-5 15:20-15:45 Qualcomm Inc: RF and Mixed-Signal Performances of a Low Cost 28nm Low-Power CMOS Technology for Wireless System-on- Chip Applications	**T3B "RRAM II"** T3B-1 13:40-14:05 Nanyang Technological University: High Performance Unipolar AlOy/HfOx/Ni Based RRAM Compatible with Si Diodes for 3D Application T3B-2 14:05-14:30 Stanford University: Theoretical Study of the Resistance Switching Mechanism in Rutile TiO2-x for ReRAM: the Role of Oxygen Vacancies and Hydrogen Impurities T3B-3 14:30-14:55 Hynix Semiconductor Inc: Highly Reliable and Fast Nonvolatile Hybrid Switching ReRAM Memory Using Thin Al2 O3 Demonstrated at 54nm Memory Array T3B-4 14:55-15:20 Renesas: High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb T3B-5 15:20-15:45 Samsung Advanced Institute of Technology: Bi-Layered RRAM with Unlimited Endurance and Extremely Uniform Switching
16:00-18:05				**T4A "High Mobility Channel Devices "** T4A-1 16:00-16:25 The University of Tokyo: High Mobility Ge pMOSFETs with ~ 1nm Thin EOT Using Al2O3/GeOx/Ge Gate Stacks Fabricated by Plasma Post Oxidation T4A-2 16:25-16:50 The University of Tokyo: High Performance Extremely-Thin Body III-V-On-Insulator MOSFETs on a Si Substrate with Ni-InGaAs Metal S/D and MOS Interface Buffer T4A-3 16:50-17:15 The University of Tokyo: CMOS Integration of InGaAs nMOSFETs and Ge pMOSFETs with Self-Align Ni-Based Metal S/D Using Direct Wafer Bonding T4A-4 17:15-17:40 AIST: Scalable TaN Metal Source/Drain & Gate InGaAs/Ge n/pMOSFETs T4A-5 17:40-18:05 IBM: A 0.021 μm2 Trigate SRAM Cell with Aggressively Scaled Gate and Contact Pitch	**T4B "NAND Flash Memory "** T4B-1 16:00-16:25 Macronix International: A Highly Scalable Vertical Gate (VG) 3D NAND Flash with Robust Program Disturb Immunity Using a Novel PN Diode Decoding Structure T4B-2 16:25-16:50 Hynix Semiconductor Inc: A Highly Manufacturable Integration Technology of 20nm Generation 64Gb Multi-Level NAND Flash Memory T4B-3 16:50-17:15 Macronix International: A Novel Low-Voltage Hot-Carrier (LVHC) Programming Method for Scaled NAND Flash Cell T4B-4 17:15-17:40 KAIST: A Novel Junctionless All-Around-Gate SONOS Device with a Quantum Nanowire on a Bulk Substrate for 3D Stack NAND Flash Memory T4B-5 17:40-18:05 Seoul National University: Extraction of 3-D Trap Position in NAND Flash Memory Considering Channel Resistance of Pass Cells and Bit- Line Interference
20:00-22:00	Joint Rump Session			Technology Rump Session	

〔Technology Short Course: June13th (Monday) 08:05-17:15/Shunju I〕
〔2011 Silicon Nanoelectronics Workshop: June12th (Sunday) 08:30-18:30, 13th (Monday) 08:30-17:00/Suzaku III〕
〔2011 Spintronics Workshop on LSI: June13th (Monday) 19:30-22:20/Suzaku II〕

2011 Symposia on VLSI Technology and Circuits June 15th (Wednesday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
7:30-17:00	Registration				
8:30-10:10	**C1 "Welcome and Plenary Session I "**			**T5A "Process Tschnology"**	**T5B "PCRAM"**
	C1-1 8:30-8:45			T5A-1 8:30-8:55	T5B-1 8:30-8:55
	Welcome and Opening Remarks			The University of Tokyo: Phase Transformation Kinetics of HfO2 Polymorphs in Ultra-Thin Region	IBM: Endurance and Scaling Trends of Novel Access-Devices for Multi-Layer Crosspoint-Memory Based on Mixed- Ionic-Electronic-Conduction
	C1-2 8:45-9:25			T5A-2 8:55-9:20	T5B-2 8:55-9:20
	JAXA: The Hayabusa Mission - Its Seven Years Flight			National University of Singapore: Novel Tellurium Co-Implantation and Segregation for Effective Source/Drain Contact Resistance Reduction and Gate Work Function Modulation in n-FinFETs	Hitachi: Phase-Change Memory Driven by Poly-Si MOS Transistor with Low Cost and High-Programming Gigabyte-Per-Second Throughput
	C1-3 9:25-10:05			T5A-3 9:20-9:45	T5B-3 9:20-9:45
	University of California at Berkeley: The Swarm at the Edge of the Cloud - A New Perspective on Wireless			AIST: Exact Control of Junction Position and Schottky Barrier Height in Dopant-Segregated Epitaxial NiSi2 for High Performance Metal Source/Drain MOSFETs	Macronix International: A Method to Maintain Phase-Change Memory Pre-Coding Data Retention after High Temperature Solder Bonding Process in Embedded Systems
				T5A-4 9:45-10:10	T5B-4 9:45-10:10
				Toshiba: An Efficient Manufacturing Technique Based on Process Compact Model to Reduce Characteristic Variation Beyond Process Limit for 40 nm Node Mass	Stanford University: A 1.4μA Reset Current Phase Change Memory Cell with Integrated Carbon Nanotube Electrodes for Cross-Point Memory Application
10:30-12:35	**C2 "Switching DC-DC Converters"**	**C3 "Advanced Wireless Transceivers"**	**C4 "Oversampling Converters"**	**T6A "Design Enablement I"**	**T6B "Novel Devices "**
	C2-1 10:30-10:55	C3-1 10:30-10:55	C4-1 10:30-10:55	T6A-1 10:30-10:55	T6B-1 10:30-10:55
	The University of Texas at Dallas: A 50.3ns Transient-Response CR-Free SIMO Power Converter with Adaptive Current Compensation	University of California at Berkeley: A 0.38THz Fully Integrated Transceiver Utilizing Quadrature Push-Push Circuitry	Oregon State University: A 12-ENOB 6X-OSR Noise-Shaped Pipelined ADC Utilizing a 9-bit Linear Front-End	Carnegie Mellon University: Design of Embedded Memory and Logic Based On Pattern Constructs	UCLA: High Performance Graphene FETs with Self-Aligned Buried Gates Fabricated on Scalable Patterned Ni- Catalyzed Graphene
	C2-2 10:55-11:20	C3-2 10:55-11:20	C4-2 10:55-11:20	T6A-2 10:55-11:20	T6B-2 10:55-11:20
	National Chiao Tung University: A 98% Cross-Talk Self-Cancellation Single-Inductor Dual-Output DC-DC Converter Using Bidirectional Power Prediction (BPP) Control in 65nm CMOS	University of California, Berkeley: A 10Gb/s 45mW Adaptive 60GHz Baseband in 65nm CMOS	Intel Corporation: A 32nm, 1.05V, BIST enabled, 10-40MHz, 11-9 bit, 0.13mm2 digitized integrator MASH DS A/D converter	Toshiba: Circuit Techniques to Improve Disturb and Write Margin Degraded by MOSFET Variability in High-Density SRAM Cells	UCLA: Non-Volatile Graphene Channel Memory (NVGM) for Flexible Electronics and 3D Multi-Stack Ultra-High- Density Data Storages
	C2-3 11:20-11:45	C3-3 11:20-11:45	C4-3 11:20-11:45	T6A-3 11:20-11:45	T6B-3 11:20-11:45
	Korea University: A Single-Inductor 8-channel Output DC-DC Boost Converter with Time-limited One-shot Current Control and Single Shared Hysteresis Comparator	Intel Corporation: A 2.5GHz delay-based wideband OFDM outphasing modulator in 45nm-LP CMOS	Stanford University: A Continuous-Time, Jitter Insensitive Sigma Delta Modulator using a Digitally Linearized Gm-C Integrator with Embedded SC Feedback DAC	Globalfoundries: Design Enablement for Yield and Area Optimization at 20 nm and Below	Renesas: A Novel BEOL Transistor (BETr) with InGaZnO Embedded in Cu-Interconnects for On-Chip High Voltage I/Os in Standard CMOS LSIs
	C2-4 11:45-12:10	C3-4 11:45-12:10	C4-4 11:45-12:10	T6A-4 11:45-12:10	T6B-4 11:45-12:10
	Hong Kong University of Science and Technology: Fixed-Frequency Adaptive-On-Time Boost Converter with Fast Transient Response and Light Load Efficiency Enhancement by Auto-Frequency-Hopping	Qualcomm Inc: A configurable multi-band multi-mode transmitter with spur cancellation through digital baseband	IMEC: A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass Delta-Sigma ADC for RF Digitization with Integrated PLL and Polyphase Decimation Filter in 40nm CMOS	Rambus: Design Challenges of Low-Power and High-Speed Memory Interface in Advanced CMOS Technology	Osaka University: Impact of Oxidation Induced Atomic Disorder in Narrow Si Nanowires on Transistor Performance
	C2-5 12:10-12:35	C3-5 12:10-12:35	C4-5 12:10-12:35	T6A-5 12:10-12:35	T6B-5 12:10-12:35
	McGill University: A Spurious-Free Switching Buck Converter Using a Delta-Sigma Modulation Controller with a Scalable Sampling Frequency	Renesas Electronics Corporation: A 3.5mm2, Inductor-less Digital-intensive Radio SoC for 300-to-950MHz ISM-band applications supporting 1.0-to-240kbps Multi-data-rates	MediaTek Wireless: A 2.8 mW Delta-Sigma ADC with 83 dB DR and 1.92 MHz BW Using FIR Outer Feedback and TIA-Based Integrator	IBM: Design Technology Co-Optimization in Technology Definition for 22nm and Beyond	Intel: Comparison of Performance, Switching Energy and Process Variations for the TFET and MOSFET in Logic
13:55-16:00	**C5 "Circuit & System Integration"**		**C6 "High Performance DACs and Amplifiers"**	**T7 "Highlights"**	
	C5-1 13:55-14:20		C6-1 13:55-14:20	T7-1 13:55-14:20	
	University of Minnesota: Measurement, Analysis and Improvement of Supply Noise in 3D ICs		Broadcom Corporation: A 100dB DR Ground-Referenced Single-Ended Class-D Amplifier in 65nm CMOS	IBM: ETSOI CMOS for System-on-Chip Applications Featuring 22nm Gate Length, Sub-100nm Gate Pitch, and 0.08μm2 SRAM Cell	
	C5-2 14:20-14:45		C6-2 14:20-14:45	T7-2 14:20-14:45	
	Panasonic Corporation: Isolation Techniques against Substrate Noise Coupling Utilizing Through Silicon Via (TSV) for RF/Mixed-Signal SoCs		Delft University of Technology: A Ping-Pong-Pang Current-Feedback Instrumentation Amplifier with 0.04% Gain Error	Renesas: Comprehensive SRAM Design Methodology for RTN Reliability	
	C5-3 14:45-15:10		C6-3 14:45-15:10	T7-3 14:45-15:10	
	National Taiwan University: A Fully-integrated Cantilever-based DNA Detection SoC in a CMOS Bio-MEMS Process		Agilent Technologies: A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz fT BiCMOS Process	Toshiba: Unified Understanding of Vth and Id Variability in Tri-Gate Nanowire MOSFETs	
	C5-4 15:10-15:35		C6-4 15:10-15:35	T7-4 15:10-15:35	
	Panasonic Corporation: A 65nm CMOS Movable Parts Manager for Optical Disc System		STmicroelectronics: A 3GS/s, 9b, 1.2V single supply, pure binary DAC with >50dB SFDR up to 1.5GHz in 65nm CMOS	IMEC: 1mA/um-ION Strained SiGe45%-IFQW pFETs with Raised and Embedded S/D	
	C5-5 15:35-16:00		C6-5 15:35-16:00		
	Hitachi, Ltd: 20-uW Operation of an a-IGZO TFT-based RFID Chip Using Purely NMOS "Active" Load Logic Gates with Ultra-Low-Consumption Power		University of California at Berkeley: A 10b 600MS/s Multi-mode CMOS DAC for Multiple Nyquist Zone Operation		
16:10-17:50	**C7 "Embedded SRAM and Applications"**	**C8 "Multi Gigabit Wireline Communication"**	**C9 "Image Sensors"**	**T8A "3D Integration "**	**T8B "Reliability and Stability "**
	C7-1 16:10-16:35	C8-1 16:10-16:35	C9-1 16:10-16:35	T8A-1 16:10-16:35	T8B-1 16:10-16:35
	TSMC: A 40nm Fully Functional SRAM with BL Swing and WL Pulse Measurement Scheme for Eliminating a Need for Additional Sensing Tolerance Margins	IBM: An 8x10-Gb/s Source-Synchronous I/O System Based on High-Density Silicon Carrier Interconnects	Sony corporation: A Digital CDS Scheme on Fully Column-Inline TDC Architecture for An APS-C Format CMOS Image Sensor	TSMC: TSV Process Optimization for Reduced Device Impact on 28nm CMOS	Hitachi: Understanding Short-Term BTI Behavior through Comprehensive Observation of Gate-Voltage Dependence of RTN in Highly Scaled High- κ / Metal-Gate pFETs
	C7-2 16:35-17:00	C8-2 16:35-17:00	C9-2 16:35-17:00	T8A-2 16:35-17:00	T8B-2 16:35-17:00
	Kobe University: A 40-nm 0.5-V 20.1-uW/MHz 8T SRAM with Low-Energy Disturb Mitigation Scheme	Rambus Inc: A 5.6Gb/s 2.4mW/Gb/s Bidirectional Link With 8ns Power-On	Samsung Advanced Institute of Technology: A 640x480 Image Sensor with Unified Pixel Architecture for 2D/3D Imaging in 0.11um CMOS	TSMC: Yield and Reliability of 3DIC Technology for Advanced 28nm Node and Beyond	MIRAI-Selete: Suppression of VT Variability Degradation Induced by NBTI with RDF Control
	C7-3 17:00-17:25	C8-3 17:00-17:25	C9-3 17:00-17:25	T8A-3 17:00-17:25	T8B-3 17:00-17:25
	National Tsing Hua University: A Larger Stacked Layer Number Scalable TSV-based 3D-SRAM for High-Performance Universal-Memory-Capacity 3D-IC Platforms	KAIST: An 8Gb/s Forwarded-Clock I/O Receiver with up to 1GHz Constant Jitter Tracking Bandwidth Using a Weak Injection-Locked Oscillator in 0.13um CMOS	Stanford University: A Dual In-Pixel Memory CMOS Image Sensor for Computation Photography	National Chiao Tung University: Novel GAA Raised Source / Drain Sub-10-nm Poly-Si NW Channel TFTs with Self-Aligned Corked Gate Structure for 3-D IC Applications	IMEC: From Mean Values to Distributions of BTI Lifetime of Deeply Scaled FETs through Atomistic Understanding of the Degradation
	C7-4 17:25-17:50	C8-4 17:25-17:50	C9-4 17:25-17:50	T8A-4 17:25-17:50	T8B-4 17:25-17:50
	Renesas Electronics Corporation: A Chip-ID Generating Circuit for Dependable LSI using Random Address Errors on Embedded SRAM and On-Chip Memory BIST	Fujitsu Labs.: A 0.12mm2 5Gbps Reciever with a Level Shifting Equalizer and a Cumulative-Histogram-Based Adaptation Engine	The University of Texas at Austin: A CMOS Sigma-Delta Photodetector Array for Bioluminescence-Based DNA Sequencing	The University of Tokyo: Hot Spot Cooling Evaluation Using Closed-Channel Cooling System (C3S) for MPU 3DI Application	TSMC: Investigation of the Self-Heating Effect on Hot-Carrier Characteristics for Packaged High Voltage Devices
19:00-21:00				Joint Cocktail/Dinner Party	

2011 Symposia on VLSI Technology and Circuits June 16th (Thursday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
8:00-17:00	Registration				
8:30-10:10	**C10 "Plenary Session II"** C10-1 8:45-9:25 NVIDIA & Stanford University — Circuit Challenges for Future Computing Systems C10-2 9:25-10:05 Omron — Smart Devices and Services in Healthcare and Wellness			**T9A "Ultra Thin Body FDSOI"** T9A-1 8:30-8:55 CEA-LETI, MINATEC — Demonstration of Low Temperature 3D Sequential FDSOI Integration Down to 50 nm Gate Length T9A-2 8:55-9:20 STMicroelectronics — Impact of Back Bias on Ultra-Thin Body and BOX (UTBB) Devices T9A-3 9:20-9:45 UC Berkeley — Stress-Induced Performance Enhancement in Si Ultra- Thin Body FD-SOI MOSFETs: Impacts of Scaling T9A-4 9:45-10:10 CEA-LETI — Ultra-Thin Buried Nitride Integration for Multi-VT, Low- Variability and Power Management in Planar FDSOI CMOSFETs	**T9B "DRAM and CMOS Sensor "** T9B-1 8:30-8:55 IMEC — Towards 1X DRAM: Improved Leakage 0.4 nm EOT STO- Based MIMcap and Explanation of Leakage Reduction Mechanism Showing Further Potential T9B-2 8:55-9:20 Renesas — Ultra-Low Leakage Junction Engineering of Cell Transistor by Raised Source/Drain for Logic-Compatible 28-nm Embedded DRAM T9B3 9:20-9:45 Hynix Semiconductor Inc — Offset Buried Metal Gate Vertical Floating Body Memory Technology with Excellent Retention Time for DRAM Application T9B-4 9:45-10:10 Semiconductor Energy Laboratory — Electronic Global Shutter CMOS Image Sensor Using Oxide Semiconductor FET with Extremely Low Off-State Current
10:30-12:35	**C11 "Fractional-N PLLs"** C11-1 10:30-10:55 Marvell Semiconductor, Inc. — A low spur fractional-N digital PLL for 802.11 a/b/g/n/ac with 0.19 ps rms jitter C11-2 10:55-11:20 Toshiba Corporation — A -104dBc/Hz In-Band Phase Noise 3GHz All Digital PLL with Phase Interpolation Based Hierarchical Time to Digital Convertor C11-3 11:20-11:45 National Taiwan University — A 3.6GHz 1MHz-Bandwidth delta-sigma Fractional-N PLL with a Quantization-Noise Shifting Architecture in 0.18um CMOS C11-4 11:45-12:10 POSTECH — A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping Delta-Sigma TDC		**C12 "Pipelined ADCs"** C12-1 10:30-10:55 Broadcom Corp — A 12b 3GS/s Pipeline ADC with 500mW and 0.4 mm2 in 40nm Digital CMOS C12-2 10:55-11:20 Panasonic Corporation — An 11b 300MS/s 0.24pJ/Conversion-Step Double-Sampling Pipelined ADC with On-chip Full Digital Calibration for all nonidealities including Memory Effects C12-3 11:20-11:45 NEC Corporation — A 22-mW 7b 1.3-GS/s Pipeline ADC with 1-bit/stage Folding Converter Architecture C12-4 11:45-12:10 Tokyo Institute of Technology — A 10b 320 MS/s 40 mW Open-Loop Interpolated Pipeline ADC C12-5 12:10-12:35 National Chiao-Tung University — A 16-mW 8-Bit 1-GS/s Subranging ADC in 55nm CMOS	**T10A "3D Integration (Focus Session)"** T10A-1 10:30-10:55 Samsung — 3D Approaches for Non-Volatile Memoriy T10A-2 10:55-11:20 STMicroelectronics — From 3D-SOC to 3D Heterogeneous Systems: Technology and Applications T10A-3 11:20-11:45 EPFL — Design Methods and Tools for 3D Integration T10A-4 11:45-12:10 Tohoku University — 3D LSI Technology and Reliability Issues T10A-5 12:10-12:35 IBM — 3D Integration from the Viewpoint of High-End Server System Design	**T10B "Characterization and Variability"** T10B-1 10:30-10:55 KAIST — Optical Charge-Pumping: A Universal Trap Characterization Technique for Nanoscale Floating Body Devices T10B-2 10:55-11:20 MIRAI-Selete — Proposal of a Model for Increased NFET Random Fluctuations T10B-3 11:20-11:45 National Chiao Tung — A Novel and Direct Experimental Observation of the Discrete Dopant Effect in Ultra-Scaled CMOS Devices T10B-4 11:45-12:10 Toshiba — Comprehensive Study of Systematic and Random Variation in Gate-Induced Drain Leakage for LSTP Applications
12:45-14:05		**Luncheon Talk**			
14:20-16:00	**C13 "High Speed Digital for Interconnects"** C13-1 14:20-14:45 NTT — The 10G-EPON OLT and ONU LSIs for the coexistence of 10G-EPON and GE-PON toward the next FTTH era C13-2 14:45-15:10 National Chiao Tung University — A 2.37Gb/s 284.8mW Rate-Compatible (491,3,6) LDPC-CC Decoder C13-3 15:10-15:35 University of California at Los Angeles — A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric C13-4 15:35-16:00 University of Michigan — SWIFT: A 2.1Tb/s 32×32 Self-Arbitrating Manycore Interconnect Fabric		**C14 "Bio Interfaces"** C14-1 14:20-14:45 IMEC — A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications C14-2 14:45-15:10 Stanford University — A 96-Channel Full Data Rate Direct Neural Interface in 0.13um CMOS C14-3 15:10-15:35 University of Michigan — BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of Texas at Austin — A Photovoltaic-Driven and Energy-Autonomous CMOS Implantable Sensor	**T11A "RTN"** T11A-1 14:20-14:45 Toshiba — Comprehensive Understanding of Random Telegraph Noise with Physics Based Simulation T11A-2 14:45-15:10 University of Tsukuba — Direct Real-Time Observation of Channel Potential Fluctuation Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals T11A-3 15:10-15:35 UC Berkeley — Impact of Random Telegraph Signaling Noise on SRAM Stability T11A-4 15:35-16:00 Samsung — A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics	**T11B "MRAM and NAND"** T11B-1 14:20-14:45 Samsung — Integration of 28nm MJT for 8~16Gb Level MRAM with Full Investigation of Thermal Stability T11B-2 14:45-15:10 LEAP — Strain-Engineering for High-Performance STT-MRAM T11B-3 15:10-15:35 Tohoku University — CoFeB/MgO Based Perpendicular Magnetic Tunnel Junctions with Stepped Structure for Symmetrizing Different Retention Times of “0” and “1” Information T11B-4 15:35-16:00 Hynix Semiconductor Inc — Highly Reliable 26nm 64Gb MLC E2NAND (Embedded-ECC & Enhanced-Efficiency) Flash Memory with MSP (Memory Signal Processing) Controller
16:15-17:55	**C15 " Clocking Building Blocks"** C15-1 16:15-16:40 POSTECH — A 0.63ps Resolution, 11b Pipeline TDC in 0.13um CMOS C15-2 16:40-17:05 University of Florida — 553-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator C15-3 17:05-17:30 Hynix Semiconductor — High-PSRR All-Digital Delay Locked Loop with Burst Update Mode and Power Noise Damping Scheme C15-4 17:30-17:55 SiTime — A Programmable MEMS-Based Clock Generator with Sub-ps Jitter Performance	**C16 "Ultra Low Power Transceivers"** C16-1 16:15-16:40 Renesas Electronics Corporation — A Battery-less WiFi-BER modulated data transmitter with ambient radio-wave energy harvesting C16-2 16:40-17:05 University of Tokyo — 315MHz Energy-Efficient Injection-Locked OOK Transmitter and 8.4uW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS C16-3 17:05-17:30 CEA LETI — A 550uW Inductorless Bandpass Quantizer in 65nm CMOS for 1.4-to-3GHz Digital RF Receivers C16-4 17:30-17:55 University of California at Berkeley — A 1mm3 2Mbps 330fJ/b Transponder for Implanted Neural Sensors	**C17 "Bio Sensors and Applications"** C17-1 16:15-16:40 Purdue university — A 0.5-V Sub-mW Wireless Magnetic Tracking Transponder for Radiation Therapy C17-2 16:40-17:05 Stanford University — A 256 Channel Magnetoresistive Biosensor Microarray for Quantitative Proteomics C17-3 17:05-17:30 University of California at Berkeley — Magnetic Relaxation Detector for Microbead Labels in Biomedical Assays C17-4 17:30-17:55 Harvard University — Low Power Control IC for Efficient High-Voltage Piezoelectric Driving in a Flying Robotic Insect	**T12 "Design Enablement II"** T12-1 16:15-16:40 Qualcomm — Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory Using Voltage Acceleration Method T12-2 16:40-17:05 IMEC — Variability and Technology Aware SRAM Product Yield Maximization T12-3 17:05-17:30 Texas Instruments — An Ultra Low-Noise MOSFET Device with Improved SNR for DCO-Type Applications T12-4 17:30-17:55 GLOBALFOUNDRIES — Bridging Design and Manufacture of Analog/Mixed-Signal Circuits in Advanced CMOS	
20:00-22:00	**Circuits Rump Session**				

2011 Symposia on VLSI Technology and Circuits June 17th (Friday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
8:00-15:00	**Circuits Registration**				
8:30-10:10	**C18 "High Performance Circuit Techniques"**	**C19 "Nonvolatile Memories"**	**C20 "High-Speed and Low Power Receiver Techniques"**		
	C18-1 8:30-8:55	C19-1 8:30-8:55	C20-1 8:30-8:55		
	Renesas Electronics Corporation — A 27% Active-Power-Reduced 40-nm CMOS Multimedia SoC with Adaptive Voltage Scaling using Distributed Universal Delay Lines	Samsung Electronics — A 21nm High Performance 64Gb MLC NAND Flash memory with 400MB/s Asynchronous Toggle DDR Interface	IBM — A 20-Gb/s, 0.66-pJ/bit Serial Receiver with 2-Stage Continuous-Time Linear Equalizer and 1-Tap Decision Feedback Equalizer in 45nm SOI CMOS		
	C18-2 8:55-9:20	C19-2 8:55-9:20	C20-2 8:55-9:20		
	University of Michigan — LC^2: Limited Contention Level Converter for Robust Wide-Range Voltage Conversion	GENUSION — A Fast Rewritable 90nm 512Mb NOR "B4-Flash" Memory with 8F2 Cell Size	National Taiwan University — A 40Gb/s Adaptive Receiver with Linear Equalizer and Merged DFE/CDR		
	C18-3 9:20-9:45	C19-3 9:20-9:45	C20-3 9:20-9:45		
	University of Michigan — Adaptive Robustness Tuning for High Performance Domino Logic	University of Tokyo — 4-Times Faster Rising VPASS (10V), 15% Lower Power VPGM (20V), Wide Output Voltage Range Voltage Generator System for 4-Times Faster 3D-integrated Solid-State Drives	IBM — A 2.6mW/Gbps 12.5Gbps RX with 8-tap Switched-Cap DFE in 32nm CMOS		
	C18-4 9:45-10:10	C19-4 9:45-10:10	C20-4 9:45-10:10		
	Hiroshima University — A 381 fs/bit, 51.7 nW/bit Nearest Hamming-Distance Search Circuit in 65 nm CMOS	IBM — A 512Mb Phase-Change Memory (PCM) in 90nm CMOS achieving 2b/cell	Columbia University — A 4.4uW Wake-Up Receiver using Ultrasound Data Communications		
10:30-12:35	**C21 "Device-based Circuit Techniques"**	**C22 "DRAM and Memory Interfaces"**	**C23 "Power Management for Energy Harvesting"**		
	C21-1 10:30-10:55	C22-1 10:30-10:55	C23-1 10:30-10:55		
	University of Michigan — A True Random Number Generator using Time-Dependent Dielectric Breakdown	IBM — 3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype	MIT — Platform Architecture for Solar, Thermal and Vibration energy combining with MPPT and single inductor		
	C21-2 10:55-11:20	C22-2 10:55-11:20	C23-2 10:55-11:20		
	Columbia University — On-chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS	Hitachi, Ltd. — In-substrate-bitline Sense Amplifier with Array-noise-gating Scheme for Low-noise 4F2 DRAM Array Operable at 10-fF Cell Capacitance	University of Texas at Dallas — A Reconfigurable SITITO Boost/Buck Regulator with Sub- Threshold Cross-Regulation-Free Dual-Mode Control for Energy- Harvesting Applications		
	C21-3 11:20-11:45	C22-3 11:20-11:45	C23-3 11:20-11:45		
	IBM — Electrical Monitoring of Gate and Active Area Mask Misalignment Error	Rambus Inc — A 12.8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications	National Chiao Tung University — A Battery-free 225 nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control		
	C21-4 11:45-12:10	C22-4 11:45-12:10	C23-4 11:45-12:10		
	National Taiwan University — A 80kS/s 36uW Resistor-based Temperature Sensor using BGR-free SAR ADC with a Unevenly-weighted Resistor String in 0.18um CMOS	Rambus Inc. — A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface	Munich University of Technology — A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications		
	C21-5 12:10-12:35		C23-5 12:10-12:35		
	IBM — PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability		HKUST — A 13.56MHz CMOS Rectifier with Switched-Offset for Reversion Current Control		
13:55-16:00	**C24 "Digital Processors"**	**C25 "Emerging ADCs"**	**C26 "Power Management Technique"**		
	C24-1 13:55-14:20	C25-1 13:55-14:20	C26-1 13:55-14:20		
	Intel Corporation — A 45nm 48-core IA processor with Variation-Aware Scheduling and Optimal Core Mapping	Keio University — A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with Tri-Level Comparator in 40 nm CMOS	IBM — Dual-Loop System of Distributed Microregulators with High DC Accuracy, Load Response Time Below 500ps, and 85mV Dropout Voltage		
	C24-2 14:20-14:45	C25-2 14:20-14:45	C26-2 14:20-14:45		
	University of California Los Angeles — A 75µW, 16-Channel Neural Spike-Sorting Processor with Unsupervised Clustering	National Tsing-Hua University — A 1-V, 8b, 40MS/s, 113uW Charge-Recycling SAR ADC with a 14uW Asynchronous Controller	NTT — MEMS-switch-based Power Management with Zero-power Voltage Monitoring for Energy Accumulation Architecture on Dust-size Wireless Sensor Nodes		
	C24-3 14:45-15:10	C25-3 14:45-15:10	C26-3 14:45-15:10		
	University of California at Los Angeles — A 7.4mW 200MS/s Wideband Spectrum Sensing Digital Baseband Processor for Cognitive Radios	Oregon State University — Digitally Synthesized Stochastic Flash ADC Using Only Standard Digital Cells	KAIST — A 210nW 29.3 ppm/degree 0.7 V Voltage Reference with a Temperature Range of -50 to 130 degree in 0.13 um CMOS		
	C24-4 15:10-15:35	C25-4 15:10-15:35	C26-4 15:10-15:35		
	Mediatek Inc. — Fully Integrated CMOS SoC for 3D Blu-ray Player Applications	Edinburgh University — A Reconfigurable 1GSps to 250MSps, 7-bit to 9-bit Highly Time-Interleaved Counter ADC in 0.13um CMOS	University of Tokyo — A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1 V Input Switched-Capacitor 1/2 Voltage Converter with Output Voltage Trimming by Hot Carrier Injection and Periodic Activation Scheme		
	C24-5 15:35-16:00	C25-5 15:35-16:00	C26-5 15:35-16:00		
	National Taiwan University — A 52mW Full HD 16-Degree Object Viewpoint Recognition SoC with Visual Vocabulary Processor for Wearable Vision Applications	Oregon State University — A 71dB SFDR Open Loop VCO-Based ADC Using 2-Level PWM Modulation	The University of Texas at Dallas — A Fast-Transient DVS-Capable Switching Converter with DeltaIL-Emulated Hysteretic Control		
16:15-17:55	**C27 "Signal Processing for Wireline"**	**C28 "Nonvolatile Memory Applications"**			
	C27-1 16:15-16:40	C28-1 16:15-16:40			
	National Taiwan University — A Laser Ranging Radar Transceiver with Modulated Evaluation Clock in 65nm CMOS Technology	Qualcomm Incorporated — A 45nm 1Mb Embedded STT-MRAM with design techniques to minimize read-disturbance			
	C27-2 16:40-17:05	C28-2 16:40-17:05			
	University of California at Los Angeles — 10Gb/s Serial I/O Receiver Based on Variable Reference ADC	Tohoku University — Fully Parallel 6T-2MTJ Nonvolatile TCAM with Single-Transistor-Based Self Match-Line Discharge Control			
	C27-3 17:05-17:30	C28-3 17:05-17:30			
	Oracle Labs — 10 Gbps, 530 fJ/b optical transceiver circuits in 40 nm CMOS	NEC Corporation — A Content Addressable Memory Using Magnetic Domain Wall Motion Cells			
	C27-4 17:30-17:55	C28-4 17:30-17:55			
	NXP Semiconductors — A direct sampling multi-channel receiver for DOCSIS 3.0 in 65nm CMOS	Carnegie Mellon University — A Non-volatile Look-Up Table Design Using PCM (Phase-Change Memory) Cells			