Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
7:30-17:00	ouzanti I	Guzdku II	Registration	Jindingu i	
				T1 "Welcome and	d Plenary Session"
				T1-1 8:30-8:45	
					and Opening Remarks
				T1-2 8:45-9:25	
8:30-10:05				University Computer-Assisted Biofabrication: The chal of Toyama tissue and organ engineering	lenges on manufacturing 3-D biological tissues for
				T1-3 9:25-10:05	
					Vave of Architectures for Media-Rich Workloads
			<b>.</b>	T2A "FinFETs"	T2B "RRAM I"
	Circuits Short Course		Circuits Workshop	T2A-1 10:40-11:05	T2B-1 10:40-11:05
	(8:10-11:30)		(8:10-11:30)	IBM Scaling of SOI FinFETs Down to Fin Width of 4 nm for the 10nm Technology Node	Stanford Forming-Free Nitrogen-Doped AlOx RRAM with University Sub-µA Programming Current
				T2A-2 11:05-11:30	T2B-2 11:05-11:30
				IBM Sub-25nm FinFET with Advanced Fin Formation	IMEC Evidences of Anodic-Oxidation Reset
10:40-12:20				and Short Channel Effect Engineering	Mechanism in TiN/NiO/Ni RRAM Cells
				T2A-3 11:30-11:55	T2B-3 11:30-11:55
				IBM Modeling of Width-Quantization-Induced Variations in Logic FinFETs for 22nm and Beyond	Stanford Resistive Switching AlOx-Based Memory with CNT University Electrode for Ultra-Low Switching Current and High Density Memory Application
				T2A-4 11:55-12:20	T2B-4 11:55-12:20
				SEMATEC Critical Discussion on (100) and (110)	IMEC Deterministic and Stochastic Component in
				H Orientation Dependent Transport: nMOS Planar and FinFET	RESET Transient of HfSiO/FUSI Gate RRAM Stack
				T3A "Advanced CMOS "	T3B "RRAM II"
				T3A-1 13:40-14:05	T3B-1 13:40-14:05
1				Samsung Aggressively Scaled High-k Last Metal Gate Stack	Nanyang High Performance Unipolar AlOy/HfOx/Ni Based
				with Low Variability for 20nm Logic High Performance and Low Power Applications	Technologica RRAM Compatible with Si Diodes for 3D Application I University
				T3A-2 14:05-14:30	T3B-2 14:05-14:30 Stanford Theoretical Study of the Resistance Switching
				IMEC Gate-Last vs . Gate-First Technology for Aggressively Scaled EOT Logic/RF CMOS	Stanford Theoretical Study of the Resistance Switching University Mechanism in Rutile TiO2-x for ReRAM: the Role of Oxygen Vacancies and Hydrogen Impurities
2.40.45.45				T3A-3 14:30-14:55	T3B-3 14:30-14:55
3:40-15:45				IBM Full Metal Gate with Borderless Contact for 14 nm and Beyond	Hynix Highly Reliable and Fast Nonvolatile Hybrid Semicondu Switching ReRAM Memory Using Thin Al2 O3 Ctor Inc Demonstrated at 54nm Memory Array
				T3A-4 14:55-15:20	T3B-4 14:55-15:20
				United A 28nm Poly/SiON CMOS Technology for Low- Microelectronics Corporation Power SoC Applications	Renesas High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb
I				T3A-5 15:20-15:45	T3B-5 15:20-15:45
				Qualcomm RF and Mixed-Signal Performances of a Low Cost	Samsung Bi-Layered RRAM with Unlimited Endurance and
	Circuite Short Course		Circuite Manhahan	Inc 28nm Low-Power CMOS Technology for Wireless	Advanced Institute of Extremely Uniform Switching
	Circuits Short Course		Circuits Workshop	System-on- Chip Applications	Technology
	(13:15-17:30)		(13:15-16:30)	T4A "High Mobility Channel Devices "	T4B "NAND Flash Memory "
				T4A-1 16:00-16:25 The High Mobility Ge pMOSFETs with ~ 1nm Thin EOT	T4B-1         16:00-16:25           Macronix         A Highly Scalable Vertical Gate (VG) 3D NAND
				University Using Al2O3/GeOx/Ge Gate Stacks Fabricated by	Internation Flash with Robust Program Disturb Immunity
				of Tokyo Plasma Post Oxidation	al Using a Novel PN Diode Decoding Structure
1				T4A-2 16:25-16:50	T4B-2 16:25-16:50
				The High Performance Extremely-Thin Body III-V-On- University Insulator MOSFETs on a Si Substrate with Ni-	Hynix A Highly Manufacturable Integration Technology Semicondu of 20nm Generation 64Gb Multi-Level NAND
l				of Tokyo InGaAs Metal S/D and MOS Interface Buffer	ctor Inc Flash Memory
				T4A-3 16:50-17:15	T4B-3 16:50-17:15
6:00-18:05				The CMOS Integration of InGaAs nMOSFETs and Ge	Macronix A Novel Low-Voltage Hot-Carrier (LVHC)
				University pMOSFETs with Self-Align Ni-Based Metal S/D of Tokyo Using Direct Wafer Bonding	Internation Programming Method for Scaled NAND Flash
				T4A-4 17:15-17:40	T4B-4 17:15-17:40
				AIST Scalable TaN Metal Source/Drain & Gate	KAIST A Novel Junctionless All-Around-Gate SONOS
				InGaAs/Ge n/pMOSFETs	Device with a Quantum Nanowire on a Bulk Substrate for 3D Stack NAND Flash Memory
I				T4A-5 17:40-18:05	T4B-5 17:40-18:05
1				IBM A 0.021 µm2 Trigate SRAM Cell with	Seoul Extraction of 3-D Trap Position in NAND Flash
l				Aggressively Scaled Gate and Contact Pitch	National Memory Considering Channel Resistance of University Pass Cells and Bit- Line Interference
0:00-22:00	Joint Rum	<b>A</b>		Technology	

[Technology Short Course: June13th (Monday) 08:05-17:15/Shunju I ] [2011 Silicon Nanoelectronics Workshop: June12th (Sunday) 08:30-18:30, 13th (Monday) 08:30-17:00/Suzaku III ] [2011 Spintronics Workshop on LSI: June13th (Monday) 19:30-22:20/Suzaku II ]

<b>T</b>		Suzeliu I	2011 Symposia on VLSI Te			th (Wednesday)	Chumin II
Time		Suzaku I	Suzaku II	Suzaku III		Shunju I	Shunju II
7:30-17:00		C1 "Welcome and	Plenary Session I "	Registration	Г	T5A "Process Tschnology"	T5B "PCRAM"
	C1-1	8:30-8:45	Flendry Session i		T5A-1	8:30-8:55	T5B-1 8:30-8:55
					The	Phase Transformation Kinetics of HfO2	IBM Endurance and Scaling Trends of Novel Access
		Welcome a	nd Opening Remarks		University o Tokyo	<sup>f</sup> Polymorphs in Ultra-Thin Region	Devices for Multi-Layer Crosspoint-Memory
	C1-2	8:45-9:25			T5A-2	8:55-9:20	Based on Mixed- Ionic-Electronic-Conduction T5B-2 8:55-9:20
	51-2	0.40-0.20			National	Novel Tellurium Co-Implantation and Segregation for	Hitachi Phase-Change Memory Driven by Poly-Si MOS
	JAXA	The Hayabusa Mis	sion - Its Seven Years Flight			f Effective Source/Drain Contact Resistance Reduction	Transistor with Low Cost and High-Programming
8:30-10:10	24.0	0.05 10.05		4	Singapore	and Gate Work Function Modulation in n-FinFETs	Gigabyte-Per-Second Throughput
	C1-3 Jniversity of	9:25-10:05			T5A-3 AIST	9:20-9:45 Exact Control of Junction Position and Schottky	T5B-3 9:20-9:45 Macronix A Method to Maintain Phase-Change Memory Pre-
	California at	The Swarm at the Edge of the	Cloud - A New Perspective on Wireless			Barrier Height in Dopant-Segregated Epitaxial NiSi2	International Coding Data Retention after High Temperature
	Berkeley				TEA 4	for High Performance Metal Source/Drain MOSFETs	Solder Bonding Process in Embedded Systems
					T5A-4 Toshiba	9:45-10:10 An Efficient Manufacturing Technique Based on	T5B-4         9:45-10:10           Stanford         A 1.4μA Reset Current Phase Change Memory Cell
						Process Compact Model to Reduce Characteristic	University with Integrated Carbon Nanotube Electrodes for
						Variation Beyond Process Limit for 40 nm Node Mass	Cross-Point Memory Application
		2 "Switching DC-DC Converters"	C3 "Advanced Wireless Transceivers"	C4 "Oversampling Converters"	T0.4 4	T6A "Design Enablement I"	T6B "Novel Devices "
	C2-1 The University	10:30-10:55 A 50.3ns Transient-Response CR-Free SIMO	C3-1 10:30-10:55	C4-1 10:30-10:55	T6A-1 Carnegie	10:30-10:55	T6B-1 10:30-10:55 High Performance Graphene FETs with Self-
	f Texas at	Power Converter with Adaptive Current	University of A 0.38THz Fully Integrated Transceiver Utilizing California at Readelace Quadrature Push-Push Circuitry	Oregon State A 12-ENOB 6X-OSR Noise-Shaped Pipelined University ADC Utilizing a 9-bit Linear Front-End	Mellon	Design of Embedded Memory and Logic Based On Pattern Constructs	UCLA Aligned Buried Gates Fabricated on Scalable
	)allas	Compensation	bei keley -	-	University		Patterned Ni- Catalyzed Graphene
	C2-2 National	10:55-11:20 A 98% Cross-Talk Self-Cancellation Single-Inductor	C3-2 10:55-11:20	C4-2 10:55-11:20 A 32nm, 1.05V, BIST enabled, 10-40MHz, 11-9	T6A-2	10:55-11:20 Circuit Techniques to Improve Disturb and Write	T6B-2 10:55-11:20 Non-Volatile Graphene Channel Memory
	Chiao Tung	Dual-Output DC-DC Converter Using Bidirectional	California A 100b/3 401111 Adaptive 000112 Baseballd III	Intel bit 0.13mm2 digitized integrator MASH DS A/D	Toshiba	Margin Degraded by MOSFET Variability in High-	
		Power Prediction (BPP) Control in 65nm CMOS	Berkeley	Corporation Converter		Density SRAM Cells	Stack Ultra-High- Density Data Storages
0:30-12:35	C2-3	11:20-11:45 A Single Inductor & channel Output DC DC Reast	C3-3 11:20-11:45	C4-3 11:20-11:45 A Continuous-Time, Jitter Insensitive Sigma Delta	T6A-3	11:20-11:45	T6B-3 11:20-11:45 A Novel BEOL Transistor (BETr) with InGaZnO
	Korea Jniversitv	A Single-Inductor 8-channel Output DC-DC Boost Converter with Time-limited One-shot Current Control	Intel A 2.5GHz delay-based wideband OFDM	Stanford Modulator using a Digitally Linearized Gm-C	Globalfound	dri Design Enablement for Yield and Area	Renesas Embedded in Cu-Interconnects for On-Chip Hig
	University	and Single Shared Hysteresis Comparator	Corporation outphasing modulator in 45nm-LP CMOS	University Integrator with Embedded SC Feedback DAC	es	Optimization at 20 nm and Below	Voltage I/Os in Standard CMOS LSIs
	<u>C2-4</u>	11:45-12:10 Fixed-Frequency Adaptive-On-Time Boost Converter	C3-4 11:45-12:10	C4-4 11:45-12:10 A 48-dB DR 80-MHz BW 8.88-GS/s Bandpass Delta-	T6A-4	11:45-12:10 Design Challenges of Low-Power and High-	T6B-4 11:45-12:10
	long Kong Iniversity of	with Fast Transient Response and Light Load	Qualcomm A configurable multi-band multi-mode transmitter	IMEC Sigma ADC for RF Digitization with Integrated PLL	Rambus	Speed Memory Interface in Advanced CMOS	Osaka Impact of Oxidation Induced Atomic Disorder in
	cience and echnology	Efficiency Enhancement by Auto-Frequency-Hopping	Inc with spur cancellation through digital baseband	and Polyphase Decimation Filter in 40nm CMOS		Technology	University Narrow Si Nanowires on Transistor Performance
	C2-5	12:10-12:35	C3-5 12:10-12:35	C4-5 12:10-12:35	T6A-5	12:10-12:35	T6B-5 12:10-12:35
	AcGill	A Spurious-Free Switching Buck Converter Using a Delta-Sigma Modulation Controller with	Renesas A 3.5mm2, Inductor-less Digital-intensive Radio SoC Electronics for 300-to-950MHz ISM-band applications supporting	A 2.8 mW Delta-Sigma ADC with 83 dB DR and 1.92 MHz BW Using FIR Outer Feedback and	IBM	Design Technology Co-Optimization in	Intel Comparison of Performance, Switching Energy and Process Variations for the TFET and
	Jniversity	a Scalable Sampling Frequency	Corporation 1.0-to-240kbps Multi-data-rates	Wireless TIA-Based Integrator		Technology Definition for 22nm and Beyond	MOSFET in Logic
		5 "Circuit & System Integration"		C6 "High Performance DACs and Amplifiers"		T7 "Hig	Jhlights"
		13:55-14:20		C6-1 13:55-14:20	T7-1	13:55-14:20	
		Measurement, Analysis and Improvement of		Broadcom A 100dB DR Ground-Referenced Single-Ended	IBM		eaturing 22nm Gate Length, Sub-100nm Gate Pitch, and
		Supply Noise in 3D ICs		Corporation Class-D Amplifier in 65nm CMOS		0.08µm2 SRAM Cell	
	05-2	14:20-14:45 Isolation Techniques against Substrate Noise		C6-2 14:20-14:45	T7-2	14:20-14:45	
	Panasonic	Coupling Utilizing Through Silicon Via (TSV) for		University of Learning-Pong-Pang Current-Feedback	Renesas	Comprehensive SRAM D	esign Methodology for RTN Reliability
	Corporation	RF/Mixed-Signal SoCs		Technology Instrumentation Amplifier with 0.04% Gain Error		-	
3:55-16:00	C5-3	14:45-15:10		C6-3 14:45-15:10	T7-3	14:45-15:10	
5.55-10.00	National Faiwan	A Fully-integrated Cantilever-based DNA		Agilent A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a	Toshiba	Unified Understanding of Vth and	Id Variability in Tri-Gate Nanowire MOSFETs
	Jniversity	Detection SoC in a CMOS Bio-MEMS Process		Technologies 165-GHz fT BiCMOS Process			
	C5-4	15:10-15:35		C6-4 15:10-15:35	T7-4	15:10-15:35	
		A 65nm CMOS Movable Parts Manager for		A 3GS/s, 9b, 1.2V single supply, pure binary STmicroelect DAC with >50dB SFDR up to 1.5GHz in 65nm	IMEC	1mA/um-ION Strained SiGe45%-	IFQW pFETs with Raised and Embedded S/D
	orporation	Optical Disc System		CMOS			
	C5-5	15:35-16:00		C6-5 15:35-16:00			
	litachi I td	20-uW Operation of an a-IGZO TFT-based RFID Chip Using Purely NMOS "Active" Load Logic Gates with		University of A 10b 600MS/s Multi-mode CMOS DAC for California at			
		Ultra-Low-Consumption Power		California at Berkeley Multiple Nyquist Zone Operation			
	C7 "	Embedded SRAM and Applications"	C8 "Multi Gigabit Wireline Communication"	C9 "Image Sensors"		T8A "3D Integration "	T8B "Reliability and Stability "
	C7-1	16:10-16:35	C8-1 16:10-16:35	C9-1 16:10-16:35	T8A-1	16:10-16:35	T8B-1 16:10-16:35
	SMC	A 40nm Fully Functional SRAM with BL Swing and WL Pulse Measurement Scheme for Eliminating a	An 8x10-Gb/s Source-Synchronous I/O System IBM Based on High-Density Silicon Carrier	A Digital CDS Scheme on Fully Column-Inline TDC Architecture for An APS-C Format CMOS	TSMC	TSV Process Optimization for Reduced Device	Understanding Short-Term BTI Behavior through Hitachi Comprehensive Observation of Gate-Voltage Dependence
		Need for Additional Sensing Tolerance Margins	Interconnects	Image Sensor		Impact on 28nm CMOS	RTN in Highly Scaled High- κ / Metal-Gate pFETs
	C7-2	16:35-17:00	C8-2 16:35-17:00	C9-2 16:35-17:00	T8A-2	16:35-17:00	T8B-2 16:35-17:00
6:10-17:50	Kobe Jniversity	A 40-nm 0.5-V 20.1-uW/MHz 8T SRAM with Low- Energy Disturb Mitigation Scheme	Rambus Inc A 5.6Gb/s 2.4mW/Gb/s Bidirectional Link With 8ns Power-On	Samsung Advanced A 640x480 Image Sensor with Unified Pixel Institute of Architecture for 2D/3D Imaging in 0.11um CMOS	тѕмс	Yield and Reliability of 3DIC Technology for Advanced 28nm Node and Beyond	Suppression of VT Variability Degradation MIRAI-Selete Induced by NBTI with RDF Control
	C7-3	17:00-17:25	C8-3 17:00-17:25	C9-3 17:00-17:25	T8A-3	17:00-17:25	T8B-3 17:00-17:25
	National	A Larger Stacked Layer Number Scalable TSV-based 3D-SRAM for High-Performance Universal-Memory-	An 8Gb/s Forwarded-Clock I/O Receiver with up to KAIST 1GHz Constant Jitter Tracking Bandwidth Using a	Stanford A Dual In-Pixel Memory CMOS Image Sensor for	r National	Novel GAA Raised Source / Drain Sub-10-nm Poly-Si NW Channel TFTs with Self-Aligned	From Mean Values to Distributions of BTI IMEC Lifetime of Deeply Scaled FETs through
		Capacity 3D-IC Platforms	Weak Injection-Locked Oscillator in 0.13um CMOS	University Computation Photography	Chiao Tung University	Corked Gate Structure for 3-D IC Applications	Atomistic Understanding of the Degradation
	C7-4	17:25-17:50	C8-4 17:25-17:50	C9-4 17:25-17:50	T8A-4	17:25-17:50	T8B-4 17:25-17:50
	Renesas	A Chip-ID Generating Circuit for Dependable LSI	A 0.12mm2 5Gbps Reciever with a Level	The University A CMOS Sigma-Delta Photodetector Array for	The	Hot Spot Cooling Evaluation Using Closed-	Investigation of the Self-Heating Effect on Hot-
		using Random Address Errors on Embedded SRAM and On-Chip Memory BIST	Fujitsu Labs. Shifting Equalizer and a Cumulative-Histogram- Based Adaptation Engine	of Texas at Austin Bioluminescence-Based DNA Sequencing	University o Tokyo	f Channel Cooling System (C3S) for MPU 3DI Application	TSMC Carrier Characteristics for Packaged High Voltage Devices
19:00-21:00	,	- F	Dabba Haaptation Engine		1		il/Dinner Party

## 2011 Symposia on VLSI Technology and Circuits June 15th (Wednesday)

Time	Suzaku I	Suzaku II	Suzaku III Bogistration	Shunju I	Shunju II
8:00-17:00	C10 "Plana	ry Session II"	Registration	T9A "Ultra Thin Body FDSOI"	T9B "DRAM and CMOS Sensor "
ī	C10 Fienar C10-1 8:45-9:25			T9A-1 8:30-8:55	T9B-1 8:30-8:55
N S	VVIDIA & Stanford Circuit Challenges for	or Future Computing Systems		CEA-LETI, Demonstration of Low Temperature 3D Sequential MINATEC FDSOI Integration Down to 50 nm Gate Length	IMEC Towards 1X DRAM: Improved Leakage 0.4 nm E STO- Based MIMcap and Explanation of Leakage Reduction Mechanism Showing Further Potential
	Jniversity C10-2 9:25-10:05			T9A-2 8:55-9:20	T9B-2 8:55-9:20
8:30-10:10	Omron Smart Devices and Serv	vices in Healthcare and Wellness		STMicroel Impact of Back Bias on Ultra-Thin Body and ectronics BOX (UTBB) Devices	Renesas Ultra-Low Leakage Junction Engineering of Cell Transistor by Raised Source/Drain for Logic- Compatible 28-nm Embedded DRAM
				T9A-3         9:20-9:45           UC         Stress-Induced Performance Enhancement in Si           Berkeley         Ultra-Thin Body FD-SOI MOSFETs: Impacts of Scaling	T9B3         9:20-9:45           Hynix         Offset Buried Metal Gate Vertical Floating Body           Semicondu         Memory Technology with Excellent Retention Tim           ctor Inc         for DRAM Application
				T9A-4 9:45-10:10 CEA-LETI Ultra-Thin Buried Nitride Integration for Multi-VT, Low-Variability and Power Management in Planar FDSOI CMOSFETs	T9B-4         9:45-10:10           Semiconduc         Electronic Global Shutter CMOS Image Sensor tor Energy Laboratory         Using Oxide Semiconductor FET with Extremely Off-State Current
	C11 "Fractional-N PLLs"		C12 "Pipelined ADCs"	T10A "3D Integration (Focus Session)"	T10B "Characterization and Variability"
(	C11-1 10:30-10:55		C12-1 10:30-10:55	T10A-1 10:30-10:55	T10B-1 10:30-10:55
S	Marvell A low spur fractional-N digital PLL for 802.11 Semiconduc or, Inc. Aloy spur fractional-N digital PLL for 802.11		Broadcom A 12b 3GS/s Pipeline ADC with 500mW and Corp 0.4 mm2 in 40nm Digital CMOS	Samsung 3D Approaches for Non-Volatile Memoriy	KAIST Optical Charge-Pumping: A Universal Trap Characterization Technique for Nanoscale Floatin Body Devices
C	C11-2 10:55-11:20		C12-2 10:55-11:20	T10A-2 10:55-11:20	T10B-2 10:55-11:20
	A -104dBc/Hz In-Band Phase Noise 3GHz All Digital Corporation PLL with Phase Interpolation Based Hierarchical Time to Digital Convertor		Panasonic Corporation An 11b 300MS/s 0.24pJ/Conversion-Step Double- Sampling Pipelined ADC with On-chip Full Digital Calibration for all nonidealities including Memory Effects	STMicroele From 3D-SOC to 3D Heterogeneous Systems: ctronics Technology and Applications	MIRAI- Proposal of a Model for Increased NFET Selete Random Fluctuations
10.00 10.05	C11-3 11:20-11:45		C12-3 11:20-11:45	T10A-3 11:20-11:45	T10B-3 11:20-11:45
т	National         A 3.6GHz 1MHz-Bandwidth delta-sigma           raiwan         Fractional-N PLL with a Quantization-Noise           Jniversity         Shifting Architecture in 0.18um CMOS		NEC A 22-mW 7b 1.3-GS/s Pipeline ADC with 1- Corporation bit/stage Folding Converter Architecture	EPFL Design Methods and Tools for 3D Integration	National         A Novel and Direct Experimental Observation of the Chiao           Discrete Dopant Effect in Ultra-Scaled CMOS           Tung         Devices
(	C11-4 11:45-12:10		C12-4 11:45-12:10	T10A-4 11:45-12:10	T10B-4 11:45-12:10
F	POSTECH A 2 GHz Fractional-N Digital PLL with 1b Noise Shaping Delta-Sigma TDC		Tokyo A 10b 320 MS/s 40 mW Open-Loop Institute of Technology Interpolated Pipeline ADC	Tohoku 3D LSI Technology and Reliability Issues University	Toshiba Comprehensive Study of Systematic and Random Variation in Gate-Induced Drain Leakage for LSTI Applications
L			C12-5 12:10-12:35	T10A-5 12:10-12:35	
			National A 16-mW 8-Bit 1-GS/s Subranging ADC in Chiao-Tung 55nm CMOS	IBM 3D Integration from the Viewpoint of High-End Server System Design	
12:45-14:05		Luncheon Talk			
Ļ	C13 "High Speed Digital for Interconnects"		C14 "Bio Interfaces"	T11A "RTN"	T11B "MRAM and NAND"
	C13-1 14:20-14:45 The 10G-EPON OLT and ONU LSIs for the coexistence of 10G-EPON and GE-PON toward the next FTTH era		C14-1         14:20-14:45           IMEC         A Configurable and Low-Power Mixed Signal SoC for Portable ECG Monitoring Applications	T11A-1 14:20-14:45 Toshiba Comprehensive Understanding of Random Telegraph Noise with Physics Based Simulation	T11B-1 14:20-14:45 Samsung Integration of 28nm MJT for 8~16Gb Level MRAM with Full Investigation of Thermal Stability
C	C13-2 14:45-15:10		C14-2 14:45-15:10	T11A-2 14:45-15:10	T11B-2 14:45-15:10
N	National A 2.37Gb/s 284.8mW Rate-Compatible			University of Direct Real-Time Observation of Channel Potential Fluctuation	
	Jniversity (491,3,6) LDPC-CC Decodel		Stanford         A 96-Channel Full Data Rate Direct Neural           University         Interface in 0.13um CMOS	Tsukuba Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals	STT-MRAM
-	University (491,3,6) LDPC-CC Decoder C13-3 15:10-15:35		University Interface in 0.13um CMOS C14-3 15:10-15:35	Tsukuba Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals 15:10-15:35	STT-MRAM T11B-3 15:10-15:35
U	Jniversity (491,3,6) LDPC-CC Decodel		University Interface in 0.13um CMOS	Tsukuba Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals T11A-3 15:10-15:35	STT-MRAM
U C	Jniversity (491,3,6) EDPCCC Decoder C13-3 15:10-15:35 Jniversity of A 1.1 GOPS/mW FPGA Chip with Hierarchical Jatifornia at Justropapore Expire		University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface University of for Wireless Epidural Recording by Intra-Skin	Tsukuba         Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals           T11A-3         15:10-15:35           UC         Impact of Random Telegraph Signaling Noise on SRAM Stability           T11A-4         15:35-16:00	STT-MRAM T11B-3 15:10-15:35 Tohoku CoFeB/MgO Based Perpendicular Magnetic Tunn University Junctions with Stepped Structure for Symmetrizin Different Retention Times of "0" and "1" Informatic T11B-4 15:35-16:00
	Jniversity (1913,36) EDFC-CC Decoder C13-3 15:10-15:35 Jniversity of A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric C13-4 15:35-16:00 Jniversity of SWIFT: A 2.1Tb/s 32×32 Self-Arbitrating Manycore Interconnect Fabric		University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of A Photovoltaic-Driven and Energy- Austin Autonomous CMOS Implantable Sensor	Tsukuba         Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals           T11A-3         15:10-15:35           UC         Impact of Random Telegraph Signaling Noise on SRAM Stability           T11A-4         15:35-16:00           Samsung         A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics	STT-MRAM T11B-3 15:10-15:35 Tohoku CoFeB/MgO Based Perpendicular Magnetic Tunn University Junctions with Stepped Structure for Symmetrizin Different Retention Times of "0" and "1" Informatic
и с и и	Jniversity (491,3,6) EDFCCC Decoder C13-3 15:10-15:35 Jniversity of the second secon	C16 "Ultra Low Power Transceivers"	University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of A Photovoltaic-Driven and Energy- Texas at Autonomous CMOS Implantable Sensor C17 "Bio Sensors and Applications"	Tsukuba         Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals.           T11A-3         15:10-15:35           UC         Impact of Random Telegraph Signaling Noise on SRAM Stability           T11A-4         15:35-16:00           Samsung         A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics           T12 "Design Enablement II"	STT-MRAM           T11B-3         15:10-15:35           Tohoku         CoFeB/MgO Based Perpendicular Magnetic Tunn Junctions with Stepped Structure for Symmetrizini Different Retention Times of "0" and "1" Informatic           T11B-4         15:35-16:00           Hynix         Highly Reliable 26nm 64Gb MLC E2NAND (Embedded Semiconduc ECC & Enhanced-Efficiency) Flash Memory with MSP
и с и и	Jniversity       (491,3,6) EDFCCC Decoder         C13-3       15:10-15:35         Jniversity of       A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric         C13-4       15:35-16:00         Jniversity of       SWIFT: A 2.1Tb/s 32×32 Self-Arbitrating Manycore Interconnect Fabric         C15 **       Clocking Building Blocks**         C15-1       16:15-16:40	C16-1 16:15-16:40	University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of A Photovoltaic-Driven and Energy- Austin Autonomous CMOS Implantable Sensor	Tsukuba     Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals       T11A-3     15:10-15:35       UC     Impact of Random Telegraph Signaling Noise on SRAM Stability       T11A-4     15:35-16:00       Samsung     A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics       T12.1     16:15-16:40	STT-MRAM           T11B-3         15:10-15:35           Tohoku         CoFeB/MgO Based Perpendicular Magnetic Tunn Junctions with Stepped Structure for Symmetrizini Different Retention Times of "0" and "1" Informatic           T11B-4         15:35-16:00           Hynix         Highly Reliable 26nm 64Gb MLC E2NAND (Embedded Semiconduc ECC & Enhanced-Efficiency) Flash Memory with MSP
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	University         (491,3,6) EDF-CC becoder           213-3         15:10-15:35           Iniversity of California at All formio at All formio at Diversity of         11 GOPS/mW FPGA Chip with Hierarchical interconnect Fabric           C13-4         15:35-16:00           Jniversity of Manycore Interconnect Fabric           C15         "Clocking Building Blocks"           C15-1         16:15-16:40           A         0.63ps Resolution, 11b Pipeline TDC in 0.13um CMOS           C15-2         16:40-17:05	C16-1         16:15-16:40           Renesas         A Battery-less WiFi-BER modulated data transmitter Corporation           Corporation         with ambient radio-wave energy harvesting           C16-2         16:40-17:05	University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of A Photovoltaic-Driven and Energy- Texas at Austin Autonomous CMOS Implantable Sensor C17-1 16:15-16:40 Purdue A 0.5-V Sub-mW Wireless Magnetic Tracking university Transponder for Radiation Therapy C17-2 16:40-17:05	Tsukuba         Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals           T11A-3         15:10-15:35           UC         Impact of Random Telegraph Signaling Noise on SRAM Stability           T11A-4         15:35-16:00           Samsung         A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics           T12-1         16:15-16:40           Qualcomm         Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory Using Voltage Acceleration Method           T12-2         16:40-17:05	STT-MRAM           T11B-3         15:10-15:35           Tohoku         CoFeB/MgO Based Perpendicular Magnetic Tunn Junctions with Stepped Structure for Symmetrizin Different Retention Times of "0" and "1" Informatic T11B-4           15:35-16:00         Hynix           Hynix         Highly Reliable 26nm 64Gb MLC E2NAND (Embedded Semiconduc EC & & Enhanced-Efficiency) Flash Memory with MSP
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6:15-17:55 F 6:15-17:55 C 8:15-17:55 C 8:15-17:55 C 8:15-17:55 C 8:15-17:55 C 8:15-17:55 C 15:15-17:55 C 15:15-17:15-17:55 C 15:15-17:55 C 15:	Iniversity       (491,3,6) EDPC-CC Decoder         C13-3       15:10-15:35         Iniversity of California at Allfornia at Interconnect Fabric       Number California at Interconnect Fabric         C13-4       15:35-16:00         Jniversity of Manycore Interconnect Fabric       SWIFT: A 2.1Tb/s 32×32 Self-Arbitrating Manycore Interconnect Fabric         C15-1       16:15-16:40         POSTECH       A 0.63ps Resolution, 11b Pipeline TDC in 0.13um CMOS         C15-2       16:40-17:05         Jniversity of S53-GHz Signal Generation in CMOS Using a Quadruple-Push Oscillator         C15-3       17:05-17:30         High-PSRR All-Digital Delay Locked Loop with semiconduc Burst Update Mode and Power Noise	C16-1         16:15-16:40           Renessa Electronics         A Battery-less WiFi-BER modulated data transmitter corporation           C16-2         16:40-17:05           University of Transmitter and 8.4uW Power-Gated Receiver Front-End for Wireless Ad Hoc Network in 40nm CMOS           C16-3         17:05-17:30           A 550uW Inductorless Bandpass Quantizer in CEA LETI           C50uW Inductorless Bandpass Quantizer in CEA LETI	University Interface in 0.13um CMOS C14-3 15:10-15:35 BioBolt: A Minimally-Invasive Neural Interface for Wireless Epidural Recording by Intra-Skin Communication C14-4 15:35-16:00 University of A Photovoltaic-Driven and Energy- Texas at Autonomous CMOS Implantable Sensor C17 "Bio Sensors and Applications" C17-1 16:15-16:40 Purdue A 0.5-V Sub-mW Wireless Magnetic Tracking university Transponder for Radiation Therapy C17-2 16:40-17:05 Stanford University of A256 Channel Magnetoresistive Biosensor Microarray for Quantitative Proteomics C17-3 17:05-17:30 University of Magnetic Relaxation Detector for Microbead California 4	Tsukuba         Correlated to Random Telegraph Nose of Drain Current Using Nanowire MOSFETs with Four- Probe Terminals           T11A-3         15:10-15:35           UC         Impact of Random Telegraph Signaling Noise on SRAM Stability           T11A-4         15:35-16:00           Samsung         A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics           T12-1         16:15-16:40           Qualcomm         Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory Using Voltage Acceleration Method           T12-2         16:40-17:05           IMEC         Variability and Technology Aware SRAM Product Yield Maximization           T12-3         17:05-17:30           Texas         An Utra Low-Noise MOSFET Device with	STT-MRAM           T11B-3         15:10-15:35           Tohoku         CoFeB/MgO Based Perpendicular Magnetic Tuni University           Different Retention Times of "0" and "1" Informati T11B-4         15:35-16:00           Hynix         Highly Reliable 26nm 64Gb MLC E2NAND (Embedded Semiconduc EC & Enhanced-Efficiency) Flash Memory with MSP

## 2011 Symposia on VLSI Technology and Circuits June 16th (Thursday)

2011 Symposia on VLSI Technology and Circuits June 17th (Friday	2011 Sv	mposia on	NVLSI "	Technology	and Circuits	June 17th (Friday)	)
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Time         Suzzku II         Suzzku II         Suzzku III         Suzzku IIII         Suzzku IIII <th>Shunju II</th>	Shunju II
C18         "High Performance Circuit Techniques"         C19         Nonvolatile Memories"         C20         "High-Speed and Low Power Receiver Techniques"           Etectories         A271m Atthen-Power-Reducet 40mm CMO3         Samaura         A271m High Performance P4GB MIC ANC CO         8.30.455         Receiver Techniques"           Composition         Delinitude Universal Delay Lines         Composition         Samaura         A271m High Performance P4GB MIC ANC CO         8.30.450         Samaura           C18.20         8.55.92.01         Composition         Delinitude Universal Delay Lines         Composition         Delinitation (March Samaura)         Flash Memory With A00MBR Asynchronous         Controus-Time Lines Equalization (A5m S01 CMOS)           61.30         9.20.94.5         C19.3         9.20.94.5         C20.3         9.20.94.5           61.31         9.20.94.5         C19.3         9.20.94.5         C20.4         9.20.94.5           10.weetsy of Adaptive Robustness Tuning for High         University of Adaptive Robustness Tuning for High         University of Adaptive Robustness Tuning for High         Equative Marka Control         C20.4         9.45.0010           C18.4         9.45.10.10         C19.4         9.45.10.10         C22.4         9.45.0010         Calma Kass Sequed Sectoria         Calma Kass Sequed Sectoria         Calma Kass Sequed Sectoria         Ca	
C18-1     8:30-8:55     C20-1     8:30-8:55       Research     A275 Active-Power-Reduct d0 Am CMOS       Exerctionics     Multimedia SoC with Adgive Votage Scaling using       Corporation     Distributed Withwersal Delay Lines       Corporation     C19-1     8:30-8:55       Exerctionics     Multimedia SoC with Adgive Votage Scaling using       Bismung     C19-2     8:55-9:20       C19-2     8:55-9:20       C19-3     9:20-9:45       Universal Votage Scaling for High     C19-1       Multipare     Robust Wide-Range Votage Scaling for High       Universal V Adgive RobustRess Tuning for High     C19-2       Multipare     A 38 fishth 51.7 nW/Dit Nearest Harming       Universal     A 38 fishth 51.7 nW/Dit Nearest Harming       Universal     A 30 fishth 51.7 nW/Dit Nearest Harming       Universal     C19-2       217     22 To Vice-Scale Concurrence       Universal     A 38 fishth 51.7 nW/Dit Nearest Harming       Universal     C22-1       Universal     C23-1       Universal     C22-1       Universal     C22-1       Universal     C22-1       Universal     C23-1       Universal     C39-45       Universal     C39-45       Universal     C39-45	
Reneard A2% Active Power-Reduced 40-tim CMOS       A 21mm High Performance 45G4 Synchronus       A 20-Gbyb, 05G-public Serial Receiver with 2-Stage         Resolution:       Multimedia So with Adaptive Mollage Sading using Market Synchronus       Coll 2-2       S:55-92.0         Resolution:       10:20       2:55-92.0       Coll 2-2       S:55-92.0         Resolution:       Coll 2-2       S:55-92.0       Coll 2-2       S:55-92.0         Resolution:       Coll 2-2       S:55-92.0       Coll 2-2       S:55-92.0         Resolution:       Coll 2-3       S:55-92.0       A Fast Rewittable 90mm 512M NOR TeA- Flash* Memory with 8F2 Cell Size       Adaptive Receiver with Linear Taken Linear Taken Linear Taken Linear Taken Linear Taken Linear Taken Linear Taken 	
Electronics       Multimedia Soc with Adaptive Voltage Scalaria using Sentences       Filash memory with 400MB/s Asynchronous       Edit Multimedia Soc with Adaptive Voltage Scalaria using Sentences         6:30-01:00       Multimedia Soc with Adaptive Voltage Scalaria using Sentences       C19-2       8:55-92.0       C20-2       8:55-92.0       C20-2       8:55-92.0         8:30-01:00       Multimedia Soc with Adaptive Voltage Conversion       A Fast Rewritable 90m S12Mb NOR 78-4       Halfmont Tawan       A 40Gb/s Adaptive Roceiver with Linear Tawan         8:30-01:00       C19-3       9:20-9.45       C20-3       9:20-9.45       C20-3       9:20-9.45         C18-3       9:20-9.45       C19-3       9:20-9.45       C20-3       9:20-9.45       C20-3       9:20-9.45         C18-4       9:45-10.10       C19-4       9:45-10.10       C20-4       9:45-10.10       C20-4       9:45-10.10         Witheread District Techniques*       C22 'DRAM and Memory Interfaces*       C23-1       0:30-10.55       C22-1       10:30-10.55         C21-1       0:30-10.55       C22-1       10:35-11.20       C21-1       0:30-10.55       C22-1       10:35-11.20       Number Generator wing         Interversity of Adaptive Readown Number Generator wing       Image Mathematic M	
Corporation         Distributed Universal Delay Lines         Colde DDR Interface         Decision Feedback Equalizer in 45mm SOL CMOS           618-2         8:55-9:20         C19-2         8:55-9:20         C20-2         8:55-9:20           1:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0:0	
B:30-10:10       University Michigan       LC*2: Limited Contention Level Converter for Michigan       A Fast Rewritable 90nm 512Mb NOR "B4- Plash" Memory with 822 Cell Size       A 40Gb/s Adaptive Receiver with Linear Equilator and Merged DFE/CDR         B:30-10:10       C19-3       9:20-9:45       C20-3:45       C20-3:45       C20-3:45         C19-3       9:20-9:45       C20-3:45       C20-3:45       C20-3:45       A 2.6mW/Gbps 12.5Gbps RX with 8-lap Switched-Cap DFE in 32nn CMOS         C19-4       9:45-10:10       C20-45       C20-9:45       C20-9:45       C20-9:45         C19-4       9:45-10:10       C20-9:45       C20-9:45       C20-9:45       A 2.6mW/Gbps 12.5Gbps RX with 8-lap Switched-Cap DFE in 32nn CMOS         University University       A 331 fs/bit, 51.7 mW/bit Nearest Hamming- University       M       A 512Mb Phase-Change Memory (PCM) in 90mm CMOS achieving 2b/cell       C20-49-45       C21-0         21       Device-based Circuit rechniques"       C22-1       10:30-10:55       C23-1       10:30-10:55         C11-1       0:30-10:55       C23-1       10:30-10:55       C23-1 <td></td>	
Classifier     Control of the stand of the s	
Michigani       Robust Wide-Range Voltage Conversion       CENSUM       Flash* Memory with 8F2 Cell Size       Jamain       Call       Subject 2019;45         C18-3       9:20-9:45       C20-3       9:20-9:45       C20-3       9:20-9:45         University       Call and participation of the participa	
C18-3       9:20-9:45       C19-3       9:20-9:45       C20-9:45         University of Adaptive Robustness Tuning for High Mediapher Performance Domino Logic       University of Adaptive Robustness Tuning for High Mediapher Sectors       University of Adaptive Robustness Tuning for High Mediapher Sectors       A 20 mW/Cbps 12.5Gbps RX with 8-tap Switched-Cap DFE in 32nm CMOS         C18-4       9:45-10:10       C19-4       9:45-10:10       C20-4       9:45-10:10         University of Adaptive Robustness Sectors       C19-4       9:45-10:10       C20-4       9:45-10:10         Strong Media       One Sector Sectors       C22 * DRAM and Memory Interfaces*       C22 * Power Management for Energy Harvesting*         University of A True Random Number Generator using Mediaph       Distriction Sectors       C22 * DRAM and Memory Interfaces*       C23 * Power Management for Energy Harvesting*         C21-1       10:30-10:55       C22-1       10:30-10:55       C23-1       10:30-10:55         C21-2       10:55-11:20       C22-2       10:55-11:20       C22-2       10:55-11:20         Ibm Midelia       On-only Combined CVI-VI Transistor       C22-3       11:20-11:45       C23-3       11:20-11:45         C21-3       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         C21-4       11:20-11:45       C22-3       11:20	
University of Adaptive Robustness Tuning for High Michigan       University of Attent Fatter Rate (Pasing VASE) (provided Fatter Rate)	
Midnigan       Performance Dominio Unity On Unity       Performance Dominio Unity       PerformanceDominio Unity       Performance Dom	
C18-4       9:45-10:10       C19-4       9:45-10:10       C20-4       9:45-10:10         Hideatima       A 381 fs/bit, 51.7 mWbit Nearest Hamming- University       Bit       A 512MD Phase-Change Memory (PCM) in 90m CMOS achieving 2b/cell       C20-4       9:45-10:10         C21       Device-based Circuit Techniques"       C22 "DRAM and Memory Interfaces"       C23 "Device Management for Energy Harvesting"         C21.1       10:30-10:55       C22-1       10:30-10:55       C22-1       10:30-10:55         University of A True Random Number Generator using memory in the Dependent Dielectric Breakdown       BM       3D Stackable 32mH High-K/Metal Gate SOI Embedded DRAM Prototype       MIT       Vibration energy combining with MPPT and single inductor         C21-2       10:55-11:20       C22-2       10:55-11:20       C23-2       10:55-11:20         Cumeation       On-chip Combined C-V/I-V Transistor University       C21-2       10:55-11:20       C23-2       11:20-11:45         C21-3       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         C21-4       11:45-12:10       C22-4       11:45-12:10       C23-4       11:20-11:45         C21-4       11:45-12:10       C22-4       11:45-12:10       National Cae/A Battery-Free 225 mW Buck Converter for Wireless Hambus Inc       A Tri-Modal 20Gbps/link University of A Eatoph	
Hiroshima University       A 381 fs/bit, 51.7 nW/bit Nearest Hamming- Distance Search Circuit in 65 nm CMOS       IBM       A 512Mb Phase-Change Memory (PCM) in 90nm CMOS achieving 2b/cell       Columbia University       A 4.4uW Wake-Up Receiver using Ultrasound Data Communications         C21       "Device-based Circuit Techniques"       C22 "DRAM and Memory Interfaces"       C23 "Power Management for Energy Harvesting"         Vibration       A 710-RAM Prototype       Distance Search Circuit Techniques"       C22.2 "DRAM Prototype       10:30-10:55         University of A True Random Number Generator using Michigan       Time-Dependent Dielectric Breakdown       3D Stackable 32nm High-K/Metal Gate SOL Embedded DRAM Prototype       Platform Architecture for Solar, Thermal and Witrate-buline Sense Amplifier with Array-noise On-chip Combined C-V/I-V Transistor University of Characterization System in 45-nm CMOS       C22-2       10:55-11:20       C23-2       10:55-11:20         C21-3       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         C21-4       11:45-12:10       C22-4       11:45-12:10       C23-3       11:20-11:45         C21-4       11:45-12:10       C22-4       11:45-12:10       C23-4       11:20-11:45         C21-5       12:01-12:35       A 50K/Si3:04W Resistor-based Temperature Mask Misalignment Error       A 12.8-Gbl/s/link Tr-Modal Single-Ended Memory Interface for Graphics Applications       A 12.4-Gbl/s/link	
University     Distance Search Circuit in 65 nm CMOS     IBM     90nm CMOS achieving 2b/cell     University     Data Communications       C21     "Device-based Circuit Techniques"     C22 "DRAM and Memory Interfaces"     C23 "Power Management for Energy Harvesting"       C21-1     10:30-10:55     C22-1     10:30-10:55     C23-1     10:30-10:55       Wirestly of A Ture Random Number Generator using Michigan     Time-Dependent Dielectric Breakdown     BM     30 Stackable 32nn High-K/Metal Gate SOI Embedded DRAM Prototype     Platform Architecture for Solar, Thermal and MIT       C21-2     10:55-11:20     C22-2     10:55-11:20     C23-2     10:55-11:20       Columbia     On-chip Combined C-V/LV Transistor University     In-substrate-bitline Sense Amplifier with Array-noise Operable at 10-FC Call Capacitance     Call Capacitance     University of A Reconfiguable SITTO Boost/Buck Regulator with Traves at sub-Threshold Crose-Regulation-Free Dual-Mode Dallas       0:30-12:35     C21-3     11:20-11:45     C22-3     11:20-11:45     C23-3     11:20-11:45       0:30-12:45     Electrical Monitoring of Gate and Active Area Mask Misalignment Error     Rambus Inc.     A 12:8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications     National A 408/s 36uW Resistor-based Temperature Tawan Sis 5 souw Resistor String in 0.18um CMOS     A 11:45-12:10     C23-4     11:45-12:10       C21-5     12:10-12:35     Rambus Inc.     A Tri-Modal 200Gpb/s/link D	
Outwessiv     Data Communications       C21     Device-based Circuit Techniques"     C22 "DRAM and Memory Interfaces"     C23 "Power Management for Energy Harvesting"       C21-1     10:30-10:55     C22-1     10:30-10:55     C23-1     10:30-10:55       University of A Ture Random Number Generator using Michigan     3D Stackable 22nm High-K/Metal Gate SOI Embedded DRAM Prototype     Platform Architecture for Solar, Thermal and With University       0:30-12:35     C21-2     10:55-11:20     C22-2     C22-2     C23-5     10:55-11:20       0-chip Combined C-V/I-V Transistor University     In-substrate-bitine Sense Amplifier with Array-noise gaing Scheme for Low-noise 4F2 DRAM Array On-chip Characterization System in 45-nm CMOS     C22-2     10:55-11:20       0:30-12:35     C21-3     11:20-11:45     C22-3     11:20-11:45       ItM     Electrical Monitoring of Gate and Active Area Mask Misalignment Error     A 12.8-Gb/Slink Tri-Modal Single-Ended National     A 80x5 360W Resistor-based Temperature Tawan     A 11:45-12:10     C23-4     11:45-12:10       National     A 80x5 360W Resistor-based Temperature Tawan     A 7th-Modal 20Gbps/link with On-Chip Vf Characterization and High Frequency AC Stress Capability     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Maxim       VID     C21-1     11:35-14:20     C25 "Emerging ADCs"     C26-1     13:55-14:20	
C21-1       10:30-10:55       C22-1       10:30-10:55       C23-1       10:30-10:55         University of A True Random Number Generator using Time-Dependent Dielectric Breakdown       ibM       3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype       MIT       Platform Architecture for Solar, Thermal and University of A Reconfigurable STITTO Boost/Buck Regulator. Columbia On-chip Combined C-V/I-V Transistor         Outworksity of Caracterization System in 45-nm CMOS       C22-2       10:55-11:20       C23-2       10:55-11:20         C21-3       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         C21-4       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         Mask Misalignment Error       C22-3       11:20-11:45       C23-3       11:20-11:45         Mask Misalignment Error       C22-4       11:45-12:10       C23-4       11:45-12:10         National       A 80k5/s 30/W Resistor-based Temperature Sensor using BGR-free SAR ADC with a Unevenity University weighted Resistor-based Temperature Taiwan       A Tri-Modal 20Gbps/link With On-Chip Vt Characterization and High Frequency AC Stress Capability       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Mainch University of C23-5       A Sub/S StoWH Power Aware LDO University of for Energy Harvesting Applications         Warket Mask Misalignment Error       C24-4       11:45-12:10       C23-5	
University of A True Random Number Generator using Michigan       A True Random Number Generator using Time-Dependent Dielectric Breakdown       BM       3D Stackable 32nm High-K/Metal Gate SOI Embedded DRAM Prototype       MIT       Vibration energy combining with MPPT and single inductor         C21-2       10:55-11:20       C22-2       10:55-11:20       C23-2       10:55-11:20       C23-2       10:55-11:20       C23-2       10:55-11:20       C23-2       10:55-11:20       C23-2       10:55-11:20       C23-3       11:20-11:45       C23-4       11:20-11:45       C23-4       11:20-11:45       C23-4       11:20-11:45       C21-5       C21-5       C21-5 <t< td=""><td></td></t<>	
University of A True Random Number Generator using Michigan     Time-Dependent Dielectric Breakdown     IBM     35 Backable 32/Im Fligh-N/Mella Cale SUI Im SubState-billine Sense Amplifer with Array-noise Orazoterization System in 45-nm CMOS     MIT     Vibration energy combining with MPPT and single inductor       0:30-12:36     On-chip Combined C-V/I-V Transistor University     C22-2     10:55-11:20     C23-2     10:55-11:20       0:30-12:36     On-chip Combined C-V/I-V Transistor University     Hitachi, Lui     Im-substate-billine Sense Amplifer with Array-noise geng Scheme for Low-noise 4F2 DRAM Array Operable at 10-fF Cell Capacitance     University of Datas     A Reconfigurable STITO Boox/Buck Regulator with Texas at Sub-Threshold Cross-Regulations       0:30-12:36     C21-3     11:20-11:45     C22-3     11:20-11:45     C23-3     11:20-11:45       Electrical Monitoring of Gate and Active Area Mask Misalignment Error     Rambus Inc.     A 12:8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications     National Chub A Biterry-free 225 m/B Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control       National Taiwan     A 80kS/s 36u/W Resistor-based Temperature Taiwan     A Tri-Modal 20Gbps/link With On-Chip V Characterization and High Frequency AC Stress Capability     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface PB TU/NBTI Monitoring Ring Oscillator Circuits     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5     Munic Hinversity     A 13:56MHz 2MOS Rectifier with Switched- Offset for Reversion Current Control <t< td=""><td></td></t<>	
0:30-12:35       C21-2       10:55-11:20       C22-2       10:55-11:20       C22-2       10:55-11:20         Columbia       On-chip Combined C-VI-V Transistor       In-substrate-bittine Sense Amplifier with Array-noise In-substrate-bittine Sen	
C21-2       10:55-11:20       C22-2       10:55-11:20       C23-2       10:55-11:20         Columbia       On-chip Combined C-V/I-V Transistor       In-substrate-billine Sense Amplifier with Array-noise       University of A Reconfigurable SITIOT Boost/Buck Regulator-Free Dual-Mode         Other Site Columbia       On-chip Combined C-V/I-V Transistor       Hitachi, Liu       In-substrate-billine Sense Amplifier with Array-noise       University of A Reconfigurable SITIOT Boost/Buck Regulator-Free Dual-Mode         Octorelist       C21-3       11:20-11:45       C22-3       11:20-11:45       C22-3       11:20-11:45         IBM       Mask Misalignment Error       C21-4       11:45-12:10       C22-4       11:45-12:10       C23-4       11:45-12:10         National       A 80x5/s 36uW Resistor-based Temperature Taiwan       Sensor using BGR-free SAR ADC with a Uneventy- University weighted Resistor String in 0.18ur CMOS       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munich Technology       A Rully-Integrated System Power Aware LDO for Energy Harvesting Applications         0:21-5       12:10-12:35       C21-5       12:10-12:35       A 13:56/Hiz CMOS Rectifier with Switched- Offset for Reversion Current Control         0:22-4       12:45-12:10       C23-5       12:10-12:35       A 13:56/Hiz CMOS Rectifier with Switched- Offset for Reversion Current Control         0:21-5       12:10-12:	
Columbia University       On-chip Combined C-V/I-V Transistor Characterization System in 45-nm CMOS       Image: In-substrate-bitline Sense Amplifer with Array-onice Derable at 10-ff Cell Capacitance       University Derable at 10-ff Cell Capacitance       University of A Reconfigurable STITC Boox/Buck Regulator with Texas of Control for Energy Harvesting Applications         0:30-12:36       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         IBM       Electrical Monitoring of Gate and Active Area Mask Misalignment Error       A 12.8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications       Valuersity University University       National A 402/KP Phase Lead Control         National Taiwan       A 80KS/s 36uW Resistor based Temperature Taiwan Sensor using BG-Rifeer SAR ADC with a Unevenity with On-Chip V Characterization and High Frequency AC Stress Capability       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munici University Weighted Resistor String in 0.18um CMOS       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munici University University       A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications         C21-5       12:10-12:35       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munici University University       A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications         C21-5       12:10-12:35       A Tri-Modal 20Gbps/link Differential/DDR3/GD	
University     Characterization System in 45-nm CMOS     Intach, Lib. guidation of the Coll Capacitance     Data Sub- Integration Cross-Regulation-Free UnderNobe       0:30-12:36     C21-3     11:20-11:45     C22-3     11:20-11:45     C23-3     11:20-11:45       Electrical Monitoring of Gate and Active Area Mask Misalignment Error     Electrical Monitoring of Gate and Active Area Mask Misalignment Error     A 12.8-Gb/s/link Tri-Modal Single-Ended memory Interface for Graphics Applications     National Chao Markon Interface Control Free Update A 12.8-Gb/s/link Tri-Modal Single-Ended Mask Misalignment Error     National Chao A Sattery-free 225 nW Buck Converter for Wireless Removes Incerve Marvesting with Dynamic On/Off Time and Adaptive Phase Lead Control       National Taiwan     A 80KS/s 36uW Resistor-based Temperature Taiwan     A 71-Modal 20Gbps/link Mith On-Chip Vt Characterization and High Frequency AC Stress Capability     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     C23-5     12:10-12:35       IBM     with On-Chip Vt Characterization and High Frequency AC Stress Capability     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24-1     13:55-14:20     C25-1     13:55-14:20     C26-1     13:55-14:20	
C21-3       11:20-11:45       C22-3       11:20-11:45       C23-3       11:20-11:45         IBM       Electrical Monitoring of Gate and Active Area Mask Misalignment Error       A 12.8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications       National Cube of Adattery-free 225 nW Buck Converter for Wireless and Adaptive Phase Lead Control         C21-4       11:45-12:10       C22-4       11:45-12:10       C23-4       11:45-12:10         National Tawan Tawan Bensor using BCR-free SAR ADC with a Unevenly- weighted Resistor String in 0.18um CMOS       C21-4       11:45-12:10       C23-4       11:45-12:10         C21-5       12:10-12:35       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munich University       Munich Weighted Resistor String in 0.18um CMOS       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munich University       A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications         PBTI/NBTI Monitoring Ring Oscillator Circuits IBM       with On-Chip Vt Characterization and High Frequency AC Stress Capability       C25 "Emerging ADCs"       C26 "Power Management Technique"         C24-1       13:55-14:20       C25-1       13:55-14:20       C26-1       13:55-14:20	
0:30-12:35     Electrical Monitoring of Gate and Active Area Mask Misalignment Error     A 12.8-Gb/s/link Tri-Modal Single-Ended Memory Interface for Graphics Applications     National Chao Tung     A Battery-free 225 nW Buck Converter for Wireless RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control       C21-4     11:45-12:10     C22-4     11:45-12:10     C23-4     11:45-12:10       National Taiwan     A 80x5/s 36uW Resistor-based Temperature Taiwan     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University weighted Resistor String in 0.18um CMOS     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University Differential/DDR3/GDDR5 Memory Interface     Munich University Weighted Resistor String in 0.18um CMOS     A Tai-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University Weighted Resistor String in 0.18um CMOS     A Tai-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University Weighted Resistor String in 0.18um CMOS     A Tai-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich Winkin University Frequency AC Stress Capability     A Fully-Integrated System Power Aware LDO Munich Differential/DDR3/GDDR5 Memory Interface       With On-Chip Vt Characterization and High Frequency AC Stress Capability     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24 * 103:55-14:20     C25 * 13:55-14:20     C26 * 13:55-14:20     C26 * 13:55-14:20	
IBM       Mask Misalignment Error       Rambus inc       Memory Interface for Graphics Applications       Tung       RF Energy Harvesting with Dynamic On/Off Time and Adaptive Phase Lead Control         C21-4       11:45-12:10       C23-4       11:45-12:10         National       A 80x5/s 36uW Resistor-based Temperature Taiwan       Remory Interface for Graphics Applications       Munich University weighted Resistor String in 0.18um CMOS       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munich University Memory Interface for Graphics Applications       A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications         C21-5       12:10-12:35       Rambus Inc.       A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface       Munich University Memory Interface for Reversion Current Control       A Stable Control for Energy Harvesting Applications         BM       with On-Chip Vt Characterization and High Frequency AC Stress Capability       KC25 "Emerging ADCs"       C26 "Power Management Technique"         C24-1       13:55-14:20       C25-1       13:55-14:20       C26-1       13:55-14:20	
C21-4     11:45-12:10     C22-4     11:45-12:10       National Taiwan     A 80K5/s 36uW Resistor-based Temperature Sensor using BGR-free SAR ADC with a Unevenly University weighted Resistor String in 0.18um CMOS     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University of Temperature     A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications       C21-5     12:10-12:35     C23-5     12:10-12:35       MW     with On-Chip Vt Characterization and High Frequency AC Stress Capability     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24-1     13:55-14:20     C25-1     13:55-14:20     C26-1     13:55-14:20	
National Taiwan     A 80x5/s 36uW Resistor-based Temperature Sensor using BGR-free SAR ADC with a Unevenity University weighted Resistor String in 0.18um CMOS     A Tri-Modal 20Gbps/link Differential/DDR3/GDDR5 Memory Interface     Munich University Temperature     A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications       C21-5     12:10-12:35 PBT/INBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability     C25 "Emerging ADCs"     C23-5     12:10-12:35 A T3-56MHz CMOS Rectifier with Switched- Offset for Reversion Current Control       C24     Digital Processors     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24-1     13:55-14:20     C26-1     13:55-14:20	
Taiwan     Sensor using BGR-free SAR ADC with a Uneventy- weighted Resistor String in 0.18um (MOS)     A Intrividual 2005pisition Differential/DDR3/GDDR5 Memory Interface     A Fully-Integrated System Power Aware LDO for Energy Harvesting Applications       C21-5     12:10-12:35     C23-5     12:10-12:35       PBTI/NBTI Monitoring Ring Oscillator Circuits informed Acceptability     C23-5     12:10-12:35       IBM     with On-Chip Vt Characterization and High Frequency AC Stress Capability     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24-1     13:55-14:20     C25-1     13:55-14:20     C26-1     13:55-14:20	
C21-5     12:10-12:35       PBTI/NBTI Monitoring Ring Oscillator Circuits       IBM     with On-Chip Vt Characterization and High Frequency AC Stress Capability       C24     Digital Processors       C24-1     13:55-14:20       C24-1     13:55-14:20	
PBTI/NBTI Monitoring Ring Oscillator Circuits with On-Chip Vt Characterization and High Frequency AC Stress Capability     A 13.56MHz CMOS Rectifier with Switched- Offset for Reversion Current Control       C24 "Digital Processors"     C25 "Emerging ADCs"     C26 "Power Management Technique"       C24-1     13:55-14:20     C26-1     13:55-14:20	
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C24 "Digital Processors"         C25 "Emerging ADCs"         C26 "Power Management Technique"           C24-1         13:55-14:20         C25-1         13:55-14:20         C26-1         13:55-14:20	
Intel A 45nm 48-core IA processor with Variation- Keio ADC with Tri-Level Comparator in 40 nm IBM with High DC Accuracy, Load Response Time Below	
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University of A 75µW, 16-Channel Neural Spike-Sorting National A 1-V, 8b, 40MS/s, 113uW Charge-Recycling MEMS-switch-based Power Management with Zero- cretifornia - Charge-Recycling	
California Los Angeles Processor with Unsupervised Clustering Los Angeles	
C24-3 14:45-15:10 C25-3 14:45-15:10 C26-3 14:45-15:10	
3:55-16:00 University of A 7.4mW 200MS/s Wideband Spectrum Oregon Digitally Synthesized Stochastic Flash ADC A 210nW 29.3 ppm/degree 0.7 V Voltage	
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Los Angeles         Cognitive Radios         University         Osing Only Standard Digital Cells         to 130 degree in 0.13 um CMOS           C24-4         15:10-15:35         C25-4         15:10-15:35         C26-4         15:10-15:35	
A Reconfigurable 1GSps to 250MSps, 7-bit to A Voltage-Reference-Free Pulse Density Modulation (VRF-PDM) 1-	
Mediatek Fully Integrated UNUS SOC for 3D Blu-ray Inc. Player Applications 9-bit Highly Time-Interleaved Counter ADC in University of Vinput Switched-Capacitor 12 Voltage Converter with Output University of Vinput Switched-Capacitor 12 Voltage Converter with Output	
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C24-5 15:35-16:00 C25-5 15:35-16:00 C26-5 15:35-16:00 C26-5 15:35-16:00	
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University Processor for Wearable Vision Applications University Using 2-Level PWWM Modulation Dallas Control	
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