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Program no. **Title**
Abstract

2A-1 Scaling of SOI FinFETs down to Fin Width of 4 nm for the 10nm technology node

Using a novel structure, we fabricate SOI FinFETs with fin width of 4nm, fin pitch of 40nm, gate length of 20nm. We achieve robust yield on arrays of thousands of fins with high structural integrity. We experimentally observe Dfin-dependent performance degradation, increased variability, and Vt shift. Capacitance measurements exhibit quantum confinement behavior which has been predicted to pose a fundamental limit to scaling FinFETs below 10nm Lg.

2A-2 Sub-25nm FinFET with Advanced Fin Formation and Short Channel Effect Engineering

FinFET devices achieving N/P Ion values of 1250/950 uA/um at 100nA/um at 1V, 1300/1000 uA/um with self-heating correction, are demonstrated, using a dual work function gate-first process flow at 100 nm gate pitch and 40 nm fin pitch. Ring-oscillator (RO, FO=3) functionality has been demonstrated, showing excellent V_{DD} scalability. We have also demonstrated logic scan chain functionality and yield improvement by optimizing the gate stack process. An optimized SIT process has been developed to improve short-channel characteristics in devices with a small number of fins in a narrow active area, which is also critical for manufacturability improvement. Various conformal doping techniques for NFET/PFET are optimized to improve device performance.

2A-3 Modeling of Width-Quantization-Induced Variations in Logic FinFETs for 22nm and Beyond

The nature of FinFET devices prohibits continuous width scaling and introduces a digitization of device width. This introduces an intrinsic variation in the device that is absent in conventional planar devices. For the first time we address how a composite Fin device can be modeled correctly. We show that the DIBL vs. SS relationship for the composite device is an easily accessible indicator for the intrinsic variations observed in a composite device.

2A-4 Critical Discussion on (100) and (110) Orientation Dependent Transport: nMOS Planar and FinFET

Electron mobility on (100) and (110) planar FETs and SOI FinFETs was evaluated. It is experimentally demonstrated that the (110) sidewall of FinFETs does not present a drawback in terms of electron mobility - contrary to results obtained on (110) planar MOSFETs. This is comprehensively explained by a combination of first principles and empirical approach closely matching the experimental data.

2B-1 Forming-Free Nitrogen-Doped AlO_x RRAM with Sub-uA Programming Current

Nitrogen-doped AlO_x Resistive RAM has been integrated on CMOS. The memory cell requires no forming, and sub-uA programming currents. The cell is capable of multi-bit storage, reliable for over 10^5 switching cycles and 10 years retention at 125°C.

2B-2 Evidences of Anodic-oxidation Reset Mechanism in TiN/NiO/Ni RRAM Cells

By means of conductance modeling, physical characterization, and stack engineering in 80nm-wide contact-hole cells, we clearly evidence for TiN/NiO/Ni RRAM systems that the reset switching corresponds to a partial Ni-rich filament constriction due to anodic oxidation mechanism at the interface with the Ni anode.

2B-3 Resistive Switching AlO_x-Based Memory with CNT Electrode for Ultra-Low Switching Current and High Density Memory Application

We report the first AlO_x-based resistive switching memory (RRAM) using carbon nanotubes (CNT) as contact electrodes. CNTs with average diameter of 1.2nm effectively localize the conduction filaments (CFs). The Al/AlOx/CNT device successfully switches over 10^4 cycles with less than 5uA programming current. Ultimate scaling down the device to 6nm x 6nm is realized by the CNT/AlOx/CNT cross-point structure and 10^4 switching cycles are achieved.This work is the first step toward RRAM with nm-scale electrodes. It paves the way for future high density, low power non-volatile RRAM memory application.

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2B-4 Deterministic and Stochastic Component in RESET Transient of HfSiO/FUSI Gate RRAM Stack

Analysis of RRAM filament properties in SiO2/HfSiO/NiSi shows how the minimal achievable current in High Resistance State (HRS) depends on the nature of the filament, quantifiable through a quantum mechanical conduction model. Lowest HRS current is obtained for narrow, metallic filaments. Additionally, RTN adds a stochastic component to the HRS current that is minimized for wider, less conductive filaments, making these more robust at reading voltage.

3A-1 Aggressively Scaled High-k Last Metal Gate Stack with Low Variability for 20nm Logic High Performance and Low Power Applications

An aggressively scaled high-k last metal gate (HKMG) stack was successfully implemented for 20nm high performance and low power applications and even below. Key technologies include aggressive Tinv scaling down to 1.1nm with new HK, suppression of Vfb roll-off, metal layer control for Vt and its excellent uniformity, and metal gate stress engineering for performance improvement.

3A-2 Gate-Last vs. Gate-First Technology for Aggressively Scaled EOT Logic/RF CMOS

We report on gate-last technology for improved effective work function tuning with 200meV higher p-EWF at 7A EOT, 2 times higher f_{max} performance, and further options for channel stress enhancement than with gate-first. Additional key features: 1) scavenging technique yielding UT-EOT down to 5A is demonstrated in gate-last, with high-k deposited first, through the use of an Etch-Stop-Layer with composite nature and similar TDDB reliability to gate-first; 2) controlled alloying for EWF engineering is obtained by careful material selection and tuned metals thicknesses ratio; 3) suppression of abnormal L_{gate}- and W_{gate}-dependence on $J_{G,}$ EOT and NBTI for devices with both high-k and metal deposited last demonstrates the potential for improved UT-EOT control down to small devices with this scheme.

3A-3 Full Metal Gate with Borderless Contact for 14 nm and Beyond

Tungsten based full metal gate (FMG) stacks that are equivalent to or better than metal inserted poly Si (MIPS) stack have been developed for borderless contact for 14nm and beyond. FMG stacks show excellent T_{inv} scaling (0.92 and 1.15nm for NFET and PFET, respectively) and enhanced hole mobility by 20% compared to MIPS gate stack. Fully integrated short channel devices and borderless contacts are demonstrated at 80nm contacted gate pitch.

3A-4 A 28nm Poly/SiON CMOS Technology for Low-Power SoC Applications

This paper presents a state-of-the-art 28nm CMOS technology using conventional poly gate and SiON gate dielectric (Poly/SiON) with best-in-the-class transistor performance, SRAM SNM (static noise margin), MOM capacitance density and mismatch, and ULK (k=2.5) interconnect. The ION are 683 and 503 uA/um (at IOFF = 1nA/um, VDD=1V) for the n- and p-MOSFET, respectively. (With normalized tOX and VDD, these values are higher than prior publication by 5%/15%). The 6T-SRAM is aggressively scaled to <0.124um^2 with SNM of 193mV at 1.0V and 144mV at 0.7V. The via and metal resistances, and the metal-line RC time constants are competitive and well controlled. The characteristics for the RF passive components (MOM capacitor, varactor, and inductor) are also excellent.

3A-5 RF and Mixed-Signal Performances of a Low Cost 28nm Low-Power CMOS Technology for Wireless System-on-Chip Applications

Extending RF/MS-CMOS to 28nm low-power Poly/SiON node for the next generation wireless SoC applications makes most economic sense because, beyond 28nm, costly HiK/MG, double-patterning, complex local interconnect, and multi-gate structures will be required for moreMoore scaling. Competitive peak fT/Fmax of 349/265GHz for NMOS, 242/184GHz for PMOS, with excellent mixed-signal properties, are reported. Effects associated with layout dependency, poly pitch, and DFM-related rules, are shown to degrade fT by ~10%, thus, require careful optimization.

3B-1 High Performance Unipolar AlO_y/HfO_x/Ni based RRAM Compatible with Si Diodes for 3D Application

We report a high performance unipolar RRAM with Ni-electrode /HfO_x /AlO_y /p+-Si structure, compatible with Si-diode selector for 3D cross-bar implementation. Highlights of the demonstrated RRAM include 1) a high on/off resistance ratio of ~10^5; 2) ~100% device yield on a 6-inch wafer; 3) excellent cycle-to-cycle and device-to-device uniformity of switching parameters (e.g. Vset, Vreset, and HRS/LRS currents); 4) satisfactory pulse switching endurance (> 10^6 cycles); 5) high temperature retention (>10^5 s @ 120 °C), and high temperature operating stability (> 200 °C) without threshold resistive switching; 6) a fast set/rest speed of ~10/30 ns; 7) full CMOS compatible materials and process: with p+-Si bottom electrode, avoiding the use of noble metals, e.g. Pt.

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3B-2 Theoretical Study of the Resistance Switching Mechanism in Rutile TiO_{2-x} for ReRAM: the Role of Oxygen Vacancies and Hydrogen Impurities

We study the resistance switching mechanism of rutile TiO_2 using ab initio calculations based on DFT. Ordering of the oxygen vacancies substantially increases the conductivity of TiO_2 by forming a conductive channel, i.e. ON state. We find that the diffusion of either oxygen or hydrogen atoms into the conductive channel causes the rupture of the conductive filament resulting in the transition from ON state to OFF state.

3B-3 Highly Reliable and Fast Nonvolatile Hybrid Switching ReRAM Memory Using Thin Al_2O_3 Demonstrated at 54nm memory Array

For the first time, very fast (10ns at even Reset) and high reliable (150°C 100h) ReRAM memory was demonstrated at 54 nm 256k bits array. Reset current successfully decreased up to 20uA using Al_2O_3 which acts as a tunnel barrier and filament source in TiO_2/Al_2O_3 stack. From statistical analysis, the possibility of increasing array size and the key factor of resistance distribution were investigated.

3B-4 High Thermal Robust ReRAM with a New Method for Suppressing Read Disturb

A thermal robust ReRAM with a new method for suppressing read disturb was investigated for the automobile application. Asymmetric structure such as $Ru/TiO_2/Ta_2O_5/TiO_2/W$ with a new operation method (write: positive bias for top Ru/read: positive bias for bottom W) could much improved the read disturb immunity. Furthermore, scalability up to 28-nm node device, low switching current (25uA), low forming voltage (<3V), high read speed (<10 nsec), and high thermal robustness (200°C) were achieved.

3B-5 Bi-layered RRAM with Unlimited Endurance and Extremely Uniform Switching

We demonstrate resistive random access memory (RRAM) architecture with bi-layered switching element for reliable resistive switching memory. Based on the modulated Schottky barrier modeling, several key functions to achieve a realiable bipolar switching property are extracted. Our device shows an excellent memory performance such as enduracne of 10^{11} cycles at 30ns, data retention of $>10^4$s at 200°C, and calculated bit error rate below 10^{-11}.

4A-1 High Mobility Ge pMOSFETs with ~1nm Thin EOT Using $Al_2O_3/GeO_x/Ge$ Gate Stacks Fabricated by Plasma Post Oxidation

A novel plasma post oxidation method has been proposed to form an $Al_2O_3/GeO_x/Ge$ gate stack by using oxygen plasma through a thin ALD Al_2O_3 layer. This Ge gate stack is shown to simultaneously realize both thin EOT of ~1 nm and low Dit of <1E11 $cm^{-2}eV^{-1}$. Ge pMOSFETs, fabricated by employing this method, have demonstrated superior device operation with high hole mobilities of 437, 526 and 345 cm^2/Vs on (100), (110) and (111) Ge substrates, respectively. These mobilities on (100) and (110) are the highest under ~1 nm EOT among the results reported so far. Also, this is the first demonstration of (110) and (111) Ge pMOSFET operations in this ultrathin EOT range.

4A-2 High Performance Extremely-thin Body III-V-On-Insulator MOSFETs on a Si Substrate with Ni-InGaAs Metal S/D and MOS Interface Buffer Engineering

We have demonstrated the extremely thin body (ETB) $In_{0.7}Ga_{0.3}As$-on-insulator (-OI) MOSFETs on Si substrates with Ni-InGaAs S/D structures. It has been found that low doping concentrations, In-rich channels ($In_{0.7}Ga_{0.3}As$), and buffer engineering provide high mobility of 2810 cm^2/Vs even the total InGaAs thickness of 10 nm. This is the first demonstration of ETB III-V-OI MOSFETs combined with the Schottky-barrier free metal S/D technology. We have also achieved excellent I_D-V_G characteristics with I_{on}/I_{off} ratio of over 10^7 and low S.S. of 103 mV/dec in 2/1/3 nm-thick InGaAs MOSFETs with buffer layers.

4A-3 CMOS integration of InGaAs nMOSFETs and Ge pMOSFETs with Self-align Ni-based Metal S/D Using Direct Wafer Bonding

We have demonstrated the integration of InGaAs nMOSFETs and Ge pMOSFETs with self-align Ni-Ge and Ni-InGaAs metal source/drain on a Ge substrate by direct wafer bonding, for the first time. Ni-based metal source/drain allows us to fabricate high performance nMOSFETs and pMOSFETs at the same time. InGaAs nMOSFET and Ge pMOSFET have exhibited the high electron and hole mobility of 1800 and 260 cm^2/Vs and the mobility enhancement against Si of 3.5^x and 2.3^x, respectively.

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4A-4 Scalable TaN Metal Source/Drain & Gate InGaAs/Ge n/pMOSFETs

We propose a scalable CMOS fabrication process for high mobility InGaAs/Ge dual channels using a common TaN metal source/drain and gate (Metal-SD&G) under consideration of material band lineup. By combining common TaN Metal-SD with compatible TaN/Al_2O_3 gate stacks, we have successfully demonstrated operation of both InGaAs nMOS and Ge pMOS devices fabricated at the same time. Excellent InGaAs/Ge n/pMOSFET performances, such as the SS of 70mV/dec and 100mV/dec for InGaAs nMOS and Ge pMOS, respectively, have been achieved. We have also verified the scalability of TaN Metal-SD&G InGaAs nMOSFETs down to 50nm with high immunity to SCEs.

4A-5 A 0.021 um^2 trigate SRAM Cell with Aggressively Scaled Gate and Contact Pitch

We present the highest density demonstration of CMOS technology reported to date featuring a 6T SRAM cell size of 0.021 um^2. The motivation for this work was to explore the limits of device patterning and basic module integration at dimensions relevant to the 10 nm node. A trigate device architecture with a minimum contacted gate pitch and minimum contacted fin pitch of 50 nm was used as the target technology for this demonstration.

4B-1 A Highly Scalable Vertical Gate (VG) 3D NAND Flash with Robust Program Disturb Immunity Using a Novel PN Diode Decoding Structure

A novel PN diode decoding method for 3D NAND Flash is proposed. The PN diodes are fabricated self-aligned at the source side of the Vertical Gate (VG) 3D NAND architecture. Contrary to the previous 3D NAND approaches, there is no need to fabricate plural string select (SSL) transistors inside the array, thus enabling a highly symmetrical and scalable cell structure. A novel three-step programming pulse waveform is integrated to implement the program-inhibit method, capitalizing on that the PN diodes can prevent leakage of the self-boosted channel potential. A large program-disturb-free window >5V is demonstrated.

4B-2 A Highly Manufacturable Integration Technology of 20nm Generation 64Gb Multi-Level NAND Flash Memory

Multi-level NAND flash memories with a 20nm design rule have been successfully developed for the first time. A 20nm rule wordline (WL) and bitline (BL) direction have been realized by Spacer Patterning Technology (SPT) of ArF immersion lithography. Key integration technologies include WL airgap with separate gate etch process and optimized control gate (CG) poly deposition process. In addition, many physical and electrical challenges are successfully demonstrated to overcome scaling limit of 20nm technology.

4B-3 A Novel Low-Voltage Hot-Carrier (LVHC) Programming Method for Scaled NAND Flash Cell

A novel low-voltage, hot-carrier programming method for NAND flash cell is presented. By suitably controlling the NAND string's conductance, a sufficient program current along with a high heating field is induced to cause hot carrier injection. This method greatly alleviated the requirements for high-voltage devices and their fabrication process. Besides, it is less sensitive to process variation and possesses better reliability than FN programming.

4B-4 A Novel Junctionless All-Around-Gate SONOS Device with a Quantum Nanowire on a Bulk Substrate for 3D Stack NAND Flash Memory

A novel junctionless all-around-gate SONOS device (4nm width, 20nm gate length) with the homogeneously n+-doped quantum SiNW is demonstrated on a bulk substrate. The results show a high read current (> 10 uA), a large VT margin (> 6.5 V), a narrowed distribution of the erased VT, and improved cyclic endurance. Moreover, the vertically integrated 9-layer single-crystalline SiNWs are successfully achieved by the developed deep RIE process for 3D NAND Flash memory.

4B-5 Extraction of 3-D Trap Position in NAND Flash Memory Considering Channel Resistance of Pass Cells and Bit-Line Interference

We extract the exact position and energy of trap at tunnel oxide which induces RTN by considering the channel resistances of pass cells in floating gate NAND flash memory string. Moreover, the trap position along the width direction is also founded by using an interference effect between BLs.

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5A-1 Phase Transformation Kinetics of HfO_2 Polymorphs in Ultra-thin Region

Thermodynamically non-equilibrium phase transformation in ultra thin HfO_2 films was investigated. Amorphous HfO_2 is crystallized into stable monoclinic phase via metastable cubic one. It was also demonstrated that the k-value of cubic-HfO_2 was ~50. Kinetic analysis according to Mehl-Avrami-Johnson law pointed out the cubic-HfO_2 is stable for practical use thanks to the suppression of monoclinic nucleus formation.

5A-2 Novel Tellurium Co-Implantation and Segregation for Effective Source/Drain Contact Resistance Reduction and Gate Work Function Modulation in n-FinFETs

We report the demonstration of a new contact resistance reduction technology for n^+ Si S/D using Tellurium (Te) implant and segregation, achieving a low electron SBH of 0.11 eV. The Te implant reduced contact resistance in n-FinFETs by 40 %. When integrated in a process flow where Te is also introduced into the gate, improvement in gate electrostatic control is observed, leading to an improvement in ballistic efficiency. At IOff of 100 nA/um, Te implant increases IOn by 22 % as compared with control FinFETs without Te implant.

5A-3 Exact Control of Junction Position and Schottky Barrier Height in Dopant-Segregated Epitaxial $NiSi_2$ for High Performance Metal Source/Drain MOSFETs

This paper reports junction position control and the Schottky barrier height tuning in ultrathin SOI MOSFETs with epitaxial $NiSi_2$ source/drain (S/D). We demonstrate the junction position control in the lateral direction with preserving the (111) facet in 8-nm-thick SOI using epitaxial NiSi2 growth. Schottky barrier height at epitaxial $NiSi_2$ can be easily controlled by P+ implanted dose using dopant segregation technique, and the saturation drain current ($I_{D\,Sat}$.) increases due to lowering Schottky barrier height. Thus, epitaxial $NiSi_2$ is a promising metal S/D for future MOSFETs.

5A-4 An Efficient Manufacturing Technique based on Process Compact Model to Reduce Characteristic Variation beyond Process Limit for 40 nm Node Mass Production

Practical manufacturing technique to reduce characteristic variation of 40 nm CMOS device has been developed. Novel feed-forward (FF) system at gate formation for tight gate length control, and FF techniques at both halo implan-tation and Spike RTA for device centering have been applied. In addition, adjusting wafer notch angle at each critical process step has been utilized to suppress within-wafer variation. As a result, total V_{th} variation at mass production has been reduced by 46%.

5B-1 Endurance and Scaling Trends of Novel Access-Devices for Multi-Layer Crosspoint-Memory Based on Mixed-Ionic-Electronic-Conduction (MIEC) Materials

We demonstrate compact integrated arrays of BEOL-friendly novel access devices (AD) based on Cu-containing MIEC materials.
In addition to the high current densities and large ON/OFF ratios needed for Phase Change Memory (PCM), scaled-down ADs also exhibit larger voltage margin Vm, ultra-low leakage (<10pA), and much higher endurance (>10^8) at high current densities. Using CMP, all-good 5x10 AD arrays with V_m > 1.1V are demonstrated in a simplified CMOS-compatible, diode-in-via (DIV) process.

5B-2 Phase-change Memory Driven by poly-Si MOS Transistor with Low Cost and High-programming Gigabyte-per-second Throughput

A phase-change memory (PCM) driven by poly-Si MOS transistors was fabricated. The thin phase-change-material layer deposited directly on the channel silicon layer in the PCM enables low-current reset operation (45 uA) compared to the conventional memory structure. This memory-cell con-figuration enables both a poly-Si MOS-driven stackable memory array and large degree programming parallelization. A contactless simple cell structure makes it possible to reduce the cell size to $4F^2$ and the number of process steps. Low cost and gigabyte-per-second programming throughput are thus made possible by this stackable phase-change memory.

5B-3 A Method to Maintain Phase-Change Memory Pre-coding Data Retention after High Temperature Solder Bonding Process in Embedded Systems

For the first time we demonstrate that a Phase Change Memory (PCM) packaged chip can hold pre-coded data after an industrial standard lead free solder bonding reflow process. Good "0" and "1" state distributions are retained in a 90nm 128Mb PCM chip after the soldering process. Furthermore, the tested chip endures more than 10 million write cycles after the pre-coding and high temperature process.

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5B-4 A 1.4uA Reset Current Phase Change Memory Cell with Integrated Carbon Nanotube Electrodes for Cross-Point Memory Application

A cross-point phase change memory cell working close to its ultimate scaling limit is demonstrated for the first time with an ultra low reset current of 1.4uA. This is the lowest value ever reported. Carbon nanotubes are utilized as the bottom electrode of the cell, which bring the lithography-independent critical dimension down to 1.2nm. Good electrical characteristics obtained demonstrate the functionality and potential viability of PCM for highly scaled ultra-dense memory at 2.5nm node.

6B-1 High Performance Graphene FETs with Self-aligned Buried Gates Fabricated on Scalable Patterned Ni-Catalyzed Graphene

For the first time, we report a scalable technique to fabricate graphene transistors with self-aligned buried gates process. The high performance buried-gate graphene transistor has excellent field effect mobility of 6,100 and 24,000 cm^2 per volt second before and after subtraction of contact resistance. To the best of our knowledge, this is the highest room temperature mobility for CVD graphene FETs reported to date. This result paves the way for manufacturable high quality graphene transistor technology.

6B-2 Non-Volatile Graphene Channel Memory for Flexible Electronics and 3D Multi-stack Ultra-high-density Data Storages

A non-volatile memory (NVM) exploiting single-layer graphene (SLG) as a channel material has been fabricated through low temperature processes below 250°C and characterized for the first time. The injection of electrons into the trap sites of a triple high-k dielectrics stack results in a memory window of more than 9.0V. The NVGMs fabricated by processes compatible with flat panel display (FPD) can be utilized for flexible electronics and high-density 3D multi-stack memory cells.

6B-3 A Novel BEOL Transistor (BETr) with InGaZnO Embedded in Cu-Interconnects for On-chip High Voltage I/Os in Standard CMOS LSIs

A novel BEOL transistor is developed in Cu interconnects with wide-band-gap InGaZnO (IGZO) film for on-chip high voltage I/Os in standard CMOS LSIs only by one additional mask. Thickness control of both the IGZO channel and gate SiN is a key to achieve high on-current with low leakage. Ability of high voltage operation with small feature size is expected as an interface bridge for signal conversion between CMOS core-logics and peripheral devices driven with high-voltages.

6B-4 Impact of Oxidation Induced Atomic Disorder in Narrow Si Nanowires on Transistor Performance

Theoretical investigations are presented for the effects of atomic disorder, which is always present in Si/SiO_2 interface, on the device performance for the first time. We show that the drain current is significantly reduced by a factor of 2 due to random configuration of Si atoms near the Si/SiO_2 interfaces in a nanowire with 2.7 nm width. NFET is more easily affected by the disorder because of localized states near the conduction-band bottom. Suppression of the atomic disorder is a key to obtain good performance of nanowire FETs.

6B-5 Comparison of Performance, Switching Energy and Process Variations for the TFET and MOSFET in Logic

A detailed circuit assessment of 20nm TFET versus MOSFET operating near device threshold supply voltage, including the consideration of process variations, is reported. For very low power logic applications requiring near device threshold supply voltage, the results show that TFET logic can operate at equal standby power and switching energy to MOSFET, but with 8x performance advantage. The study also shows that device parameter variation is not a factor for differentiation between MOSFET and TFET.

7-1 ETSOI CMOS for System-on-Chip Applications Featuring 22nm Gate Length, Sub-100nm Gate Pitch, and 0.08um² SRAM Cell

We report ETSOI CMOS with 22nm gate length and sub-100nm gate pitch for system-on-chip (SoC) applications. Competitive drive current of I_{on}=1150/1050uA/um at I_{off}=100nA/um for high performance (HP) and I_{on}=920/880uA/um at I_{off}=1nA/um for low power (LP) NFET/PFET, respectively, at V_{DD}=1V. High density 6-T SRAM cells down to 0.08um² are demonstrated. ETSOI ring oscillator exhibits 25% improvement compared to 28nm bulk LP. Cost-free ETSOI epitaxy resistors and gate diodes are also demonstrated.

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7-2 Comprehensive SRAM Design Methodology for RTN Reliability

In this paper, a comprehensive design flow for achieving reliable SRAMs against random telegraph noise (RTN) is presented. The tailing information of RTN amplitude distributions is important for guardbanding, and can be directly extracted from SRAM test results. Monte Carlo simulation is in excellent agreement with the measurements, and can be used for detailed design. A simple extrapolation method for intuitive understanding of long term RTN impact is also proposed.

7-3 Unified Understanding of V_{th} and I_d Variability in Tri-Gate Nanowire MOSFETs

We systematically study V_{th} and Id variability of nanowire transistors. The universal line appears in Pelgrom plot for a wide range of gate length, nanowire width and height. Deviation of the narrowest transistor from the universal line was eliminated by suppressing the parasitic resistance. A_{vt} of nanowire transistors is lower than planar transistors due to gate grain alignment. Improvement of roughness limited mobility and its fluctuations are essential to reduce I_{dsat} and I_{dlin} variations.

7-4 1mA/um-I_{ON} Strained $SiGe_{45\%}$-IFQW pFETs with Raised and Embedded S/D

A 2nd generation of SiGe-IFQW pFETs is presented in this work. $SiGe_{25\%}$-embedded Source/Drain was implemented, leading to an excellent short channel control and logic performance. No narrow-width effect was found and a multi-V_{TH} strategy is also offered. Performance of the strained-IFQW pFETs was finally demonstrated at lower V_{DD}.

8A-1 TSV Process Optimization for Reduced Device Impact on 28nm CMOS

A through-silicon-via (TSV) process is demonstrated on 28nm CMOS baseline with good electrical performance and low cost. TSV leakage, yield, C-V flat-band shift, Cu contamination, and reliability are significantly improved via process optimization. The preferred TSV processing could relax TSV stress and minimize keep-out zone (KOZ). In this study, we also address the impact of multiple-TSVs additive stress impact, TSV signal coupling effect, and TSV depletion impact to assess the power-TSV plug cell in design practice.

8A-2 Yield and Reliability of 3DIC Technology for Advanced 28nm Node and Beyond

A stacked three-dimension integrated circuit (3D-IC) of 28nm chips was demonstrated. Key enabling technologies such as through silicon via (TSV) formation, wafer thinning, redistribution layer (RDL), micro bump and joint were developed for chip stacking and interconnect functions evaluation. The excellent performances of 3D-IC yield and reliability characteristics are key milestones in promising manufacturability of 3D-IC by silicon foundry technology.

8A-3 Novel GAA Raised Source / Drain Sub-10-nm Poly-Si NW Channel TFTs with Self-Aligned Corked Gate Structure for 3-D IC Applications

A novel gate-all-around raised source / drain sub-10-nm poly-Si nanowire (NW) channel TFTs with self-aligned corked gate structure (GAA RSDNW-TFTs) have been successfully demonstrated. It is through the use of a novel fabrication process requiring no advanced lithographic tools. The corked gate (CG) structure, only the poly gate pattern was etched, reduces complex of process significantly. For the first time, several properties of this 3D architecture are explored: (i) the Si NW dimension is about 7 nm ² 12 nm and a superior smooth elliptical shape is obtained in the category of poly-Si NW TFTs. (ii) the temperature dependence and the instability under PBTI stress of the main electrical parameters are proposed.

8A-4 Hot Spot Cooling Evaluation Using Closed-Channel Cooling System (C^3S) for MPU 3DI Application

A novel closed-channel cooling system (C^3S) for microprocessor application has been studied. A 0.038 cm^2 micro heaters as small as hot spot block in MPUs are fabricated. Maximum temperature was 350 °C at 28 W/cm^2 of power density. The cooling system enables decreasing temperature more than 30 °C with the liquid flow rate ranged 200 ul/min. It is found that micro bubble in water affects cooling efficiency due to vaporization kinetics. Cooling by water shows higher efficiency than that of IPA. With keeping lower micro bubble concentration of water, the heater temperature at 268 °C decreases to 143 and 63 °C at the flow rates of 100 and 600 ul/min, respectively.

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8B-1 Understanding Short-term BTI Behavior through Comprehensive Observation of Gate-voltage Dependence of RTN in Highly Scaled High-k / Metal-gate pFETs

In this paper, we report the results of extensive RTN trap analysis in high-k / metal-gate pFETs with respect to the response of >1400 traps to gate voltage, and discuss, for the first time, the impact of these results on understanding BTI stress and recovery effects. Our results suggest that the statistical variation in BTI effects in scaled devices may become very large because of the wide range of trap characteristics.

8B-2 Suppression of V_T Variability Degradation Induced by NBTI with RDF Control

V_T variability degradation induced by negative bias temperature instability (NBTI) and its relation with random dopant fluctuation (RDF) is investigated by a special large-scale (16000 PFETs) device matrix array (DMA) TEG exclusive for NBTI variability measurements. It is clarified that V_T variability degradation is suppressed by reducing channel or halo dopant concentration. The suppression me-chanism is discussed in terms of channel potential fluctuation caused by RDF.

8B-3 From Mean Values to Distributions of BTI Lifetime of Deeply Scaled FETs through Atomistic Understanding of the Degradation

Since only a few gate oxide defects are expected in future nm-sized CMOS devices, the well-defined Bias-Temperature-Instability (BTI) lifetime of large devices becomes distributed. This paradigm shift is addressed by demonstrating the methodology to predict the VTH shift distributions after BTI stress: the critical reliability issue in modern CMOS technologies. The sources of time dependent variability are identified through the understanding of the atomistic impact of individual traps.

8B-4 Investigation of the Self-Heating Effect on Hot-Carrier Characteristics for Packaged High Voltage Devices

HVNMOS device degradation due to AC/DC hot carrier injection (HCI) stress between package level (PL) and wafer level (WL) is characterized and their relationship to the power generation is quantified. It is observed that Idlin degradation in PL is worse compared to WL during DC HCI stress due to excessive self-heating (SH) in PL compared to WL. It is also validated that SH mechanism is the dominant factor for I_{dlin} degradation compared to HCI impact ionization during pack-aged HVNMOS HCI stress. A new reliability characterization methodology for HVNMOS is also proposed, which eliminates the PL SH effect and boost up the product safe-operating-area (SOA) capability.

9A-1 Demonstration of Low Temperature 3D Sequential FDSOI Integration down to 50 nm Gate Length

For the first time, 3D sequential integration is demonstrated down to LG=50nm. Molecular bonding is used to design a perfect a top active layer (thickness control, cristallinity) and a low Thermal Budget (TB) top FET (600°C) has been developed for bottom FET preservation. We demonstrate that this integration is viable for bottom and top MOSFETs with advanced LG. Additionally the low TB process compared to its high temperature counterpart translates in worthy advantages in terms of gate stack: 3A EOT decrease, improved insulating properties. We demonstrate also the smallest Inter-Layer-Dielectric (ILD) thickness down to 23 nm, paving the way to ultra dense and robust SRAMs.

9A-2 Impact of Back Bias on Ultra-Thin Body and BOX (UTBB) Devices

We reported a thorough study of the back bias impact on ultra-thin body and BOX (UTBB) devices. The temperature effect, SCE, GIDL and reliability from back bias were explored. V_t modulation from back bias is well maintained across a wide temperature range. Contrary to Bulk, GIDL is reduced from reverse bias in UTBB devices. The impact on aggressively scaled circuits, such as 100nm CPP ROs and 0.08um2 6-T SRAM, was demonstrated for the first time.

9A-3 Stress-induced Performance Enhancement in Si Ultra-Thin Body FD-SOI MOSFETs: Impacts of Scaling

A detailed study of the impact of channel stress on (100)/<110> Ultra-Thin Body and BOX (UT2B) Fully Depleted SOI (FD-SOI) MOSFET performance is presented. Stress-induced mobility enhancement diminishes with Si body thickness scaling below 5nm for electrons but not for holes. Performance enhancement is maintained with gate-length scaling.

Program no. **Title**
Abstract

9A-4 Ultra Thin Buried Nitride Integration for Multi V_T, Low Variability and Power

We highlight an original solution to adjust the threshold voltage of Fully Depleted Silicon-On-Insulator CMOS down to 20nm gate length thanks to charge storage in a thin buried nitride layer. In particular, high performance pMOS with Ioff=500nA/micron (V_T=-0.2V) are demonstrated in a gate first approach. This technique is combined with back-bias for power management and with a smart process compensation technique to improve the device variability down to sigma(V_T)=4mV for L=30nm and W=500nm.

9B-1 Towards 1X DRAM: Improved Leakage 0.4 nm EOT STO-based MIMcap and Explanation of Leakage Reduction Mechanism Showing Further Potential

We report record JG-EOT DRAM MIMcap of 10^{-7} A/cm^2 at 0.40 nm EOT with RuO_x/TiO_x/Sr-rich STO. We explain origin of low JG-EOT. TiO_x reduces EOT on TiN, Ru or RuO_x, but RuO_x is needed for low JG. We measured FLP at STO midgap and same barrier (~1.6 eV) from all BE. Leakage is controlled by similar traps in STO for all stacks and BE, and attribute improvement with RuO_x to local STO trap density reduction.

9B-2 Ultra-Low Leakage Junction Engineering of Cell Transistor by Raised Source/Drain for Logic-Compatible 28-nm Embedded DRAM

An ultra-low leakage junction design concept is proposed for further scaling of cell transistor for logic-compatible eDRAM. Raised source/drain (RSD) enables to introduce graded junction to short-channel FET to reduce junction leakage. Furthermore, the LDD formed by thermal diffusion from phosphorus-doped RSD enables to suppress subthreshold leakage by removing LDD ion implantation that causes extra junction broadening. We demonstrated the cell FET with 0.1-pA off-leakage at 115°C without Ion degradation for fully logic-compatible 28-nm eDRAM.

9B-3 Offset Buried Metal Gate Vertical Floating Body Memory Technology with Excellent Retention Time for DRAM Application

Offset buried metal gate vertical floating body (FB) memory cell technology fabricated on a recess gate DRAM technology is presented. Cell operating window (OW) is improved by 75%, while static and disturb tRET @ 1.3V, T=93C are > 10x better than our previous work [1]. Array measurements and TCAD results confirm that maximum junction electric field (Emax) reduction is the primary reason for tRET improvement.

9B-4 Electronic Global Shutter CMOS Image Sensor Using Oxide Semiconductor FET with Extremely Low Off-state Current

A novel CMOS image sensor including a pixel with a hybrid structure of an oxide semiconductor FET (OS-FET) and Si(SOI)-FETs has been developed. The OS-FET has an extremely low off-state current, and thus can form a highly insulating charge storage node in combination with SOI. We have therefore applied the OS-FET to an electronic global shutter CMOS image sensor and confirmed improvement in imaging quality.

10B-1 Optical Charge-Pumping: A Universal Trap Characterization Technique for Nanoscale Floating Body Devices

A universal trap characterization technique for nanoscale floating body devices is demonstrated. It overcomes the limits of conventional charge pumping. Exploiting optically generated carriers, the interface trap density, the energy distribution of interface traps, and the bulk region trap density are extracted directly without additional fabrication or the use of extra test patterns. The proposed technique can provide a trap analysis tool for a study of reliability regardless of the device structure, material, or dimension.

10B-2 Proposal of a Model for Increased NFET Random Fluctuations

It is shown, using kinetic Monte Carlo simulation, that variability in the amount of point defects created by source/drain (S/D) implantation can significantly increase NFET random fluctuation through the modulation of boron transient enhanced diffusion (TED). This model is consistent with reported NFET fluctuation behavior.

Program no. **Title**
Abstract

10B-3 A Novel and Direct Experimental Observation of the Discrete Dopant Effect in Ultra-Scaled CMOS Devices

For the first time, the channel discrete dopant profiling (DDP) of small devices are demonstrated experi- mentally based on a quasi-2D V_{th} model. The discrete -dopant distribution along the channel direction can be determined. Boron cluster in nMOSFETs was observed, resulting in a larger V_{th} variation, in comparison to that of pMOSFETs. Moreover, experiments have been extended to the advanced strain-CMOS devices. For the SiC S/D nMOSFET, the carbon out-diffusion has been identified; for SiGe S/D pMOSFET, Ge out-diffusion has also been observed. This approach provides a direct-observation of the random dopant fluctuation (RDF) and is useful for studying the V_{th} variability of future generation CMOS devices.

10B-4 Comprehensive Study of Systematic and Random Variation in Gate-Induced Drain Leakage for LSTP Applications

Systematic and random variability of Gate-Induced Drain Leakage (GIDL) current have been studied for the first time. Trap-assisted tunneling current shows more instability than band-to-band tunneling current in every kinds of variations resulting from high sensitivity of the traps to impurities under MOSFET channel.

11A-1 Comprehensive Understanding of Random Telegraph Noise with Physics Based Simulation

Physical modeling of transient and frequency domain noise simulation for random telegraph noise (RTN) is conducted, considering discretized traps and energy transition in insulator. The models are implemented in a 3D device simulator to consider the device structure effect and bias effect universally. Trap density and trap distribution in insulator are predicted quantitatively with comparison of measured data and simulated data. In addition, we present negative pre-pulse effect for RTN reduction.

11A-2 Direct Real-Time Observation of Channel Potential Fluctuation Correlated to Random Telegraph Noise of Drain Current Using Nanowire MOSFETs with Four-Probe Terminals

We have successfully characterized the dynamical fluctuation of electrical potential due to random telegraph noise (RTN) using MOSFETs with extra terminals for potential sensing. Among some cases of potential changes, devices with clear response in the extra terminals were analyzed in detail. It was found RTN can cause the potential fluctuation in the entire channel region. The magnitude of the fluctuation was consistent with those due to Vg in static properties. These results demonstrate the direct observation of channel potential changes due to number fluctuation phenomena.

11A-3 Impact of Random Telegraph Signaling Noise on SRAM Stability

Large-signal bias and temperature dependences of random telegraph signaling (RTS) noise in transistors and their impact on the dynamic stability of 6T SRAM cells are investigated. RTS causes fluctuations in SRAM stability that are dependent on cell access history and trap characteristics. Access patterns for characterizing the worst-case and best-case dynamic stability are developed.

11A-4 A New Approach of NAND Flash Cell Trap Analysis Using RTN Characteristics

We measured RTN characteristics in NAND flash cell array and test structure having 27 nm design rule depending on different program and erase states. From these measured results, we analyzed the trap properties along the active width direction from of NAND flash cell. Using special analysis methods, we verified the validity of this characterization tool and applied it to various processed NAND flash memory cells.

11B-1 Integration of 28nm MJT for 8-16Gb Level MRAM with Full Investigation of Thermal Stability

28nm MTJ for 8-16Gb MRAM device has been successfully integrated with special etch technique. Resistance separation between high and low R states was 15.2, comparable to that for 80nm MTJ cells. Thermal stability factor followed prediction well, and MTJ with free layer of 25A and aspect ratio of 3 showed 56. In order to realize sub-30nm MRAM device, a novel FL with substantially low critical current density needs to be developed.

Program no. **Title**
Abstract

11B-2 Strain-Engineering for High-Performance STT-MRAM

Strain-engineering using the inverse magnetostrictive effect has been performed to improve the performance of STT-MRAM.The thermal stability factor E/k_BT has been enhanced by 40% without increasing a switching current by controlling the process-induced stress in a free layer in MTJ with mechanically engineered manufacturing steps.

11B-3 CoFeB/MgO Based Perpendicular Magnetic Tunnel Junctions with Stepped Structure for Symmetrizing Different Retention Times of "0" and "1" Information

We investigated perpendicular magnetic tunnel junctions (p-MTJs) with a stepped structure for spin-transfer torque random access memory. In conventional p-MTJs, the retention time for storing "1" is shorter than that for storing "0," because of the mangetostatic energy difference between the two states caused by dipole interaction. To counter this, we show, by employing a stepped structure, that the retention time can be made equivalent regardless of the stored information.

11B-4 Highly Reliable 26nm 64Gb MLC E2NAND (Embedded-ECC & Enhanced-efficiency) Flash Memory with MSP (Memory Signal Processing) Controller

A highly reliable 26nm 64GB MLC E2NAND (E2: Embedded-ECC & Enhanced-efficiency) flash memory has been successfully developed. To overcome scaling challenges, novel integration and operation technologies, such as 2-dummy word-line (WL) scheme, depletion suppressing process, hydrogen reducing process and Virtual Negative Read (VNR) scheme are introduced. And also, Memory Signal Processing (MSP) controller is used for enhancing performance and reliability. Finally, 5K cycling and 1 year data retention can be greatly achieved.

12-1 Non-Gaussian Distribution of SRAM Read Current and Design Impact to Low Power Memory Using Voltage Acceleration Method

SRAM read current tail distribution beyond 6 sigma was studied using Voltage Acceleration Method (VAM). For the first time, non-Gaussian distribution of SRAM read current was confirmed with direct measurements on silicon. Data shows that conventional assumption of Gaussian distribution in read current is inaccurate especially at low Vdd and cold temperature conditions for low power memory in 28nm and beyond technology nodes. In 28nm, this inaccuracy would lead to 2x bit access delay penalty.

12-2 Variability and Technology Aware SRAM Product Yield Maximization

This work assesses the impact of process variability such as device mismatch of two in-house FinFET and a planar technology on key figures of merit (SNM and WTP) of SRAMs
- for the first time not only at cell but also at product level. Statistical VCCmin analysis shows that VCC limits for array sizes are 512Kbit at 1V for planar, 2Mbit at 0.9V FOR BFF, and - far ahead - at least 1GBit at 0.7V for undoped SOIFF devices.

12-3 An Ultra Low-Noise MOSFET Device with Improved SNR for DCO-type Applications

An Ultra-Low Noise (ULN) MOSFET device used as a gm-pair in a DCO circuit is presented. Device 1/f noise reduces by >12X while circuit SNR improves by >1.2dB for an optimized process. While strong process correlation for device 1/f noise is seen, a weak correlation at circuit level is noticed. Noise is primarily dependent on halo implant conditions while SNR dispersion is influenced by Fluorine (F) addition. Overall, the ULN device improves SNR yield by ~3% and the optimized circuit-and-device performance is seen for reduced-halo and no-F process condition.

12-4 Bridging Design and Manufacture of Analog/Mixed-Signal Circuits in Advanced CMOS

We present device and circuit characterization resulting from technology/design co-development to improve the design and manufacture of analog/mixed-signal (AMS) circuits in processors. We introduce I_D-based MOSFET transconductance measurements and a new measurement of drain saturation margin at realistic analog biasing. We also describe routinely monitored scribe lane replicas of key AMS passives and circuits. Such measurements enable construction and validation of compact models better suited to AMS needs than those historically tailored for logic design.
