2012 Symposium on VLSI Technology Accepted Papers Listed by Submission Number

The Titles and Author List appear as they were submitted by the author. They will be proofed and corrected for the Proceedings and Final Program.

Submission Number: **6**
Session/Paper Slot Number: **T13-5**
Wednesday, June 13 - 5:05pm
Strain Engineered Extremely Thin SOI (ETSOI) for High-Performance CMOS, Ali Khakifirooz, Kangguo Cheng, Toshiharu Nagumo, Nicolas Loubet, Thomas Adam, Alexander Reznicek, James Kuss, Davood Shahrjerdi, Raghavasimhan Sreenivasan, Shom Ponoth, Hong He, Pranita Kulkarni, Qing Liu, Pouya Hashemi, Prasanna Khare, Scott Luning, Sanjay Mehta, Jocelyne Gimbert, Yu Zhu and Zhengmao Zhu

Submission Number: **12**
Session/Paper Slot Number: **T21-5**
Thursday, June 14 - 5:05pm
InGaSb: single channel solution for realizing III-V CMOS, Ze Yuan, Aneesh Nainani, Archana Kumar, Ximeng Guan, Brian R. Bennett, J. Brad Boos, Mario G. Ancona and Krishna C. Saraswat

Submission Number: **18**
Session/Paper Slot Number: **T14-5**
Wednesday, June 13 - 5:05pm
Sub-fM DNA Sensitivity by Self-Aligned Maskless Thin-Film Transistor-Based SoC Bioelectronics, Min-Cheng Chen, Chang-Hsien Lin, Chia-Yi Lin, Fu-Kuo Hsueh, Wen-Hsien Huang, Yu-Chung Lien, Hsiu-Chih Chen, Hsiao-Ting Hsueh, Che-Wei Huang, Chih-Ting Lin, Yin-Chih Liu, Ta-Hsien Lee, Mu-Yi Hua, Jian-Tai Qiu, Mao-Chen Liu, Yao-Jen Lee, Jia-Min Shieh, ChiaHua Ho, Chenming Hu and Fu-Liang Yang

Submission Number: **19**
Session/Paper Slot Number: **J-T10-4**
Wednesday, June 13 - 11:40am
A Highly Pitch Scalable 3D Vertical Gate (VG) NAND Flash Decoded by a Novel Self-Aligned Independently Controlled Double Gate (IDG) String Select Transistor (SSL), Chih-Ping Chen, Hang-Ting Lue, Kuo-Pin Chang, Yi-Hsuan Hsiao, Chih-Chang Hsieh, Shih-Hong Chen, Yen-Hao Shih, Kuang-Yeu Hsieh, Tahone Yang, Kuang-Chao Chen and Chih-Yuan Lu

Submission Number: **23**
Session/Paper Slot Number: **T13-3**
Wednesday, June 13 - 4:15pm
Impact of Back Biasing on Carrier Transport in Ultra-Thin-Body and BOX (UTBB) Fully Depleted SOI MOSFETs, Nuo Xu, Francois Andrieu, Byron Ho, Bich-Yen Nguyen, Olivier Weber, Carlos Mazure, Olivier Faynot, Thierry Poiroux and Tsu-Jae King Liu

Submission Number: **28**
Session/Paper Slot Number: **T20-3**
Thursday, June 14 - 2:20pm
High-Aspect Ratio Through Silicon Via (TSV) Technology, Hung-Pin Chang, Hsin-Yu Chen, Pei-Ching Kuo, Alton Chien, Ebin Liao, Tzu-Chiun Lin, Jacky Wei, Yung-Chi Lin, Yi-Hsiu Chen, Ku-Feng Yang, Hung-An Teng, Justin Tsai, Cheng-Chieh Hsieh, M.F. CHEN, Yuan-Hong Liou, Tsang-Jiuh Wu, Shang Y. Hou, Wen-Chih Chiou, Shin-Puu Jeng and Chen-Yua Yu

Submission Number: **29**
Session/Paper Slot Number: **J-T12-4**
Wednesday, June 13 - 2:45pm
An ultra-thin interposer utilizing 3D TSV technology, Wen-Chih Chiou, Ku-Feng Yang, Constant Yeh, Shih-Hui Wang, Yuan-Hong Liou, Tsang-Jiuh Wu, Jing-Cheng Lin, Cheng-Chieh Hsieh, Hung-Pin Chang, Jacky Wei, Yung-Chi Lin, Yi-Hsiu Chen, Hung-Jung Tu, Tu-Hao Yu, Po-Hao Tsai, Shang Y. Hou, Da-Yuan Shih, Kim Hong Chen, Shin-Puu Jeng and Chen-Hua Yu

Submission Number: **30**
Session/Paper Slot Number: **T20-4**
Thursday, June 14 - 2:45pm
Demonstration of Inter-chip Data Transmission in a Three-dimensional Stacked Chip Fabricated by Chip-level TSV Integration, Kazuyuki Hozawa, Futoshi Furuta, Yuko Hanaoka, Mayu Aoki, Kenichi Osada, Kenichi Takeda, Kang Wook Lee, Takafumi Fukushima and Mitsumasa Koyanagi

Submission Number: **33**
Session/Paper Slot Number: **T4-3**
Tuesday, June 12 - 2:20pm
Dramatic Improvement of high-K Gate Dielectric Reliability by Replacing Metal Gate Electrode with Mono-Layer Graphene, Jong Kyung Park, Seung Min Song, Jeong Hun Mun and Byung Jin Cho

Submission Number: **34**
Session/Paper Slot Number: **T18-2**
Thursday, June 14 - 10:25am
Multi-Layer Sidewall WOX Resistive Memory Suitable for 3D ReRAM, W.C. Chien, F.M. Lee, Y.Y. Lin, M.H. Lee, S.H. Chen, C.C. Hsieh, E.K. Lai, H.H. Hui, Y.K. Huang, C.C. Yu, C.F. Chen, H.L. Lung, K.Y. Hsieh and Chih-Yuan Lu

Submission Number: **36**
Session/Paper Slot Number: **T7-1**
Tuesday, June 12 - 3:25pm
Enhancement of data retention and write current scaling for sub-20nm STT-MRAM by utilizing dual interfaces for perpendicular magnetic anisotropy, Jeong-Heon Park, Younghyun Kim, Woochang Lim, Jaehoon Kim, Sanghwan Park, Juhyun Kim, Woojin Kim, Kiwoong Kim, Junho Jeong, Sechung Oh, Jang Eun Lee, Soon Oh Park, Steven Watts, Dmytro Apalkov, Vladimir Nikitin, Mohamad Krounbi, Sangsup Jeong, Siyoung Choi, Hokyu Kang and Chilhee Chung

Submission Number: **38**
Session/Paper Slot Number: **T5-1**
Tuesday, June 12 - 1:30pm
Scalable 3-D vertical chain-cell-type phase-change memory with 4F2 poly-Si diodes, Masaharu Kinoshita, Yoshitaka Sasago, Hiroyuki Minemura, Yumiko Anzai, Mitsuharu Tai, Yoshihisa Fujisaki, Shuichi Kusaba, Tadao Morimoto, Takashi Takahama, Toshiyuki Mine, Akio Shima, Yoshiki Yonamoto and Takashi Kobayashi

Submission Number: **40**
Session/Paper Slot Number: **T3-4**
Tuesday, June 12 - 11:40am
Ferroelectricity in HfO2 enables nonvolatile data storage in 28 nm HKMG, Johannes Müller, Ekaterina Yurchuk, Till Schlösser, Jan Paul, Raik Hoffmann, Stefan Müller, Dominik Martin, Stefan Slesazeck, Patrick Polakowski, Jonas Sundqvist, Malte Czernohorsky, Konrad Seidel, Peter Kücher, Roman Boschke, Martin Trentzsch, Klaus Gebauer, Uwe Schröder and Thomas Mikolajick

Submission Number: **43**
Session/Paper Slot Number: **T14-4**
Wednesday, June 13 - 4:40pm
High Performance Bilayer Oxide Transistor for Gate Driver Circuitry Implemented on Power Electronic Devices, Sanghun Jeon, Hojung Kim, Hyunsik Choi, Ihun Song, Seung-Eon Ahn, Chang Jung Kim, Jaikwang Shin, U-In Chung, Inkyung Yoo and Kinam Kim

Submission Number: **46**
Session/Paper Slot Number: **T9-1**
Wednesday, June 13 - 10:25am
Atom Probe Tomography for 3D-Dopant Analysis in FinFET Devices, Ajay Kumar Kambham, Gerd Zschaetzsch, Yuichiro Sasaki, Mitsuhiro Togo, Naoto Horiguchi, Jay Mody, Antonios Florakis, Durga Rao Gajula, Arul Kumar, Matthieu Gilbert and Wilfried Vandervorst

Submission Number: **48**
Session/Paper Slot Number: **T8-1**
Wednesday, June 13 - 8:05am
A Novel Cross Point One-Resistor (0T1R) Conductive Bridge Random Access Memory (CBRAM) with Ultra Low Set/Reset Operation Current, F.M. Lee, Y.Y. Lin, M.H. Lee, W.C. Chien, H.L. Lung, K.Y. Hsieh and C.Y. Lu

Submission Number: **49**
Session/Paper Slot Number: **J-C6-4**
Wednesday, June 13 - 4:40pm
A Simple New Write Scheme for Low Latency Operation of Phase Change Memory, Yu-Yu Lin, Yi-Chou Chen, Feng-Ming Lee, Matthew BrightSky, Hsiang-Lan Lung and Chung Lam

Submission Number: **50**
Session/Paper Slot Number: **T7-5**
Tuesday, June 12 - 5:05pm
Highly Scalable STT-MRAM with 3-Dimensional Cell Structure using In-plane Magnetic Anisotropy Materials, Sungchul Lee, Kwangseok Kim, Keewon Kim, Unghwan Pi, U-In Chung, Inkyung Yoo and Kinam Kim

Submission Number: **51**
Session/Paper Slot Number: **T8-3**
Wednesday, June 13 - 8:55am
Multi-level Switching of Triple-layered TaOx RRAM with Excellent Reliability for Storage Class Memory, Seung Ryul Lee, Young-Bae Kim, Man Chang, Kyung Min Kim, Chang Bum Lee, Ji Hyun Hur, Gyeong-Su Park, Dongsoo Lee, Myoung-Jae Lee, Chang Jung Kim, U-In Chung, In-Kyeong Yoo and Kinam Kim

Submission Number: **53**
Session/Paper Slot Number: **T18-1**
Thursday, June 14 - 10:00am
Integration of 4F2 Selector-less Crossbar Array 2Mb ReRAM Based on Transition Metal Oxides for High Density Memory Applications, Hyung Dong Lee and Soo Gil Kim

Submission Number: **57**
Session/Paper Slot Number: **T3-2**
Tuesday, June 12 - 10:50am
Intrinsic Fluctuations in Vertical NAND Flash Memories, Etienne Nowak, Jae-Ho Kim, HyeYoung Kwon, Young-Gu Kim, Jae Sung Sim, Seung-Hyun Lim, Dae Sin Kim, Keun-Ho Lee, Young-Kwan Park, Jeong-Hyuk Choi and Chilhee Chung

Submission Number: **59**
Session/Paper Slot Number: **T5-2**
Tuesday, June 12 - 1:55pm
Varistor-type Bidirectional Switch (JMAX>107A/cm2, Selectivity~104) for 3D Bipolar Resistive Memory Arrays, Wootae Lee, Jubong Park, Jungho Shin, Jiyong Woo, Seonghyun Kim, Godeuni Choi, Seungjae Jung, Sangsu Park, Daeseok Lee, Euijun Cha, Hyung Dong Lee, Soo Gil Kim, Suock Chung and Hyunsang Hwang

Submission Number: **61**
Session/Paper Slot Number: **T3-1**
Tuesday, June 12 - 10:25am
A New Metal Control Gate Last Process (MCGL process) for High Performance DC-SF (Dual Control gate with Surrounding Floating gate) 3D NAND Flash Memory, Yoohyun Noh, Youngsoo Ahn, Hyunseung Yoo, Byeongil Han, Sungjae Chung, Keonsoo Shim, Keunwoo Lee, Sanghyon kwak, Sungchul Shin, Iksoo Choi, Sanghyuk Nam, Gyuseog Cho, Dongsun Sheen, Seungho Pyi, Jongmoo Choi, Sungkye Park, Jinwoong Kim, Seokkiu Lee, Seiichi Aritome and Sungjoo Hong

Submission Number: **64**
Session/Paper Slot Number: **T16-2**
Thursday, June 14 - 8:30am
New Insights into AC RTN in Scaled High-k/Metal-gate MOSFETs under Digital Circuit Operations, Jibin Zou, Runsheng Wang, Nanbo Gong, Ru Huang, Xiaoqing Xu, Jiaojiao Ou, Changze Liu, Jianping Wang, Jinhua Liu, Jingang Wu, Shaofeng Yu, Pengpeng Ren, Hanming Wu, Shiuh-Wuu Lee and Yangyuan Wang

Submission Number: **76**
Session/Paper Slot Number: **T22-3**
Thursday, June 14 - 4:15pm
Accurate Chip Leakage Prediction: Challenges and Solutions, Xiaojun Yu, Jie Deng, Sim Loo, Kevin Dezfulian, Susan Lichtensteiger, Jeanne Bickford, Nazmul Habib, Paul Chang, Anda Mocuta and Ken Rim

Submission Number: **78**
Session/Paper Slot Number: **T19-4**
Thursday, June 14 - 2:45pm
Segmented-Channel Si(1-x)Ge(x)/Si pMOSFET for Improved ION and Reduced Variability, Byron Ho, Nuo Xu, Bingxi Wood, Vinh Tran, Saurabh Chopra, Yihwan Kim, Bich-Yen Nguyen, Olivier Bonnin, Carlos Mazure, Satheesh Kuppurao, Chorng-Ping Chang and Tsu-Jae King Liu

Submission Number: **82**
Session/Paper Slot Number: **T18-3**
Thursday, June 14 - 10:50am
Ultrathin (<10nm) Nb2O5/NbO2 Hybrid Memory with Both Memory and Selector Characteristics for High Density 3D Vertically Stackable RRAM Applications, Seonghyun Kim, Xinjun Liu, Jubong Park, Seungjae Jung, Wootae Lee, Jiyong Woo, Jungho Shin, Godeuni Choi, Chumhum Cho, Sangsu Park, Daeseok Lee, Eui-jun Cha, Byoung-Hun Lee, Hyung Dong Lee, Soo Gil Kim, Suock Jung and Hyunsang Hwang

Submission Number: **90**
Session/Paper Slot Number: **T16-1**
Thursday, June 14 - 8:05am
Voltage and Temperature Dependence of Random Telegraph Noise in Highly Scaled HKMG ETSOI nFETs and its Impact on Logic Delay Uncertainty, Hiroshi Miki, Masanao Yamaoka, David J. Frank, Kangguo Cheng, Dae-Gyu Park, Effendi Leobandung and Kazuyoshi Torii

Submission Number: **95**
Session/Paper Slot Number: **T6-5**
Tuesday, June 12 - 5:05pm
Demonstration of Improved Heteroepitaxy, Scaled Gate Stack and Reduced Interface States Enabling Staggered Heterojunction Tunnel FETs with Highest Drive Current and On-Off Ratio, Dheeraj Mohata, Bijesh Rajamohanan, Yan Zhu, Mantu Hudait, Richard Southwick, Zakariae Chbili, David Gundlach, John Suehle, Joel Fastenau, Dmitri Loubychev, Amy Liu, Theresa Mayer, Vijay Narayanan and Suman Datta

Submission Number: **96**
Session/Paper Slot Number: **T5-3**
Tuesday, June 12 - 2:20pm
Nonvolatile 32x32 Crossbar Atom Switch Block Integrated on a 65 nm CMOS Platform, Naoki Banno, Munehiro Tada, Toshitsugu Sakamoto, Koichiro Okamoto, Makoto Miyamura, Noriyuki Iguchi, Tatsuhiko Nohisa and Hiromitsu Hada

Submission Number: **97**
Session/Paper Slot Number: **T22-2**
Thursday, June 14 - 3:50pm
The Understanding of the Trap Induced Variation in Bulk Tri-gate Devices by a Novel Random Trap Profiling (RTP) Technique, HM Tsai, ER Hsieh, Steve S Chung, CH Tsai, RM Huang, CT Tsai and CW Liang

Submission Number: **102**
Session/Paper Slot Number: **T9-4**
Wednesday, June 13 - 11:40am
ZnO: an attractive option for n-type metal-interfacial layer-semiconductor (Si, Ge, SiC) contacts, Prashanth Paramahans Manik, Shashank Gupta, Ravi kesh Mishra, Nitai Agarwal, Aneesh Nainani, Yi-Chiau Huang, Mathew Abraham, Udayan Ganguly and Saurabh Lodha

Submission Number: **105**
Session/Paper Slot Number: **T3-3**
Tuesday, June 12 - 11:15am
A New GIDL Phenomenon by Field Effect of Neighboring Cell Transistors and Its Control Solutions in Sub-30 nm NAND Flash Devices, Il Han PARK, Wook-Ghee Hahn, Ki-Whan Song, Ki Hwan Choi, Hyun-Ki Choi, Sung Bok Lee, Chang-Sub Lee, Jai Hyuk Song, Jin Man Han, Kye Hyun Kyoung and Young-Hyun Jun

Submission Number: **110**
Session/Paper Slot Number: **T15-4**
Thursday, June 14 - 9:20am
Advanced modeling and optimization of high performance 32nm HKMG SOI CMOS for RF/analog SoC applications, Sungjae Lee, Jim Johnson, Brian Greene, Anthony Chou, Kai Zhao, Murshed Chowdhury, Jang Sim, Arvind Kumar, Daeik Kim, Akil Sutton, Suk Hoon Ku, Yue Liang, Yanfeng Wang, Dustin Slisher, Kevin Duncan, Paul Hyde, Rainer Thoma, Jie Deng, Yanqing Deng and Rajvi Rupani

Submission Number: **113**
Session/Paper Slot Number: **T11-2**
Wednesday, June 13 - 1:55pm
GeSn Channel nMOSFETs: Material Potential and Technological Outlook, Suyog Gupta, Benjamin Vincent, Dennis Lin, Marika Gunji, Andrea Firrincieli, Federica Gencarelli, Blanka Magyari-Köpe, Bin Yang, Bastien Douhard, Joris Delmotte, Alexis Franquet, Matty Caymax, Johan Dekoster, Yoshio Nishi and Krishna Saraswat

Submission Number: **117**
Session/Paper Slot Number: **T8-4**
Wednesday, June 13 - 9:20am
Conductive Filament Scaling of TaOx Bipolar ReRAM for Long Retention with Low Current Operation, Takeki Ninomiya, Takeshi Takagi, Zhiqiang Wei, Shunsaku Muraoka, Ryutaro Yasuhara, Koji Katayama, Yuuichirou Ikeda, Ken Kawai, Yoshikazu Kato, Yoshio Kawashima, Satoru Ito, Takumi Mikawa, Kazuhiko Shimakawa and Kunitoshi Aono

Submission Number: **119**
Session/Paper Slot Number: **T02-1**
Tuesday, June 12 - 10:25am
10nm-Diameter Tri-Gate Silicon Nanowire MOSFETs with Enhanced High-Field Transport and Vth Tunability through Thin BOX, Masumi Saitoh, Kensuke Ota, Chika Tanaka, Ken Uchida and Toshinori Numata

Submission Number: **123**
Session/Paper Slot Number: **T7-3**
Tuesday, June 12 - 4:15pm
High-speed and reliable domain wall motion device: Material design for embedded memory and logic application, Shunsuke Fukami

Submission Number: **130**
Session/Paper Slot Number: **J-C6-5**
Wednesday, June 13 - 5:05pm
Analysis of Random Telegraph Noise and Low Frequency Noise Properties in 3-D Stacked NAND Flash Memory with Tube-Type Poly-Si Channel Structure, Min-Kyu Jeong, Sung-Min Joe, Chang-Su Seo, Kyung-Rok Han, Eunseok Choi, Sung-Kye Park and Jong-Ho Lee

Submission Number: **132**
Session/Paper Slot Number: **T7-4**
Tuesday, June 12 - 4:40pm
Spintronics Primitive Gate with High Error Correction Efficiency 6 (Perror)^2 for Logic-in Memory Architecture, Yukihide Tsuji, Ryusuke Nebashi, Noboru Sakimura, Ayuka Morioka, Hiroaki Honjo, Koiichi Tokutome, Sadahiko Miura, Tetsuhiro Suzuki, Shunsuke Fukami, Keizo Kinoshita, Takahiro Hanyu, Tetsuo Endo, Naoki Kasai, Hideo Ohno and Tadahiko Sugibayashi

Submission Number: **134**
Session/Paper Slot Number: **T14-3**
Wednesday, June 13 - 4:15pm
Operation of Functional Circuit Elements using BEOL-Transistor with InGaZnO Channel for On-chip High/Low Voltage Bridging I/Os and High-Current Switches, Kishou Kaneko, Hiroshi Sunamura, Mitsuru Narihiro, Shinobu Saito, Naoya Furutake, Masami Hane and Yoshihiro Hayashi

Submission Number: **140**
Session/Paper Slot Number: **T4-1**
Tuesday, June 12 - 1:30pm
Implementing cubic-phase HfO2 with k-value ~ 30 in low-VT replacement gate pMOS devices for improved EOT-Scaling and reliability, Lars-Åke Ragnarsson, Christoph Adelmann, Yuichi Higuchi, Karl Opsomer, Anabela Veloso, Soon Aik Chew, Erika Röhr, Emma Vecchio, Xiaoping Shi, Katia Devriendt, Farid Sebaai, Thomas Kauerauf, Malgorzata Pawlak, Tom Schram, Sven Van Elshocht, Naoto Horiguchi and Aaron Thean

Submission Number: **141**
Session/Paper Slot Number: **T13-1**
Wednesday, June 13 - 3:25pm
Poly/High-k/SiON Gate Stack and Novel Profile Engineering Dedicated for Ultralow-Voltage Silicon-on-Thin-BOX (SOTB) CMOS Operation, Yoshiki Yamamoto, Hideki Makiyama, Takaaki Tsunomura, Toshiaki Iwamatsu, Hidekazu Oda, Nobuyuki Sugii, Yasuo Yamaguchi, Tomoko Mizutani and Toshiro Hiramoto

Submission Number: **142**
Session/Paper Slot Number: **T19-2**
Thursday, June 14 - 1:55pm
85nm-Wide 1.5mA/um-ION IFQW SiGe-pFET: Raised vs Embedded Si75%Ge25% S/D Benchmarking and In-Depth Hole Transport Study, Jerome Mitard, Liesbeth Witters, Geert Eneman, Geert Hellings, Luigi Pantisano, Andriy Hikavyy, Roger Loo, Pierre Eyben, Naoto Horiguchi and Aaron Thean

Submission Number: **143**
Session/Paper Slot Number: **T13-2**
Wednesday, June 13 - 3:50pm
Efficiency of Mechanical Stressors in Planar FDSOI n and p MOSFETs down to 14nm Gate Length, Siméon Morvan, François Andrieu, Mikael Cassé, Olivier Weber, Nuo Xu, Pierre Perreau, Jean-Michel Hartmann, Jean-Charles Barbé, Jérôme Mazurier, Phuong Nguyen, Claire Fenouillet-Bérangee, Claude Tabone, Lucie Tosti, Laurent Brévard, Alain Toffoli, Dominique Lafond, Bich-Yen Nguyen, Gérard Ghibaudo, Olivier Faynot and Thierry Poiroux

Submission Number: **144**
Session/Paper Slot Number: **T02-4**
Tuesday, June 12 - 11:40am
FinFET Parasitic Resistance Reduction by Segregating Shallow Sb, Ge and As Implants at the Silicide Interface, Crystal Kenney, Kah-Wee Ang, Ken Matthews, Max Liehr, Matt Minakais, Martin Rodgers, Vidya Kaushik, Steve Novak, Steve Gausepohl, Chris Hobbs, Paul Kirsch and Raj Jammy

Submission Number: **147**
Session/Paper Slot Number: **T13-4**
Wednesday, June 13 - 4:40pm
Enhancement of Devices Performance of hybrid FDSOI/Bulk Technology by using UTBOX sSOI substrates, Claire Fenouillet-Beranger, Pierre Perreau, Olivier Weber, Imed Ben-Akkez, Antoine Cros, Aurelie Bajolet, Sebastien Haendler, Pascal Fonteneau, Pascal Gouraud, Emmanuel Richard, Francesco Abbate, David Barge, Nicolas Planes, Walter Schwarzenbach, Francois Andrieu, Thierry Poiroux, Dominique Golanski, Olivier Faynot, Michel Haond and Frederic Boeuf

Submission Number: **148**
Session/Paper Slot Number: **T21-1**
Thursday, June 14 - 3:25pm
Sub-60 nm Deeply-Scaled Channel Length Extremely-thin Body In_xGa_{1-x}As-On-Insulator MOSFETs on a Si with Ni-InGaAs Metal S/D and MOS Interface Buffer Engineering, SangHyeon Kim, Masafumi Yokoyama, Noriyuki Taoka, Ryosho Nakane, Tetsuji Yasuda, Osamu Ichikawa, Noboru Fukuhara, Masahiko Hata, Mitsuru Takenaka and Shinichi Takagi

Submission Number: **149**
Session/Paper Slot Number: **T6-4**
Tuesday, June 12 - 4:40pm
Strained Tunnel FETs with record Ion:First demonstration of ETSOI TFETs with SiGe channel and RSD, Anthony Villalon, Cyrille Le Royer, Mikaël Cassé, David Cooper, Bernard Prévitali, Claude Tabone, Jean-Michel Hartmann, Pierre Perreau, Pierrette Rivallin, Jean-François Damlencourt, Fabienne Allain, François Andrieu, Olivier Weber, Olivier Faynot and Thierry Poiroux

Submission Number: **150**
Session/Paper Slot Number: **T19-1**
Thursday, June 14 - 1:30pm
High Mobility Ge pMOSFETs with 0.7 nm Ultrathin EOT using HfO2/Al2O3/GeOx/Ge Gate Stacks Fabricated by Plasma Post Oxidation, Rui Zhang, Po-Chin Huang, Noriyuki Taoka, Mitsuru Takenaka and Shinichi Takagi

Submission Number: **151**
Session/Paper Slot Number: **T4-2**
Tuesday, June 12 - 1:55pm
A Novel Low Resistance Gate Fill for Extreme Gate Length Scaling at 20nm and Beyond for Gate-Last High-k/Metal Gate CMOS Technology, Unoh Kwon, Keith Wong, Siddarth Krishnan, Laertis Economikos, Xing Zhang, Claude Ortolland, Liem Do Thanh, Jean-Baptiste Laloe, Jing Yan Huang, Lisa Edge, Huey Ming Wang, Michael Gribelyuk, David Rath, Raphael Bingert, Yanxiang Liu, Ruqiang Bao, Ilryong Kim, Ravikumar Ramachandran, Wing Lai and Michael Chudzik

Submission Number: **154**
Session/Paper Slot Number: **T4-4**
Tuesday, June 12 - 2:45pm
Process control & Integration options of RMG Technology for aggressively scaled devices, Anabela Veloso, Y. Higuchi, S. Chew, K. Devriendt, L. Ragnarsson, F. Sebaai, T. Schram, S. Brus, E. Vecchio, K. Kellens, G. Eneman, E. Simoen, M. Cho, V. Paraschiv, Y. Crabbe, H. Bender, A. Phatak, W. Yoo, A. Thean and N. Horiguchi

Submission Number: **156**
Session/Paper Slot Number: **T11-3**
Wednesday, June 13 - 2:20pm
Strained Germanium-Tin (GeSn) N-channel MOSFETs featuring Low Temperature N+/P Junction Formation and GeSnO2 Interfacial Layer, Genquan Han, Shaojian Su, Lanxiang Wang, Wei Wang, Xiao Gong, Yue Yang, Pengfei Guo, Cheng Guo, Guangze Zhang, Jisheng Pan, Zheng Zhang, Chunlai Xue, Buwen Cheng and Yee-Chia Yeo

Submission Number: **159**
Session/Paper Slot Number: **T02-2**
Tuesday, June 12 - 10:50am
Strain-Induced Performance Enhancement of Tri-Gate and Omega-Gate Nanowire FETs Scaled Down to 10nm Width, Remi coquand, Mikael cassé, sylvain barraud, pierre leroux, david cooper, christian vizioz, christine comboroure, pierre perreau, virginie maffini-alvaro, claude tabone, lucie tostie, sebastien barnola, vincent delaye, gilles reimbold, gerard ghibaudo, daniela munteanu, stephane monfray, frederic boeuf, olivier faynot and thierry poiroux

Submission Number: **160**
Session/Paper Slot Number: **T18-4**
Thursday, June 14 - 11:15am
Process-improved RRAM cell performance and reliability and paving the way for manufacturability and scalability for high density memory application, Gouri Sankar Kar, Andrea Fantini, Yang Yin Chen, Vasile Paraschiv, Bogdan Govorean, Hubert Hody, Nico Jossart, Hilde Tielens, Stephan Brus, Olivier Richard, Tom Vandeweyer, Dirk Wouters, Laith Altimime and Malgorzata Jurczak

Submission Number: **162**
Session/Paper Slot Number: **T21-2**
Thursday, June 14 - 3:50pm
InAs Quantum-Well MOSFET (Lg = 100 nm) with Record High gm, fT and fmax, Tae-Woo Kim, Richard Hill, Chris Hobbs, Paul Kirsch and Raj Jammy

Submission Number: **164**
Session/Paper Slot Number: **T9-2**
Wednesday, June 13 - 10:50am
A 32nm High-K and Metal-Gate Anti-Fuse Array Featuring a 1.01um2 1T1C Bit Cell, Sarvesh Kulkarni, Sangwoo Pae, Zhanping Chen, Walid Hafez, Brian Pedersen, Anisur Rahman, Tom Tong, Uddalak Bhattacharya, Chia-Hong Jan and Kevin Zhang

Submission Number: **165**
Session/Paper Slot Number: **T20-1**
Thursday, June 14 - 1:30pm
Ultrafast Parallel Reconfiguration of 3D-Stacked Reconfigurable Spin Logic Chip with On-chip SPRAM (SPin-transfer torque RAM), Tetsu Tanaka, Hisashi Kino, Ryuta Nakazawa, Kouji Kiyoyama, Hideo Ohno and Mitsumasa Koyanagi

Submission Number: **166**
Session/Paper Slot Number: **T11-1**
Wednesday, June 13 - 1:30pm
A New Liner Stressor (GeTe) featuring Stress Enhancement due to Very Large Phase-Change Induced Volume Contraction for p-Channel FinFETs, Ran Cheng, Yinjie Ding, Shao Ming Koh, Ashivini Gyanathan, Fan Bai, Bin Liu and Yee-Chia Yeo

Submission Number: **168**
Session/Paper Slot Number: **T8-2**
Wednesday, June 13 - 8:30am
Field-driven ultrafast sub-ns programming in W\Al2O3\Ti\CuTe-based 1T1R CBRAM system, Ludovic Goux, K Sankaran, G Kar, N Jossart, K Opsomer, R Degraeve, G Pourtois, G-M Rignanese, C Detavernier, S Clima, Y-Y Chen, A Fantini, B Govoreanu, D.J. Wouters, M Jurczak, L Altimime and J Kittl

Submission Number: **170**
Session/Paper Slot Number: **T02-3**
Tuesday, June 12 - 11:15am
Channel Doping Impact on FinFETs for 22nm and Beyond, Chung-Hsun Lin, Rama Kambhampati, Robert Miller, Terence Hook, Andres Bryant, Wilfried Haensch, Philip Oldiges, Isaac Lauer, Tenko Yamashita, Veeraraghavan Basker, Theodorus Standaert, Kern Rim, Effendi Leobandung, Huiming Bu and Mukesh Khare

Submission Number: **174**
Session/Paper Slot Number: **T18-5**
Thursday, June 14 - 11:40am
Ultralow sub-500nA operating current high-performance TiN\Al2O3\HfO2\Hf\TiN bipolar RRAM achieved through understanding-based stack-engineering, Ludovic Goux, A Fantini, G Kar, Y-Y Chen, N Jossart, R Degraeve, S Clima, B Govoreanu, G Lorenzo, G Pourtois, D.J. Wouters, J.A. Kittl, L Altimime and M Jurczak

Submission Number: **177**
Session/Paper Slot Number: **T15-3**
Thursday, June 14 - 8:55am
28nm FDSOI Technology Platform for High-Speed Low-Voltage Digital Applications, Nicolas PLANES, Olivier WEBER, Vincent BARRAL, Sebastien HAENDLER, Daniel NOBLET, Damien CROAIN, Mathilde BOCAT, Pierre-Olivier SASSOULAS, Xavier FEDERSPIEL, Antoine CROS, Aurelie BAJOLET, Emmanuel RICHARD, Benjamin DUMONT, Pierre PERREAU, David PETIT, Dominique GOLANSKI, Claire FENOUILLET-BERANGER, Nelly GUILLOT, Mustapha RAFIK and Vincent HUARD

Submission Number: **179**
Session/Paper Slot Number: **T21-3**
Thursday, June 14 - 4:15pm
Antimonide NMOSFET with Source Side Injection Velocity of 2.7x10^7 cm/s for Low Power High Performance Logic Applications, Ashkar Ali, Himanshu Madan, Michael Barth, Matthew Hollander, Brad Boos, Brian Bennett and Suman Datta

Submission Number: **183**
Session/Paper Slot Number: **T14-2**
Wednesday, June 13 - 3:50pm
Graphene Interconnect Lifetime under High Current Stress, Xiangyu Chen, David Seo, Sunae Seo, Hyunjong Chung and H.-S. Philip Wong

Submission Number: **185**
Session/Paper Slot Number: **T15-2**
Thursday, June 14 - 8:30am
A 22nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors, Chris Auth, C Allen, A Blattner, D Bergstrom, M Brazier, M Bost, M Buehler, V Chikarmane, T Glassman, R Grover, W Han, D Hanken, M Hattendorf, P Hentges, R Heussner, J Hicks, D Ingerly, P Jain, S Jaloviar and R James

Submission Number: **192**
Session/Paper Slot Number: **T21-4**
Thursday, June 14 - 4:40pm
Understanding the Feasibility of Scaled III-V TFET for Logic By Bridging Atomistic Simulations and Experimental Results, Uygar E. Avci, Sayed Hasan, Dmitri E. Nikonov, Rafael Rios, Kelin Kuhn and Ian A. Young

Submission Number: **194**
Session/Paper Slot Number: **T5-4**
Tuesday, June 12 - 2:45pm
Large-scale (512kbit) integration of Multilayer-ready Access-Devices based on Mixed-Ionic-Electronic-Conduction (MIEC) at 100% yield, Geoffrey W. Burr, Kumar Virwani, Rohit S. Shenoy, Alvaro Padilla, Matthew BrightSky, Eric A. Joseph, Michael Lofaro, Andrew J. Kellock, Robin S. King, Khanh Nguyen, Amy N. Bowers, Mark Jurich, Charles T. Rettner, Bryan Jackson, Donald S. Bethune, Robert M. Shelby, Teya Topuria, Noel Arellano, Bulent N. Kurdi and Kailash Gopalakrishnan

Submission Number: **196**
Session/Paper Slot Number: **T22-1**
Thursday, June 14 - 3:25pm
Threshold Voltage and DIBL variability modeling for SRAM and Analog MOSFETs, Nattapol Damrongplasit, Luis Zamudio and Sriram Balasubramanian

Submission Number: **198**
Session/Paper Slot Number: **T11-4**
Wednesday, June 13 - 2:45pm
Towards High Performance Ge1-xSnx and In0.7Ga0.3As CMOS: A Novel Common Gate Stack featuring Sub-400 ºC Si2H6 Passivation, Single TaN Metal Gate, and Sub-1.3 nm EOT, Xiao Gong, Shaojian Su, Bin Liu, Lanxiang Wang, Wei Wang, Yue Yang, Eugene Kong, Buwen Cheng, Genquan Han and Yee Chia Yeo

Submission Number: **199**
Session/Paper Slot Number: **T16-4**
Thursday, June 14 - 9:20am
Continuous characterization of MOSFET from low-frequency noise to thermal noise using a novel measurement system up to 100 MHz, Kenji Ohmori, Ryu Hasunuma, Wei Feng and Keisaku Yamada

Submission Number: **208**
Session/Paper Slot Number: **T9-3**
Wednesday, June 13 - 11:15am
Replacement Metal Gate Extendible to 11 nm Technology, Naomi Yoshida, Xinyu Fu, Kun Xu, Yu Lei, Haichun Yang, Shiyu Sun, Hao Chen, Andrew Darlak, Ray Donohoe, Christopher Lazik, Rajkumar Jakkaraju, Atif Noori, Steven Hung, Igor Peidous, Chrong-Ping Chang and Adam Brand

Submission Number: **211**
Session/Paper Slot Number: **T15-1**
Thursday, June 14 - 8:05am
High Performance Bulk Planar 20nm CMOS Technology for Low Power Mobile Applications, Huiling Shang

Submission Number: **214**
Session/Paper Slot Number: **T7-2**
Tuesday, June 12 - 3:50pm
Demonstration of Non-volatile Working Memory through Interface Engineering in STT-MRAM, Chikako Yoshida, Takao Ochiai, Yoshihisa Iba, Yuichi Yamazaki, Koji Tsunoda, Atsushi Takahashi and Toshihiro Sugii

Submission Number: **216**
Session/Paper Slot Number: **T19-3**
Thursday, June 14 - 2:20pm
High-mobility and Low-parasitic Resistance Characteristics in Strained Ge Nanowire pMOSFETs with Metal Source/Drain Structure Formed by Doping-free Processes, Keiji Ikeda, Mizuki Ono, Daisuke Kosemura, Koji Usuda, Minoru Oda, Yuuichi Kamimuta, Toshifumi Irisawa, Yoshihiko Moriyama, Atsushi Ogura and Tsutomu Tezuka

Submission Number: **217**
Session/Paper Slot Number: **T8-5**
Wednesday, June 13 - 9:45am
Dynamic 'Hour Glass' Model for SET and RESET in HfO2 RRAM, Robin Degraeve, Andrea Fantini, Sergiu Clima, Bogdan Govoreanu, Ludovic Goux, Yang Yin Chen, Dirk Wouters, Philippe Roussel, Gouri Sankar Kar, Geoffrey Pourtois, Stefan Cosemans, Jorge Kittle, Laith Altimime, Guido Groeseneken and Malgorzata Jurczak

Submission Number: **218**
Session/Paper Slot Number: **T16-3**
Thursday, June 14 - 8:55am
Comprehensive Investigations on Neutral and Attractive Traps in Random Telegraph Signal Noise Phenomena using (100)- and (110)-Orientated CMOSFETs, Jiezhi Chen, Izumi Hirano, Kosuke Tatsumura and Yuuichiro Mitani

Submission Number: **224**
Session/Paper Slot Number: **T14-1**
Wednesday, June 13 - 3:25pm
A Novel Chemically, Thermally and Electrically Robust Cu Interconnect Structure with an Organic Non-porous Ultralow-k Dielectric Fluorocarbon (k=2.2), Xun Gu, Akinobu Teramoto, Rihito Kuroda, Yugo Tomita, Takenao Nemoto, Shin-ichiro Kuroki, Shigetoshi Sugawa and Tadahiro Ohmi

Submission Number: **227**
Session/Paper Slot Number: **T20-2**
Thursday, June 14 - 1:55pm
Development of Ultra-Thin Chip-on-Wafer Process using Bumpless Interconnects for Three-Dimensional Memory/Logic Applications, Nobuhide Maeda, Hideki Kitada, Koji Fujimoto, Yougsuk Kim, Shoichi Kodama, Seiichi Yoshimi, Miyuki Akazawa, Yoriko Mizushima and Takayuki Ohba