FIRST ANNOUNCEMENT AND CALL FOR PAPERS

2012 SYMPOSIUM ON VLSI TECHNOLOGY

Hilton Hawaiian Village, Honolulu, Hawaii

June 12 - 14, 2012

Sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics
in cooperation with the IEEE Solid State Circuits Society

The 2012 Symposium on VLSI Technology welcomes the submission of original papers on all aspects of IC technology. The 2012 Symposium on VLSI Circuits (please see the reverse side) will be held at the same location, with two days of overlap, to facilitate synergistic interactions among participants in areas of joint interest. **A single registration fee allows participants to attend both of the Symposia.**

CONFERENCE SCOPE

The scope of the Symposium on VLSI Technology includes innovations and advances in the following areas:

- **New concepts and breakthroughs in VLSI processes and devices** for Memory, Logic, I/O, and I/F
- **Advanced gate stacks and interconnects** in VLSI processes and devices
- **Advanced lithography and fine-patterning** technologies for high-density VLSI
- **New functional devices** beyond CMOS with a path for VLSI implementation
- **Packaging of VLSI devices** including 3D-system integration
- **Advanced device analysis, materials and modeling** for VLSIs
- **Reliability** related to the above devices
- **Theory and fundamentals** related to the above devices
- **New concepts and technologies** for VLSI manufacturing
- **Heterogeneous integration** of non-Si materials/devices on large Si substrates

NEW JOINT TECHNOLOGY AND CIRCUITS FOCUS SESSIONS

Joint technology and circuits focus sessions comprising invited and contributed papers will be offered in special areas of joint interest. Paper submissions highlighting **major innovations and advances in materials, processes, devices, integration, reliability and modeling** in these areas are strongly encouraged:

- **Design in scaled technologies:** Impact of advanced device & interconnect materials or structures on digital circuit performance, power, density; device design & process/technology optimization for analog/mixed-signal circuits.
- **Design enablement:** technology and design co-optimization for improved performance, yield, reliability, ultra-low voltage/power operation, density, and cost.
- **Memory technology and design:** embedded SRAM, DRAM and NVRAM technology/design co-optimization.
- **3D (TSV) and heterogeneous integration:** 3D-technologies and system co-optimization; power delivery and management; thermal management; inter-chip communications; heterogeneous integration.

SUBMISSION OF PAPERS

Prospective authors must submit camera-ready papers in the format of two pages to the following web site:

http://www.vlsisymposium.org

Papers must describe original work with results from experiments or simulations. An author's guide is available on the web site. **Hard copy submissions will not be accepted.** Accepted papers will be published as submitted. Industry and university submissions are encouraged. Partial travel expense support for student presenters is available upon request.

Paper Submission Deadline is January 23, 2012, 5:00 P.M. PST

A very limited number of Late News papers, highlighting very recent and impactful results will be considered. The deadline for Late News paper submission is **March 22nd, 2012, 5:00 P.M. PST**.

The technical content beyond the abstract of an accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium. The IEEE reserves the right to exclude a paper from distribution (*e.g.*, via IEEE Xplore) if the paper is not presented at the conference.

BEST STUDENT PAPER AWARD

The selection of the Best Student Paper will be based upon the quality of the written paper and the presentation. The student must be the lead author and presenter of the paper, and must identify it as a student paper during submission.

VLSI TECHNOLOGY SHORT COURSE on June 11, 2012

A one-day short course will be offered on VLSI technology topics of current interest. Details will be given in the VLSI Technology Symposium Advance Program, which will be posted on the web by April 2012.

SATELLITE WORKSHOP

The 2012 Silicon Nanoelectronics Workshop will be held on June 10-11, 2012, at the same location.

INFORMATION AND REGISTRATION

Prospective attendees can obtain further information and forms for registration and hotel reservations from the Symposium website by visiting www.vlsisymposium.org or from the closest secretariat.

Secretariat for VLSI Symposia (USA)
Widerkehr and Associates
19803 Laurel Valley Place
Montgomery Village, MD 20886, USA
Tel: +1-301-527-0900 ext. 2
Fax: +1-301-527-0994
E-mail: vlsi@vlsisymposium.org

Secretariat for VLSI Symposia (Japan)
c/o ICS Convention Design, Inc.
Chiyoda Bldg. 1-5-18 Sarugaku-cho
Chiyoda-ku, Tokyo 101-8449, Japan
Tel: +81-3-3219-3541
Fax: +81-3-3219-3577
E-mail: vlsisymp@ics-inc.co.jp