2013 Symposia on VLSI Circuits Short Course

(Suzaku I)

Tuesday, June 11

15:55-16:55 Device-Aware Design Flow Management

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Abstract

20nm CMOS technology is the node which stops the smooth evolution toward smaller lithography. Dual patterning lithography and new generation of fully depleted devices were major disruptions which introduce a high level of instability of CMOS device performances and design rules. Tolerance versus process variations is incompatible with analog designer needs but are the constraints he has to comply with. Evolution of analog design methodology is mandatory to insure on-time development of embedded analog functions. Higher level of abstraction is the path to make analog design less sensitive to process effect but is in contradiction with layout dependent effects. The course introduces major process disruptive changes impacting analog design and shows how new design methodology has to be deployed to insure fast and safe development of embedded analog functions.

Biography

Pierre Dautriche was born in Mazingarbe, France, in 1960. He received the M.Sc degree in Microelectronics engineering from the Institut Supérieur d'Electronique du Nord in France in 1982, followed by a Ph.D degree from the University of Lille, France.

From 1983 to 1987, he was appointed RF design engineer at the Philips Research Laboratories in Limeil Brevannes, France. His main focus was the development of tuners for TV applications using GaAs technology. In 1987, he joined Thomson Tubes Electroniques in Saint-Egrève, France where he was working as project leader in the field of CCD sensor development. In 1991, he joined Thomson Military and Space Components organization where he put in place IR technology. During this period he worked on CCD multiplexer technology associated to PtSi and pyroelectric processes. In 1993, he took the lead of rad-hard component development group. At that time his main activity was focused on the development of memory and CPUs using SOI technology. During the same period he took the lead of the high speed analog to digital converter group. In 1995, I joined Thomson Consumer Electronics Components where he was appointed group leader of the CMOS analog IP activity.

In 1998, he joined STMicroelectronics as group leader of the CMOS analog IP group delivering CMOS analog IP across STMicroelectronics organization. At that time the main focus was the development of high performance analog functions such as high speed ADC and DAC, frequency synthesizers using standard digital CMOS process. He was then appointed engineering director in charge of the development of consumer applications receiver products. His activity covered RF technology as well as advanced CMOS for mixed chip application. In 2007, he joined the Technology R&D organization of STMicroelectronics and he is actually Director of Analog and Mixed Signal activities covering both IP development and Analog Design methodology.

He has published in scientific media and has filed numerous patents in the field of analog design technology.