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Media Contacts:

Secretariat for VLSI Symposia (Japan and Asia)
c/o ICS Convention Design, Inc.
Chiyoda Bldg. 1-5-18 Sarugaku-cho, Chiyoda-ku,
Tokyo 101-8449 Japan
Tel: +81-3-3219-3541
Fax: +81-3-3219-3577
E-mail: vlsisymp@ics-inc.co.jp

BtB Marketing (NorthAmerica and EU)
Chris Burke
BtB Marketing
co-Media Relations Director
Tel: +1-919-872-8172
E-mail: chris.burke@btbmarketing.com

For Immediate Release

Tip Sheet for 2013 Symposia on VLSI Technology and Circuits

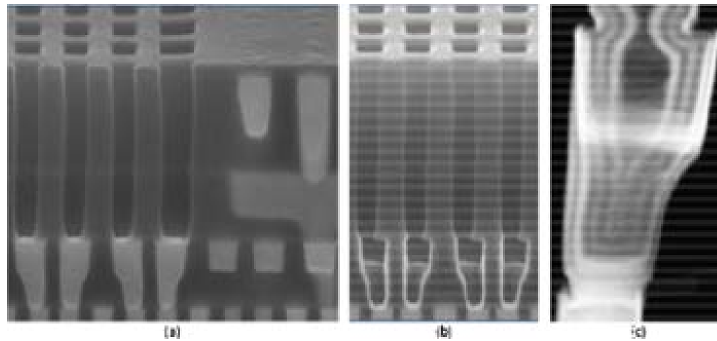
KYOTO, JAPAN -- This Tip Sheet is an advance look at some of the most newsworthy papers to be presented at the 2013 Symposia on VLSI Technology and Circuits, which will be held at the Rihga Royal Hotel Kyoto, Kyoto Japan here June 11-13, 2013 (Technology) and June 12-14, 2013 (Circuits).

A) Symposium on VLSI Technology Highlight Papers

22-nm Embedded DRAM SoC Technology featuring Trigate Transistors and MIMCAP COB

Mass production of high performance CPU with 22 nm generation CMOS devices has been already started in last year. At this year's Symposium on VLSI Technology, Intel will report technical details of their embedded DRAM with 22 nm generation technology on bulk silicon wafer. They realized 0.029 μm^2 DRAM cell capable of meeting >100 μs retention at 95 C. The excellent leakage and performance characteristics of Tri-gate transistors have been optimized for the access transistor, while maintaining the performance needed to enable high performance circuits in the same die. A high aspect-ratio, 3-D Capacitor-Over-Bitline(COB) metal-insulator-metal(MIM) capacitor trench has been integrated into the ultra-low-k interlayer dielectric and Cu metallization used for interconnect stacks. Excellent retention capability and yield have been demonstrated.

(*Paper T2-1,* "A 22nm High Performance Embedded DRAM Technology Featuring Tri-gate Transistors and MIMCAP COB," R. Brain *et al.*, Intel)

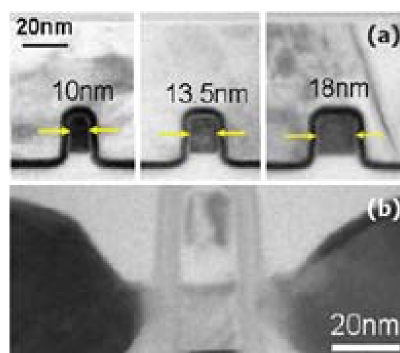


Cross-section transmission electron micrograph of
a high aspect-ratio COB eDRAM bitcell array.

Aggressively scaled SiGe Channel on insulator Trigate pFET with implant-free process

The adoption of advanced high-mobility Silicon Germanium(SiGe) channel materials with aggressively scaled Tri-gate pFETs on insulator is reported for the first time. SiGe is widely known as a suitable channel material for p-type MOS device, thanks to its higher hole mobility than that in conventional silicon material. In this paper, IBM and GLOBALFOUNDRIES report a SiGe channel Tri-gate pFET with aggressively scaled Fin width(W_{fin}) and Gate length(L_g) dimensions, which is fabricated using SiGe on insulator substrate. Excellent electrostatic control down to L_g= 18 nm and W_{fin}< 18 nm has been reported. Using an optimized implant-free raised source/drain process, on-current I_{on} = 1.1 mA/μm at off-leakage current I_{off} = 100 nA/μm and supply voltage V_{dd}= 1.0 V has been achieved.

(Paper T2-2, "*High Performance $Si_{1-x}Ge_x$ Channel on Insulator Trigate PFETs Featuring an Implant-Free Process and Aggressively-Scaled Fin and Gate Dimensions*," P. Hasemi *et al.*, IBM& GLOBALFOUNDRIES.)

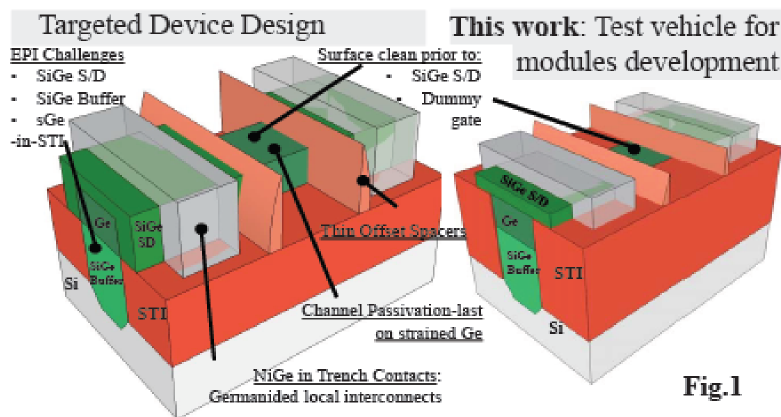


(a) Cross-section TEM images across SiGe fin with H_{fin} = 17 nm and W_{fin} = 10.0, 13.5 and 18.0 nm.
(b) Cross-section TEM image of a single-fin with Gate length less than 20 nm.

Strained Ge-in-STI Implant-Free Quantum Well pFETs for Silicon-compatible CMOS platform

To proceed "More Moore" for 10 nm technology node and beyond, higher performance of current drive should be required for scaled device, especially in pFET. One approach for device performance improvement is to use Silicon Germanium(SiGe) or Germanium as a channel material to enhance hole mobility than strained silicon, as shown in the previous paper. In this work, IMEC and GLOBALFOUNDRIES present a first demonstration of Strained Germanium(sGe) channel pFETs fabricated on SiGe strain relaxed buffers(SRB), which is surrounded by STI(Shallow Trench Isolation) region. Also, they introduced raised SiGe source/drain structure (Ge concentration = 75%) with implant free quantum well(IFQW), Replacement Metal Gate process and Germanide in contacts to solve void issues for this device. Thanks to highly strained Ge channel, hole mobility up to 550 cm^2/Vs and record NBTI reliability at T_{inv} ~ 1.7 nm are demonstrated.

(Paper T2-3, "*First Demonstration of Strained Ge-in-STI IFQW pFETs Featuring Raised SiGe 75% S/D, Replacement Metal Gate and Germanided Local Interconnects*," J. Mitard et al., IMEC & GLOBALFOUNDRIES)



Schematic view of proposed(Left) and studied (Right) structure of Ge-in- STI IFQW pFETs with raised SiGe source/drain and Germanided Local Interconnects. Germanium channel is regrown on SiGe buffer region which is defined by STI.

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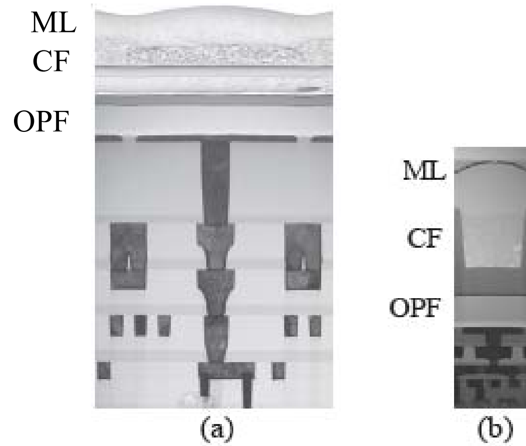
Organic Photoconductive Film Image Sensor with Extremely High Saturation

Silicon CMOS image sensor(CIS) has been widely used for digital still cameras, cellular phones and smart phones. Nowadays, both sensitivity improvement and noise reduction have been continuously done with much efforts. Even though, still one serious problem remains for CIS; relatively low dynamic range for capturing both bright and dark images at the same time. To improve the dynamic range in the image sensor, Panasonic and FUJIFILM propose the image sensor with thin organic photoconductive film(OPF), laminated on CMOS circuits. Owing to high capacity of a charge storage node, the saturation level is 12 dB higher than those of conventional silicon CIS. Because of the very thinness of the laminated film, the device is crosstalk-free structure. Also, an incident light angle of over 30-degree is realized in this novel structure.

(Paper T2-4, "*Thin Organic Photocunductive Film Image Sensors with Extremely High Saturation of 9500 electrons/μm²*," M. Mori *et al*., Panasonic and FUJI FILM)

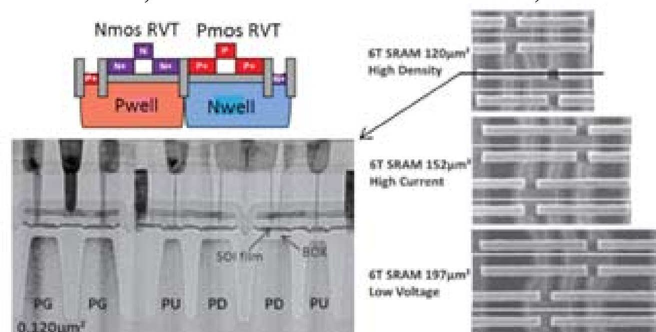


Cross Sectional TEM images of 3.0 μm (LHS) and 0.9 μm(RHS) pixels
of Organic Photoconductive Film Image Sensor
ML: Micro Lense, CF: Color Filters, OPF: Organic Photoconductive Film

Ultra Low Leakage, High Speed and Low Voltage FDSOI SRAMs

In this paper from STMicroelectronics and CEA-LETI, six Transistor SRAM(6T-SRAM) cells for High Density (0.120 μm^2), High Current (0.152 μm^2) and Low Voltage(0.197 μm^2) purposes are fabricated with 28 nm node FDSOI technology for the first time. Starting from a direct porting of bulk planar CMOS design, the improvement in read current I_{read} has been confirmed up to +50% (@V_{dd}=1.0V) & +200%(@ V_{dd}=0.6 V), respectively, compared with 28 nm Low-Power(LP) CMOS technology. Additionally, -100mV minimum operating voltage(V_{min}) reduction has been demonstrated with 28 nm FDSOI technology. Alternative flip-well and single well architecture provides further speed and V_{min} improvement, down to 0.42V on 1Mb 0.197μm^2. Ultimate stand-by leakage below 1pA on 0.120μm^2 bitcell at V_{dd}=0.6V is finally reached by taking the full benefits of the back bias capability of FDSOI.

(Paper JJ2-3, "*FDSOI Process/Design full solutions for Ultra Low Leakage*, *High Speed and Low Voltage SRAMs*," R. Ranica et al., STMicroelectronics & CEA-LETI)



Cross-sectional and plain view of FDSOI SRAM cells for High Density (0.120 μm^2), High Current (0.152 μm^2) and Low Voltage(0.197 μm^2).

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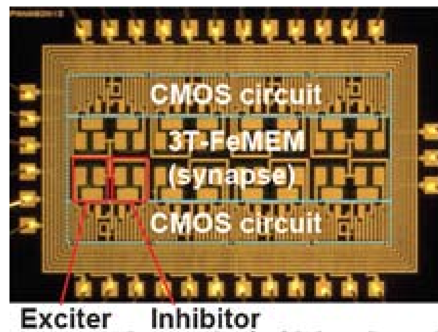
Three-Terminal Ferroelectric Memristor enabling On-chip Pattern recognition

Neural network is among the most effective learning and cognitive methods to achieve low power, highly parallel and flexible systems. To realize the function of the synopse, continuous conduction modification is required for the circuit elements. In previous report, two-terminal non-volatile memory, such as ReRAM or PCRAM, was used for this purpose, however the trial has not been fully succeeded. In this paper, on-chip pattern recognition in a neural network circuit using three-terminal non-volatile memories is demonstrated for the first time. The authors from Panasonic fabricated the module chip of the neural network with 16 synopses using multiple three-terminal ferroelectric memristors (3T-FeMEMs). By using the analog and non-volatile conductance change of the 3T-FeMEM as a synaptic weight, the matrix patterns are successfully learned. By using this system, even when an incomplete pattern is input to the neural network circuit, it automatically recognizes the original pattern.

(Paper T16-2, "Neural Network based on a Three-Terminal Ferroelectric Memristor to Enable On-chip Pattern Recognition," Y. Kaneko *et al.*, Panasonic)



Chip micrograph of fabricated neural network chip with Ferroelectric Memristors.

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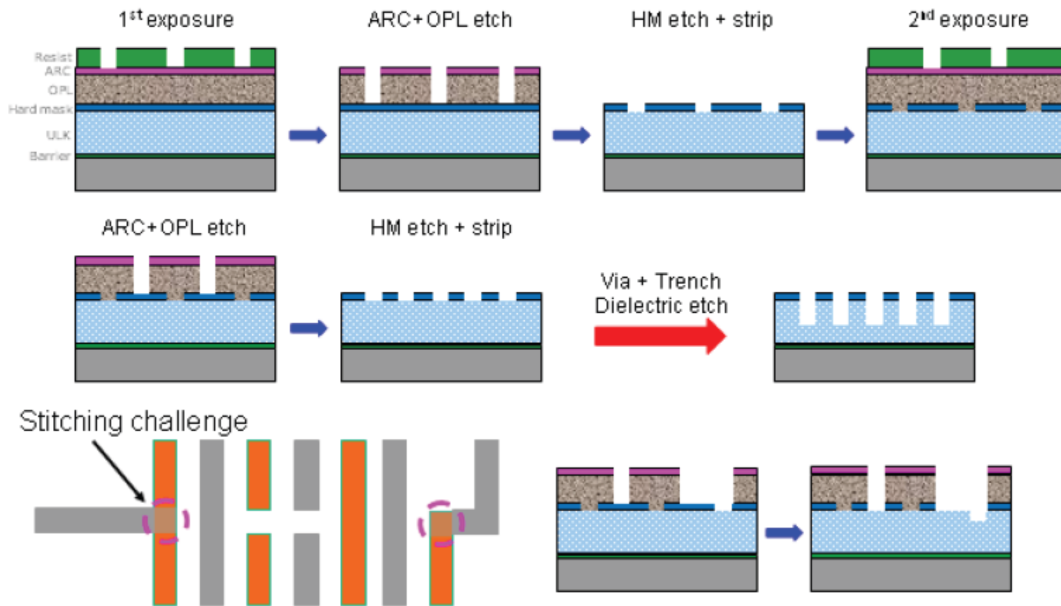
64 nm Pitch Interconnects

In this paper, the authors from STMicrolectronics, Samsung, GLOBAL FOUNDRIES and IBM report 64nm pitch BEOL integration and material strategy to enable aggressive groundrules and extendibility for multi-node insertions. Exploitation of bright field entitlements at trench and via lithography enables tight via and bi-directional trench pitch. Setting the same mask metal spacing equal to contacted poly pitch(CPP) maximized density scaling and speed of standard cell automation by avoiding cell abutment conflicts. A Self-Aligned-Via (SAV) approach was exploited for single pattern via extendibility, enabling via placement at CPP with a single mask. The resulting groundrules and process module have been plugged in to multiple technology nodes without re-development needed. Scaling, performance, and reliability requirements are achieved across a spectrum of low power-high performance applications.

(Paper T14-5, "*64nm Pitch Interconnects: Optimized for Designability, Manufacturability and Extendibility*," C. Goldberg et al., STMicroelectronics, Samsung, GLOBALFOUNDRIES, IBM)

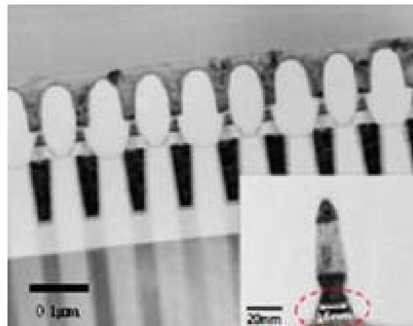


Double patterning with Lithography-Etching & Lithography-Etching (LELE) process flow of Trench formation for 64nm pitch interconnect.

Sub-20 nm perpendicular STT-MRAM with enhancement of switching margin

The most important challenges for Spin-Transfer-Torque Magnetoresistive Random Access Memory(STT-MRAM) technology for sub-20 nm node is to control strong magnetostatic interactions between magnetic layers, which causes the lack of the stability of each functional layers in perpendicular MTJs. The authors from Samsung report the stable magnetization switching without magnetostatic interference by introducing a novel structure with superior pinned layer stability. Wide switching field margins have been secured for reproducible STT switching as well as a tightly controlled H_{offset} below 100 Oe. Switching voltage margin of the novel structure are also wide enough to show definite STT switching.

(Paper T6-3, "*Enhancement of switching margin by utilizing superior pinned layer stability for sub-20 nm perpendicular STT-MRAM*," W. C. Lim et al., Samsung)



Cross-sectional TEM image of MTJs at 20 nm node

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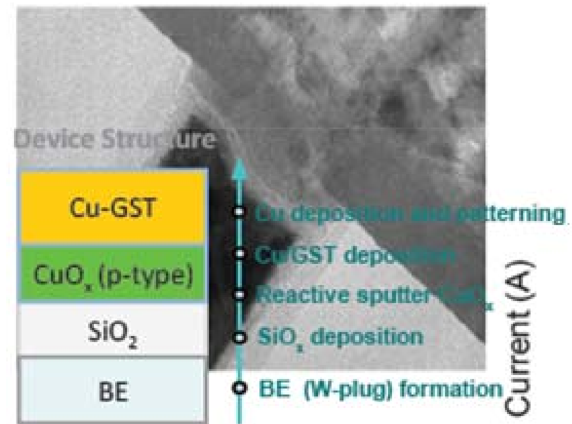
Novel Conducting Bridge Resistive Memory using a Semiconducting Dynamic E-field Moderating Layer

Resistive Random Access Memory (ReRAM) has drawn much interest recently for post-NAND flash memory devices, because of its high On/Off ratio, high speed and good scalability, etc. Conducting bridge resistive memory utilizes the switching by forming and disrupting a thin conducting filament, but this phenomenon causes high E-field in the insulator just before the filament is completed (or begins to disrupt). This paper from Macronix addresses, for the first time, degradation caused by this high E-field and a novel solution is proposed. A p-type CuOx semiconductor layer is added as an E-field moderator that dynamically reduces the E-field. The proposed CuOx layer at the Cu-GST/SiO_2 interface not only eliminates this issue but also serves as a Cu back-diffusion barrier, both greatly improve the device performance.

(Paper T8-4, "*A Novel Conducting Bridge Resistive Memory Using a Semiconducting Dynamic E-field Moderating Layer*," F. M. Lee et al., Macronix)



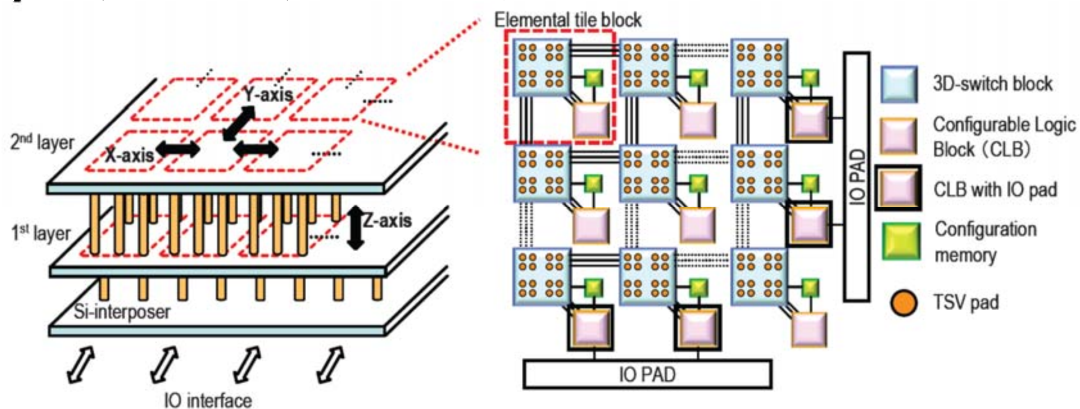
TEM image and the cell structure of the EM Conducting Bridge Device. By adding a p-type CuOx layer, the applied voltage is redistributed, and E-field is reduced.

B) Symposium on VLSI Circuits Highlight Papers

Can we build high performance 3D structures for increased scalability of FPGAs?

Field Programmable Gate Arrays (FPGAs) have become a viable alternative to custom Integrated Circuits (ICs) by providing flexible computing platforms with improved costs and shorter time to-market. Three-dimensional (3D) Integrated Circuits (ICs) with Through Silicon Vias (TSV) is a technology that will increase the functionality, scale of integration, and performance of integrated systems. This paper features a low-capacitance embedded TSV design with improved Z-axis transmission performance. It also describes an innovative clock synchronization scheme for reduced clock skew between the layers.

(*Paper C3-5,* "Scalable 3D-FPGA using wafer-to-wafer TSV interconnect of 15 Tbps/W, 3.3 Tbps/mm2," F. Furuta *et al*, ASET and Hitachi)



Architecture of a homogeneous 3D-FPGA.

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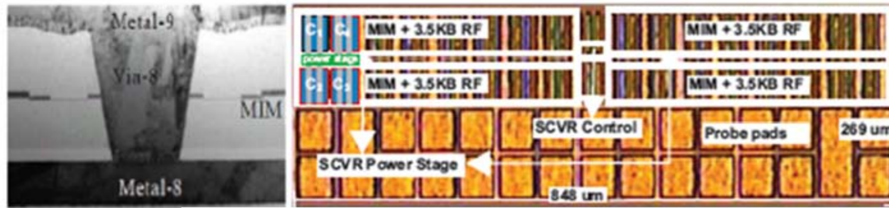
Implementation of a Fully Integrated Switched Capacitor Step-Down DC-DC Converter in 22nm Tri-Gate CMOS Process

Today, high-performance DC-DC converters have been developed for dynamic voltage and frequency scaling (DVFS) and/or multi-voltage system-on-chip designs. In the DC-DC converter session, Intel Corporation will present a switched capacitor step-down converter designed in a 22nm tri-gate CMOS technology that has been highlighted by its feasibility and future prospects. The converter provides a wide output voltage range of 0.45-1V from a fixed input voltage of 1.225V by changing the connection of high-density MIM capacitors, and achieves 84% maximum-conversion efficiency. It supports all digital feedback control and significantly small die area.

(*Paper C13-5,* "A 0.45-1V Fully Integrated Reconfigurable Switched Capacitor Step-Down DC-DC converter with High Density MIM Capacitor in 22nm Tri-Gate CMOS," R. Jain *et al*, Intel)

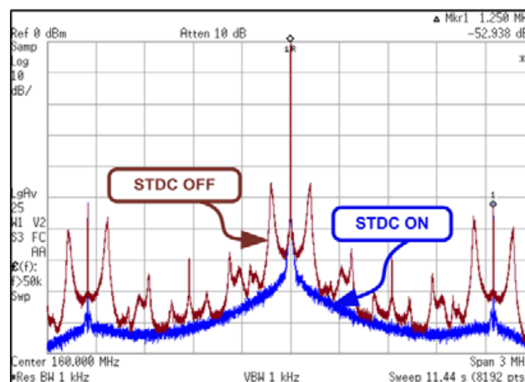


Cross-sectional TEM image of MIM capacitor and die photo.

A 2.5GHz 5.4mW 1-to-2048 Digital Clock Multiplier using a Scrambling TDC

Digital PLLs (DPLLs) have emerged as an attractive architecture for clock generation in nanometer CMOS technologies. Despite their digital-friendly nature, DPLLs suffers from jitter degradation of time-to-digital converters (TDC). This work from Oregon State University presents a low-jitter digital PLL with a novel scrambling TDC which suppresses jitter by reducing jitter accumulation time without a power hungry high resolution TDC. It generates 150MHz to 2.56GHz while achieving 2.7ps-rms jitter and consuming only 5.4mW, which is the lowest jitter and best power efficiency for large divider value PLLs.

(*Paper C12-1,* "A 2.5GHz 5.4mW 1-to-2048 Digital Clock Multiplier using a Scrambling TDC," R. N. Nandwana *et al*, Oregon State Univ.)



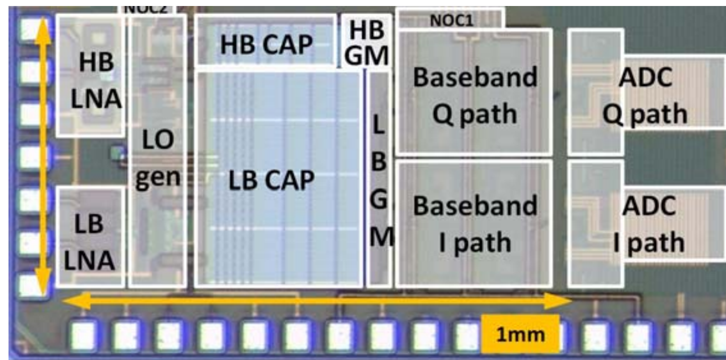
Measured output spectrum with and without scrambling TDC (STDC).

A Step Toward Practical Use of Software-Defined-Radio by Advanced CMOS

For practical use of software-defined-radio (SDR) transceiver, aggressive power reduction and frequency band extension by technology scaling is essential while keeping high linearity even at low power supply voltage. A paper from IMEC Leuven and Renesas Electronics Corp. presents the first 28nm-CMOS high-linear wideband SDR receiver. In the frequency range from 0.4 to 6 GHz, it achieves a noise figure of 1.8 - 3dB, IIP2 higher than 85dBm, and out-of-band IIP3 higher than 3dBm at power consumption

less than 40mW from 0.9V supply voltage. The paper raises expectations of the SDR transceiver even for mobile terminals.

(*Paper C11-1,* "A 0.9V Low-Power 0.4-6GHz Linear SDR Receiver in 28nm CMOS," J. Borremans *et al*, IMEC)

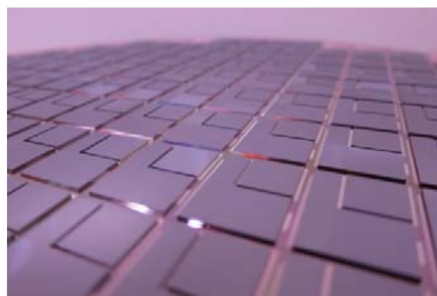


Die photo of the 28nm-CMOS high-linear wideband SDR receiver.

CoWoS (Chip-on-Wafer-on-Substrate) for Next Generation Memory Interface?

3D stacking technologies for heterogeneous integration are becoming essential innovations for the industry's move beyond Moore's Law. Memory interfaces also seek the optimized solution by mixing various technologies such as TSV (through-silicon via), Wide-IO, MCP (multi-chip package), POP (package-on-package), and silicon interposer. Engineers in TSMC demonstrate a 1 Tera b/s embedded DRAM interface implemented with their frontend-to-backend heterogeneous integration solution named CoWoS. This paper describes a low-cost 1024-bit wide parallel transceiver communicating between an eDRAM and a SoC fabricated in 40nm CMOS which are stacked on a silicon interposer chip in 65nm CMOS.

(*Paper C3-1,* "An Extra Low-Power 1Tbit/s Bandwidth PLL/DLL-less eDRAM PHY Using 0.3V Low-Swing IO for 2.5D CoWoS Application," M. Lin *et al*, TSMC)

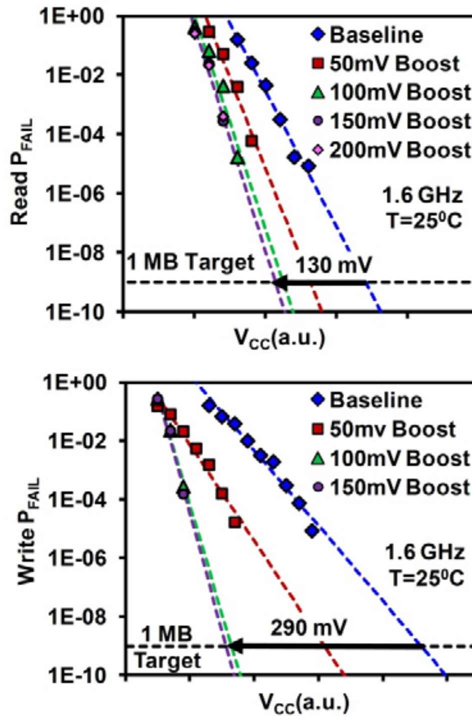


Die photo after stacking.

Dual-Vcc 8T-bitcell SRAM Array in 22nm Tri-Gate CMOS for Energy-Efficient Operation across Wide Dynamic Voltage Range

A 14KB 8T-bitcell SRAM array is demonstrated in 22nm tri-gate CMOS with fine-grain dual-Vcc assist techniques. Vmin limiting 8T-bitcell nodes are boosted selectively during read and write to improve overall chip-Vmin. Bit failure rates (Pfail) are measured for different Vboost values above Vcc and incremented in 50mV steps. Extrapolations of the measured Pfail vs. Vcc data to a 1MB target array size demonstrate 130mV lower read-Vmin and 290mV lower write-Vmin compared to the baseline single Vcc design at 1.6GHz. Measurements show 130-290mV lower Vmin with 27-46% lower power at 0.4-1.6GHz for varying amounts of boosting, array activity and voltage regulator efficiency.

(*Paper JJ2-6,* "Dual-Vcc 8T-bitcell SRAM Array in 22nm Tri-Gate CMOS for Energy-Efficient Operation across Wide Dynamic Voltage Range," J. Kulkarni *et al*, Intel)

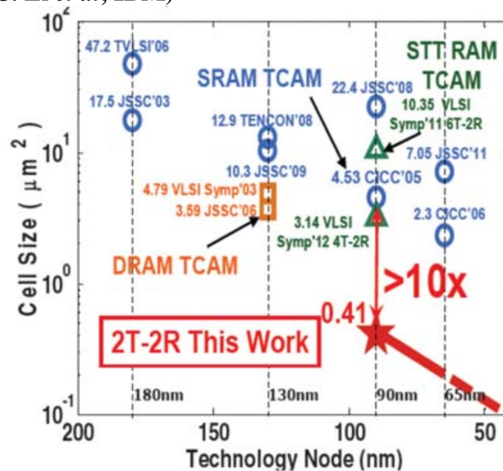


Measured read and write failure rate (P_{FAIL}) vs. V_{CC}.

Smallest Nonvolatile TCAM Cell Based on Phase Change Memory Technology

The first demonstrated nonvolatile TCAM chip using a 2-transistor/2-resistive-storage cell with PCM technology is unveiled. The proposed TCAM cell realizes smallest cell size, which is 1/10 of SRAM cells. In addition to the cell technology, a novel search operation called two-bit encoding scheme and a proposed clocked self-referenced sensing scheme are implemented in a 1Mb TCAM chip with 90-nm CMOS technology. The chip achieves short match delay of 1.9 ns and 9.8 ns under operation voltage of 1.2 V and 0.75 V, respectively.

(*Paper C9-1,* "1Mb 0.41 μm² 2T-2R Cell Nonvolatile TCAM with Two-bit Encoding and Clocked Self-Referenced Sensing," J. Li *et al*, IBM)



Comparison of proposed TCAM cell size with the state-of-art.

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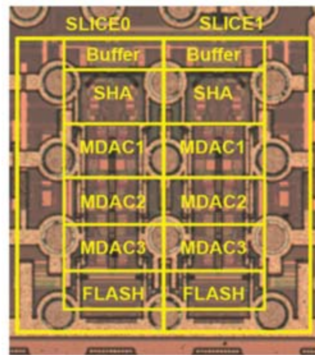
High-Performance, Low-Power ADC

Broadcom will present a 5.4-GS/s 12-bit time-interleaved pipeline analog-to-digital converter (ADC) which enables wideband direct sampling receivers for most wired and wireless communication systems. To achieve high-speed and low power consumption, novel amplifier topology and multiplying digital-to-analog converter (MDAC) structure are proposed. The ADC is implemented in 28-nm CMOS technology, and achieves a signal-to-noise ratio (SNR) of 61-dB up to 2.6GHz input frequency, while consuming only 500mW.

(*Paper C8-1,* "A 5.4GS/s 12b 500mW Pipeline ADC in 28nm CMOS," J. Wu *et al*, Broadcom)

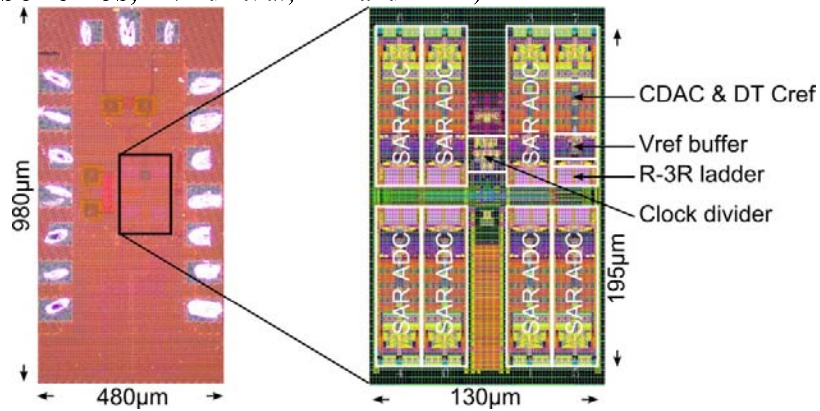


Die photo of the 5.4-GS/s 12-bit time-interleaved pipeline analog-to-digital converter.

An 8bit 8.8GS/s ADC for Next-Generation High-Speed Links

This is one of the most important papers in the session of Nyquist Converters. The 8x interleaved SAR ADC has achieved a high speed operation with low power consumption of 35mW at 1V supply voltage and small chip area of 130um x 195um in 32nm CMOS SOI technology. Its FoM is 58fJ/conversion-step. This ADC with superior performance than existing 6bit-accuracy over-4GS/s ADCs is based on various interesting techniques including a low-power voltage reference buffer with per-channel gain control and a pass-gate selection clocking scheme for low skew, and will be presented by IBM Research (Zurich) and EPFL at the conference.

(*Paper C21-1,* "A 35mW8b 8.8 GS/s SAR ADC with Low-Power Capacitive Reference Buffers in 32nm Digital SOI CMOS," L. Kull *et al*, IBM and EPFL)

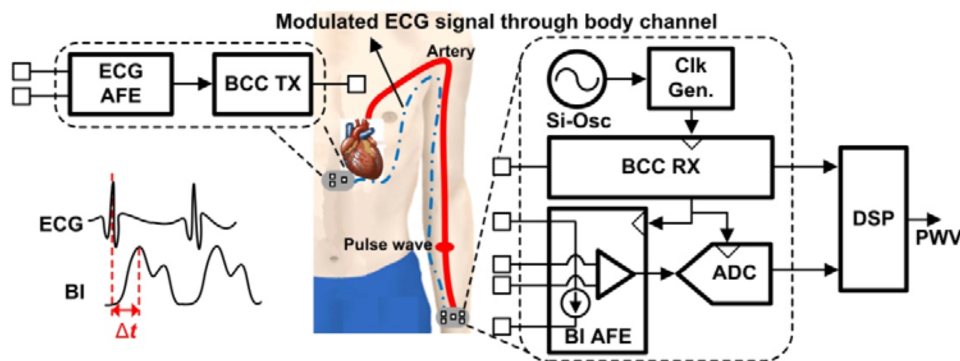


Die photo and layout of the 32nm 8bit 8.8GS/s ADC.

An Integrated Pulse Wave Velocity Sensor using Bio-impedance and Noise-shaped Body Channel Communication

Pulse wave velocity (PWV) is a measure of arterial stiffness which is an important indicator to diagnose cardiovascular disease. KASIT proposes an all-electrical PWV measurement system with an ECG sensor and an integrated PWV sensor, which are put on chest and wrist, respectively. The developed PWV sensor detects the ECG signal which propagates along the artery and measures the bio-impedance (BI). PWV is calculated from the time-difference between the signals from the ECG sensor and the BI sensor. Such an electrical measurement system based on body channel communication can remove cumbersome wires on the body.

(*Paper C17-4,* "An Integrated Pulse Wave Velocity Sensor using Bio-impedance and Noise-shaped Body Channel Communication," W. Lee *et al*, KAIST)



PWV sensor architecture.

Here are definitions of some important technical terms:

- **Back-End/BEOL** and **Front-End/FEOL** -- In integrated circuit manufacturing, transistors and other active devices are built first (at the front end of the manufacturing line or FEOL), while the interconnect, or the wiring, is built afterward, at the "back end" of the manufacturing line (BEOL).
- **CMOS/MOS/MOSFET/FET**-- Most transistors today are FETs, or field-effect transistors. Most FETs are built with CMOS manufacturing technology (complementary metal oxide semiconductor). Generically they are called MOSFETs, or sometimes MOS transistors.
- **COB --** Capacitor Over Bitline. A kind of DRAM storage capacitor, a part of which overhangs on the bitline.
- **Compound/III-V Semiconductors** -- Most semiconductors are silicon-based, but researchers continue to investigate other semiconducting materials with higher electron mobilities because they can be used to make faster devices. The tradeoff is that the materials are harder to work with than silicon.Compound semiconductors are made of two or more elements (e.g. GaAs, InP, GaN, etc.) which are generally found in groups III and V of the periodic table of the elements.
- **CPP** --Contacted Poly-Silicon (Gate) pitch.
- **FinFET** -- A transistor whose shape resembles a fin, usually with multiple gates surrounding it for better on/off switching control.
- **Front-End/FEOL and Back-End/BEOL** -- In integrated circuit manufacturing, transistors and other active devices are built first (at the front end of the manufacturing line or FEOL), while the interconnect, or the wiring, is built afterward, at the "back end" of the manufacturing line (BEOL).
- **High-k Dielectrics/Metal Gates** -- A dielectric is an electrical insulator. "k" is the relative permittivity and is a measure of how well a material will prevent current flow between the gate electrode and the channel region of a field-effect transistor, while capacitively coupling the two to control on/off switching. In future CMOS integrated circuits (chips) the gate dielectric will need to provide capacitive coupling equivalent to that of a silicon-dioxide layer that is just a few atoms thick, to allow the length of the channel region to be scaled down to 10 nm and below. Metal gate materials are more compatible with high-k gate dielectrics than are traditional doped polycrystalline silicon material. Much progress has been made in recent years to integrate metal gates into the CMOS process flow for the manufacture of high-performance chips.
- **III-V** -- see Compound/III-V Semiconductors
- **Integrated Circuit** -- An electrical circuit comprising many interconnected elements (e.g. transistors, diodes, capacitors, resistors, inductors) built on a semiconducting substrate.
- **Interconnect** -- The metal lines, or wiring, connecting transistors and other circuit elements. See **Back-End/BEOL**.
- **Low-k Dielectrics/Interconnect** -- Interconnect refers to the metal wires that connect elements together in an integrated circuit (chip). The close proximity of adjacent wires can result in capacitance that can limit chip performance. A low-k dielectric is needed, to electrically insulate the copper lines while minimizing their mutual capacitance, but these materials are generally more fragile and thus pose challenges for manufacturing.
- **MEMS** -- A micro-electro-mechanical system, containing micrometer-scale moving parts.
- **MIMCAP**– Metal-Insulator-Metal Capacitance fabricated by BEOL process.
- **N-FET/P-FET or NMOS/PMOS** -- MOSFETs come in two varieties (n-channel or p-channel) which operate in a complementary fashion.
- **Non-volatile memory (NVM)** – A type of computer memory that retains its stored information even when the power is off.
- **Phase-Change Memory/PCM** -- Phase-change materials have crystalline and non-crystalline states which are used to represent the digits "0" or "1" in computer non-volatile memory. Electrical current is used to toggle between the two states – heat from the current causes the material to change its state.
- **Resistive Random Access Memory** -- A non-volatile memory device which uses the resistance change for data storage. The resistance change is caused by the filament formation or disruption within the insulator by high voltage application.
- **Scaling/Density/Integration** -- Scaling is making transistors and other circuit elements smaller so that more of them will fit on a chip. A denser chip has more transistors on it than one which is less

dense. Integration is combining circuit elements on a chip to add more functions to achieve lower cost per function.

- **Semiconductor** -- A material that can be made to conduct or to block the passage of electrical current, giving the ability to store and process information.
- **SOI** -- A silicon-on-insulator substrate, used to reduce parasitic capacitance and thereby improve integrated circuit performance
- **Spin Transfer Torque Magnetoresistive Random Access Memory (STT-MRAM)**-- A kind of non-volatile random-access memory device which uses the magnetoresistance change for data storage. Basically, MRAM cell is composed of driver transistor and magnetic tunnel junction(MTJ). The resistance of MTJ is dependent on the spin state of the magnetic thin film in the MTJ, which is controlled by the external magnetic field or the spin polarized electron current. In latter case, spin transfer torque(STT) is the main force of the switching. Both high speed and low power consumption are expected in STT-MRAM.
- **Strained silicon & SiGe stressors** -- Silicon is said to be "strained" when its atoms are pulled farther apart or closer together than normal. Doing so alters the ease with which electrons flow through the silicon, enabling transistors built with it to operate faster and /or at lower voltage. The external **stressors** which impart strain are materials with slightly different atomic spacing than silicon. For example, a common way to compressively strain the channel region of a p-channel silicon field-effect transistor is to embed silicon-germanium (**SiGe**) – which has larger atomic spacing than does Si -- in the source and drain regions which it spans
- **SRAM** -- A type of computer memory (static random access memory) that uses six or more transistors to store each bit of information. It can be written to and read from very quickly.
- **Technology Generations/Nodes** – High-volume production of 32-nm generation CMOS chips by leading companies is established. The next generation, 22 nm, has entered production in 2012.
- **Transistor** -- A tiny electrical switch that serves as the building block for integrated circuits. It has no moving parts and is made with a semiconductor material, usually silicon. Transistors can be ganged together by the billions on chips and programmed to receive, process and store information, and to output information and/or control signals.

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