2013 Symposia on VLSI Technology and Circuits June 11th (Tuesday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
7:30-17:00	**Registration**				
8:30-10:05	**8:20-11:50 Circuits Short Course**		**8:20-11:50 Circuits Workshop**	**T1 "Welcome and Plenary Session"** T1-1 8:30-8:45 ***Welcome and Opening Remarks*** T1-2 8:45-9:25 (**Plenary**) TSMC System Scaling and Collaborative Open Innovation T1-3 9:25-10:05 (**Plenary**) Qualcomm Technologies System Design Considerations for Next Generation Wireless Mobile Devices	
10:30-12:10	8:20-11:50 Circuits Short Course		8:20-11:50 Circuits Workshop	**T2: Highlight** T2-1 10:30-10:55 Intel A 22nm High Performance Embedded DRAM SoCTechnology Featuring Tri-Gate Transistors and MIMCAP COB T2-2 10:55-11:20 IBM Research High-Performance Si1-xGex Channel on Insulator Trigate PFETs Featuring an Implant-Free Process and Aggressively- Scaled Fin and Gate Dimensions, T2-3 11:20-11:45 GLOBALFOUNDRIES First Demonstration of Strained Ge-in-STI IFQW pFETs Featuring Raised SiGe75% S/D, Replacement Metal Gate and Germanided Local Interconnects T2-4 11:45-12:10 Panasonic Thin Organic Photoconductive Film Image Sensors with Extremely High Saturation of 8500 electrons/μm^2	
13:30-15:35	13:40-17:00 Circuits Short Course		13:40-17:00 Circuits Workshop	**T3: Ge MOSFET** T3-1 13:30-13:55 The Univ. of Tokyo Examination of Physical Origins Limiting Effective Mobility of Ge MOSFETs and the Improvement by Atomic Deuterium Annealing T3-2 13:55-14:20 The Univ. of Tokyo Enhancement of High-Ns Electron Mobility in Sub-nm EOT Ge n-MOSFETs T3-3 14:20-14:45 GNC Enhancement o f Hole Mobility and Cut - Off Characteristics of Strained Ge Nanowire pMOSFETs by Using Plasma Oxidized GeOx Inter-Layer for Gate Stack T3-4 14:45-15:10 Stanford Univ. Fabrication of GeSn-On-Insulator (GSOI) to Enable Monolithic 3D Co-Integration of Logic and Photonics T3-5 15:10-15:35 National Univ. of Singapore Uniaxially Strained Germanium-Tin (GeSn) Gate-All-Around Nanowire PFETs Enabled by a Novel Top-Down Nanowire Formation Technology	**T4: (FS) 3D System and Packaging** T4-1 13:30-13:55 (**Invited**) Altera Manufacturability Optimization and Design Validation Studies for FPGA-Based, 3D Integrated Circuits T4-2 13:55-14:20 (**Invited**) IBM Research Scaling Challenges of Packaging in the Era of Big Data T4-3 14:20-14:45 TSMC An Integrated Air Gap Structure to Achieve High-Performance TSV Interconnects for 28nm 3D-IC Integration T4-4 14:45-15:10 Seoul National Univ. A New Guard-Ring Technique to Reduce Coupling Noise from Through Silicon Via (TSV) Utilizing Inversion Charge Induced by Interface Charge T4-5 15:10-15:35 TSMC High-Performance Inductors for Integrated Fan-Out Wafer Level Packaging (InFO-WLP)
15:50-17:30				**T5: III-V MOSFET** T5-1 15:50-16:15 The Univ. of Tokyo Strained Extremely-Thin Body $In_{0.53}Ga_{0.47}As$-On-Insulator MOSFETs on Si Substrates T5-2 16:15-16:40 The Univ. of Tokyo High Performance Extremely-Thin Body InAs-On-Insulator MOSFETs on Si with Ni-InGaAs Metal S/D by Contact Resistance Reduction Technology T5-3 16:40-17:05 Stanford Univ. Optimal Device Architecture and Hetero-Integration Scheme for III-V CMOS T5-4 17:05-17:30 GNC Demonstration of InGaAs/Ge Dual Channel CMOS Inverters with High Electron and Hole Mobility Using Staked 3D Integration	**T6: (FS) 3D and Emerging Memory** T6-1 15:50-16:15 (**Invited**) Toshiba Bit Cost Scalable (BiCS) Technology for Future Ultra High Density Storage Memories T6-2 16:15-16:40 (**Invited**) Panasonic Comprehensive Understanding of Conductive Filament Characteristics and Retention Properties for Highly Reliable ReRAM T6-3 16:40-17:05 Samsung Enhancement of Switching Margin by Utilizing Superior Pinned Layer Stability for Sub-20nm Perpendicular STT-MRAM T6-4 17:05-17:30 IBM Almaden Research Center Recovery Dynamics and Fast (Sub-50ns) Read Operation with Access Devices for 3D Crosspoint Memory Based on Mixed-Ionic-Electronic-Conduction (MIEC)
20:00-22:00	**Joint Rump Session** **SOC vs. 3D IC in the More-than-Moore Era**			**Technology Rump Session 1** **Low Voltage - How Low Can We Go?**	**Technology Rump Session 2** **Novel Hierarchy in Emerging Memory**

Technology Short Course: June 10th (Monday) 8:10-17:15 / Shunju I
2013 Silicon Nanoelectronics Workshop: June 9th (Sunday) 08:30-18:30, 10th (Monday) 08:30-17:00 / Suzaku III
2013 Spintronics Workshop on LSI: June 10th (Monday) 19:00-22:00 / Suzaku II

2013 Symposia on VLSI Technology and Circuits June 12th (Wednesday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
7:30-17:00	**Registration**				
8:30-9:50				**C1 "Welcome Session"** C1-1 8:30-8:45 ***Welcome and Opening Remarks*** **"Executive Panel "** C1-2 8:45-9:50 ***Executive Panel (4 presentations)***	
10:30-12:35	**C3(JFS): 3D Integrated Circuits & Applications**		**C2: Imagers**	**T7: Advanced FinFET**	**T8: ReRAM 1**
	C3-1 10:30-10:55 TSMC: An Extra Low-Power 1Tbit/s Bandwidth PLL/DLL-Less eDRAM PHY Using 0.3V Low-Swing IO for 2.5D CoWoS Application		C2-1 10:30-10:55 Aptina Japan: A 1-inch Optical Format, 14.2M-Pixel, 80fps CMOS Image Sensor with a Pipelined Pixel Reset and Readout Operation	T7-1 10:30-10:55 National Univ. of Singapore: A New Expandible ZnS-SiO2 Liner Stressor for N-Channel FinFETs	T8-1 10:30-10:55 imec: Modeling RRAM Set/Reset Statistics Resulting in Guidelines for Optimized Operation
	C3-2 10:55-11:20 TSMC: 3D IC Heterogeneous Integration of GPS RF Receiver, Baseband, and DRAM on CoWoS with System BIST Solution		C2-2 10:55-11:20 Univ. of Michigan: A 5.9µm-Pixel 2D/3D Image Sensor with Background Suppression over 100klx	T7-2 10:55-11:20 Samsung: 3 Dimensional Scaling Extensibility on Epitaxial Source Drain Strain Technology toward Fin FET and Beyond	T8-2 10:55-11:20 Macronix International: A Novel High Performance WO_X ReRAM Based on Thermally-Induced SET Operation
	C3-3 11:20-11:45 Macronix International: 3D Stackable Vertical-Gate BE-SONOS NAND Flash with Layer-Aware Program-and-Read Schemes and Wave-Propagation Fail-Bit-Detection against Cross-Layer Process Variations		C2-3 11:20-11:45 Panasonic: An Ultra-Low Noise Photoconductive Film Image Sensor with a High-Speed Column Feedback Amplifier Noise Canceller	T7-3 11:20-11:45 SEMATECH: Effects of Layout and Process Parameters on Device/Circuit Performance and Variability for 10nm Node FinFET Technology	T8-3 11:20-11:45 Fudan Univ.: Reliability Significant Improvement of Resistive Switching Memory by Dynamic Self-Adaptive Write Method
	C3-4 11:45-12:10 CEA, Leti: A 0.9 pJ/bit, 12.8 GByte/s WideIO Memory Interface in a 3D-IC NoC-Based MPSoC		C2-4 11:45-12:10 Columbia Univ.: A 100-fps Fluorescence Lifetime Imager in Standard 0.13-µm CMOS	T7-4 11:45-12:10 imec: Quantum Well Band Calculations and Their Impact on Device Isolation and Work Function Requirements for SiGe and III/V Strained Heterostructure FinFETs	T8-4 11:45-12:10 Macronix International: A Novel Conducting Bridge Resistive Memory Using a Semiconducting Dynamic E-Field Moderating Layer
	C3-5 12:10-12:35 ASET: Scalable 3D-FPGA Using Wafer-to-Wafer TSV Interconnect of 15 Tbps/W, 3.3 Tbps/mm^2		C2-5 12:10-12:35 Univ. of Texas: 820-GHz Imaging Array Using Diode-Connected NMOS Transistors in 130-nm CMOS	T7-5 12:10-12:35 GNC: Superior Cut-Off Characteristics of Lg=40nm W_{fin}=7nm Poly Ge Junctionless Tri-Gate FET for Stacked 3D Circuits Integration	T8-5 12:10-12:35 Stanford Univ.: Dopant Selection Rules for Extrinsic Tunability of HfO_x RRAM Characteristics: A Systematic Study
13:55-16:00	**C5: Delta-Sigma Modulators**		**C4: Circuits for Biomedical Applications**	**JJFS1: Design Enablement**	**T9: PCRAM and MRAM**
	C5-1 13:55-14:20 MediaTek: A 75.1dB SNDR 840MS/s CT ΔΣ Modulator with 30MHz Bandwidth and 46.4fJ/conv FOM in 55nm CMOS		C4-1 13:55-14:20 Hong Kong Univ. of Sci. and Tech.: A 200-Channel 10µW 0.04mm^2 Dual-Mode Acquisition IC for High Density MEA	JJ1-1 13:55-14:20 **(Invited)** TSMC: Enabling Circuit Design Using FinFETs through Close Ecosystem Collaboration	T9-1 13:55-14:20 LEAP: Charge Injection Super-Lattice Phase Change Memory for Low Power and High Density Storage Device Applications
	C5-2 14:20-14:45 Univ. of Michigan: A 69dB SNDR, 25MHz BW, 800MS/s Continuous-Time Bandpass ΔΣ ADC Using DAC Duty Cycle Control for Low Power and Reconfigurability		C4-2 14:20-14:45 Case Western Reserve Univ.: A Neurochemical Pattern Generator SoC with Switched-Electrode Management for Single-Chip Electrical Stimulation and 9.3µW, 78pA_{rms}, 400V/s FSCV Sensing	JJ1-2 14:20-14:45 Intel: A 3.6GB/s 1.3mW 400mV 0.051mm^2 Near-Threshold Voltage Resilient Router in 22nm Tri-Gate CMOS	T9-2 14:20-14:45 Macronix International: A Scalable Volume-Confined Phase Change Memory Using Physical Vapor Deposition
	C5-3 14:45-15:10 Intel: A 66dB SNDR 15MHz BW SAR Assisted ΔΣ ADC in 22nm Tri-Gate CMOS		C4-3 14:45-15:10 National Chiao Tung Univ.: A 28.6µW Mixed-Signal Processor for Epileptic Seizure Detection	JJ1-3 14:45-15:10 imec: Layout-Induced Stress Effects in 14nm & 10nm FinFETs and Their Impact on Performance	T9-3 14:45-15:10 LEAP: Novel Highly Scalable Multi-Level Cell for STT-MRAM with Stacked Perpendicular MTJs
	C5-4 15:10-15:35 National Taiwan Univ.: A 379nW 58.5dB SNDR VCO-Based ΔΣ Modulator for Bio-Potential Monitoring		C4-4 15:10-15:35 ETH Zurich: A 1024-Channel CMOS Microelectrode-Array System with 26'400 Electrodes for Recording and Stimulation of Electro- Active Cells In-Vitro	JJ1-4 15:10-15:35 IBM Micro-electronics: Process and Local Layout Effect Interaction on a High Performance Planar 20nm CMOS	T9-4 15:10-15:35 LEAP: Top-Pinned Perpendicular MTJ Structure with a Counter Bias Magnetic Field Layer for Suppressing a Stray-Field in Highly Scalable STT-MRAM
	C5-5 15:35-16:00 Oregon State Univ.: A 4.1mW, 12-bit ENOB, 5MHz BW, VCO-Based ADC with On-Chip Deterministic Digital Background Calibration in 90nm CMOS		C4-5 15:35-16:00 Hong Kong Univ. of Sci. and Tech.: A 51fA/Hz$^{0.5}$ Low Power Heterodyne Impedance Analyzer for Electrochemical Impedance Spectroscopy	JJ1-5 15:35-16:00 STARC: 0.5V Image Processor with 563 GOPS/W SIMD and 32bit CPU Using High Voltage Clock Distribution (HVCD) and Adaptive Frequency Scaling (AFS) with 40nm CMOS	T9-5 15:35-16:00 Renesas Electronics: Low-Current Domain Wa l l Mot ion MRAM with Perpendicularly Magnetized CoFeB/MgO Magnetic Tunnel Junction and Underlying Hard Magnets
16:10-17:50	**T10: More than Moore**		**C6: Application Specific Wireless Transceivers**	**(break)**	**T11: NAND and 3D NVM**
	T10-1 16:10-16:35 Univ. of California: Benefits of Segmented Si/SiGe p-Channel MOSFETs forAnalog/RF Applications		C6-1 16:10-16:35 Broadcom: A 2dB NF Receiver with 10mA Battery Current Suitable for Coexistence Applications	JJ1-6 16:10-16:35 **(Invited)** Intel Mobile Communications Group: **Design for ESD Protection at Its Limits**	T11-1 16:10-16:35 Macronix International: A Novel Bit Alterable 3D NAND Flash Using Junction-Free P-Channel Device with Band-to-Band Tunneling Induced Hot-Electron Programming
	T10-2 16:35-17:00 Toshiba: Scaling Strategy for Low Power RF Applications with Multi Gate Oxide Dual Work Function (DWF) MOSFETs Utilizing Self-Aligned Integration Scheme		C6-2 16:35-17:00 Mstar Semi-conductor: A Low-Cost SAW-Less GSM/GPRS SoC with Integrated Connectivity and 32-kHz Crystal Removal in 55nm	JJ1-7 16:35-17:00 Univ. of Tsukuba: Application of Low-Noise TIA ICs for Novel Sensing of MOSFET Noise up to the GHz Region	T11-2 16:35-17:00 Seoul National Univ: A New Read Method Suppressing Effect of Random Telegraph Noise in NAND Flash Memory by Using Hysteretic Characteristic
	T10-3 17:00-17:25 Samsung: Time of Flight Image Sensor with 7µm Pixel and 640x480 Resolution		C6-3 17:00-17:25 Panasonic: A 1.15V Low Power Mobile ISDB-Tsb/Tmm/T and DVB-T Tuner SoC in 40nm CMOS	JJ1-8 17:00-17:25 ST Micro-electronics: First Demonstration of a Full 28nm High-k/Metal Gate Circuit Transfer from Bulk to UTBB FDSOI Technology through Hybrid Integration	T11-3 17:00-17:25 Macronix International: Study of the Interference and Disturb Mechanisms of Split-Page 3D Vertical Gate (VG) NAND Flash and Optimized Programming Algorithms for Multi-Level Cell (MLC) Storage
	T10-4 17:25-17:50 Univ. of California: A MEMS-Based Charge Pump		C6-4 17:25-17:50 Intel: Two-Channel Receiver Back-End Using Statistically Calibrated HRM with >70dB 3rd and 5th Harmonic Rejection for Carrier Aggregation in 32nm CMOS	JJ1-9 17:25-17:50 ST Micro-electronics: 2.6GHz Ultra-Wide Voltage Range Energy Efficient Dual A9 in 28nm UTBB FD-SOI	T11-4 17:25-17:50 Stanford Univ.: 3D Vertical RRAM – Scaling Limit Analysis and Demonstration of 3D Array Operation
19:00-21:00				**Joint Banquet**	

2013 Symposia on VLSI Technology and Circuits June 13th (Thursday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
8:00-17:00	**Registration**				
8:30-10:10	**C7 "Plenary Session"** C7-1 8:45-9:25 (Plenary) Samsung: Perspectives on Mobile Devices and Their Impact on Semiconductor Technologies C7-2 9:25-10:05 (Plenary) Corning: Glass for the Future: Displays and Semiconductors				**T12: ReRAM 2** T12-1 8:30-8:55 imec: Understanding of the Intrinsic Characteristics and Memory Trade-Offs of Sub-μA Filamentary RRAM Operation T12-2 8:55-9:20 imec: RTN Insight to Filamentary Instability and Disturb Immunity in Ultra-Low Power Switching HfO_x and AlO_x RRAM T12-3 9:20-9:45 National Chiao Tung Univ.: Self-Rectifying Bipolar TaOx/TiO2 RRAM with Superior Endurance Over 1012 Cycles for 3D High-Density Storage- Class Memory T12-4 9:45-10:10 POSTECH: Multi-Layer Tunnel Barrier ($Ta_2O_5/TaO_x/TiO_2$) Engineering for Bipolar RRAM Selector Applications
10:30-12:35	**C8: Pipeline ADCs** C8-1 10:30-10:55 Broadcom: A 5.4GS/s 12b 500mW Pipeline ADC in 28nm CMOS C8-2 10:55-11:20 Oregon State Univ.: A 75.9dB-SNDR 2.96mW 29fJ/Conv-Step Ringamp-Only Pipelined ADC C8-3 11:20-11:45 Oregon State Univ: A 70MS/s 69.3dB SNDR 38.2fJ/Conversion-Step Time- Based Pipelined ADC C8-4 11:45-12:10 Stanford Univ.: A 12-Bit, 200-MS/s, 11.5-mW Pipeline ADC Using a Pulsed Bucket Brigade Front-End C8-5 12:10-12:35 Univ. of California: A 10-Bit 800-MHz 19-mW CMOS ADC		**T13: RTN** T13-1 10:30-10:55 Toshiba: Experimental Study of Channel Doping Concentration Impacts on Random Telegraph Signal Noise and Successful Noise Suppression by Strain Induced Mobility Enhancement T13-2 10:55-11:20 Beijing Univ.: Deep Understanding of AC RTN in MuGFETs through New Characterization Method and Impacts on Logic Circuits T13-3 11:20-11:45 Univ. of Minnesota: RTN Induced Frequency Shift Measurements Using a Ring Oscillator Based Circuit T13-4 11:45-12:10 imec: Degradation of Time Dependent Variability Due to Interface State Generation	**C9(JFS) Emerging Memories** C9-1 10:30-10:55 IBM T. J. Watson Research Center: 1Mb 0.41 μm^2 2T-2R Cell Nonvolatile TCAM with Two-Bit Encoding and Clocked Self-Referenced Sensing C9-2 10:55-11:20 Tohoku Univ.: Fabrication of a 99%-Energy-Less Nonvolatile Multi-Functional CAM Chip Using Hierarchical Power Gating for a Massively-Parallel Full-Text-Search Engine C9-3 11:20-11:45 Toshiba: A 250-MHz 256b-I/O 1-Mb STT-MRAM with Advanced Perpendicular MTJ Based Dual Cell for Nonvolatile Magnetic Caches to Reduce Active Power of Processors C9-4 11:45-12:10 Tohoku Univ.: A 1.5nsec/2.1nsec Random Read/Write Cycle 1Mb STT-RAM Using 6T2MTJ Cell with Background Write for Nonvolatile e-Memories C9-5 12:10-12:35 National Tsing Hua Univ.: Area-Efficient Embedded RRAM Macros with Sub-5ns Random-Read-Access-Time Using Logic-Process Parasitic-BJT- Switch (0T1R) Cell and Read-Disturb-Free Temperature-Aware Current-Mode Read Scheme	**T14: Process Technology** T14-1 10:30-10:55 imec: Highly Scalable Effective Work Function Engineering Approach for Multi-V_T Modulation of Planar and FinFET-Based RMG High-k Last Devices for (Sub-)22nm Nodes T14-2 10:55-11:20 imec: Heated Implantation with Amorphous Carbon CMOS Mask for Scaled FinFETs T14-3 11:20-11:45 GLOBAL FOUNDRIES: NFET Effective Work Function Improvement via Stress Memorization Technique in Replacement Metal Gate Technology T14-4 11:45-12:10 The Pennsylvania State Univ.: Barrier Height Reduction to 0.15eV and Contact Resistivity Reduction to 9.1×10^{-9} Ω-cm^2 Using Ultrathin TiO_{2-x} Interlayer between Metal and Silicon T14-5 12:10-12:35 ST Micro electronics: 64nm Pitch Interconnects: Optimized for Designability, Manufacturability and Extendibility
12:45-14:05		**Luncheon Talk** Otowa Electric: Symbiosis with Lightning Which Is One of the Most Spectacular Natural Phenomenon			
14:20-16:00	**C10: PLL Building Blocks** C10-1 14:20-14:45 KAIST: A 9b, 1.12ps Resolution 2.5b/Stage Pipelined Time-to- Digital Converter in 65nm CMOS Using Time-Register C10-2 14:45-15:10 Stanford Univ: A 0.11mm^2, 5.7-to-6.7GHz, Parametrically Pumped Quadrature LC-VCO with Digital Outputs C10-3 15:10-15:35 Keio Univ: A 720μW 873MHz-1.008GHz Injection-Locked Frequency Multiplier with 0.3V Supply Voltage in 90nm CMOS C10-4 15:35-16:00 STARC: 93% Power Reduction by Automatic Self Power Gating (ASPG) and Multistage Inverter for Negative Resistance (MINR) in 0.7V, 9.2μW, 39MHz Crystal Oscillator		**C11: Low Power Wireless** C11-1 14:20-14:45 imec: A 0.9V Low-Power 0.4-6GHz Linear SDR Receiver in 28nm CMOS C11-2 14:45-15:10 Texas Instruments: An Ultra Low Power, Reconfigurable, Multi-Standard Transceiver Using Fully Digital PLL C11-3 15:10-15:35 NTT Microsystem Integration Labs: Intermittent Transmitter Circuit with Novel Feedback Source Follower Amplifier for Solar Powered 5-mm-Cubic Wireless Sensor Nodes with 1/20λ Dipole Antenna C11-4 15:35-16:00 Purdue Univ.: A -90dBm Sensitivity Wireless Transceiver Using VCO-PA-LNA-Switch-Modulator Co-Design for Low Power Insect- Based Wireless Sensor Networks	**JJFS2: SRAM** JJ2-1 14:20-14:45 (Invited) IBM SRDC: Fully-Depleted Planar Technologies and Static RAM JJ2-2 14:45-15:10 Renesas Electronics: A 20nm 0.6V 2.1μW/MHz 128kb SRAM with No Half Select Issue by Interleave Wordline and Hierarchical Bitline Scheme JJ2-3 15:10-15:35 ST Micro-electronics: FDSOI Process/Design Full Solutions for Ultra Low Leakage, High Speed and Low Voltage SRAMs JJ2-4 15:35-16:00 LEAP: Ultralow-Voltage Operation of Silicon-on-Thin-BOX (SOTB) 2Mbit SRAM Down to 0.37 V Utilizing Adaptive Back Bias	**T15: Nanowire** T15-1 14:20-14:45 ST Micro electronics: Innovative Through-Si 3D Lithography for Ultimate Self-Aligned Planar Double-Gate and Gate-All-Around Nanowire Transistors T15-2 14:45-15:10 Toshiba: Systematic Understanding of Channel-Size Dependence of Low-Frequency Noise in 10nm-Diameter Tri-Gate Nanowire MOSFETs T15-3 15:10-15:35 CEA, LETI: Scaling of Ω-Gate SOI Nanowire N- and P-FET Down to 10nm Gate Length: Size- and Orientation-Dependent Strain Effects T15-4 15:35-16:00 National Chiao-Tung Univ.: Performance of GAA Poly-Si Nanosheet (2nm) Channel of Junctionless Transistors with Ideal Subthreshold Slope
16:15-18:20	**C12: Clock and Frequency Generation** C12-1 16:15-16:40 Oregon State Univ.: A 2.5GHz 5.4mW 1-to-2048 Digital Clock Multiplier Using a Scrambling TDC C12-2 16:40-17:05 Seoul National Univ.: A 1.3-mW, 1.6-GHz Digital Delay-Locked Loop with Two-Cycle Locking Time and Dither-Free Tracking C12-3 17:05-17:30 Broadcom: A 288fs RMS Jitter Versatile 8-12.4GHz Wide-Band Fractional-N Synthesizer for SONET and SerDes C12-4 17:30-17:55 Univ. of Minnesota: A 32nm, 0.9V Supply-Noise Sensitivity Tracking PLL for Improved Clock Data Compensation Featuring a Deep Trench Capacitor Based Loop Filter	**T17: Late News Session** T17-1 16:15-16:30 Univ. of California: Record Extrinsic Transconductance (2.45 mS/μm at V_{DS} = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ Channel MOSFETs Using MOCVD Source-Drain Regrowth T17-2 16:30-16:45 IBM Semi conductor: Experimental Analysis and Modeling of Self Heating Effect in Dielectric Isolated Planar and Fin Devices T17-3 16:45-17:00 Renesas Electronics: High-Voltage Complementary BEOL-FETs on Cu Interconnects Using N-type IGZO and P-type SnO Dual Oxide Semiconductor Channels	**C13: Linear Regulators and DC-DC Converters** C13-1 16:15-16:40 National Chiao Tung Univ.: A 0.6V Resistance-Locked Loop Embedded Digital Low Dropout Regulator in 40nm CMOS with 77% Power Supply Rejection Improvement C13-2 16:40-17:05 KAIST: High-Gain Wide-Bandwidth Capacitor-Less Low-Dropout Regulator with Zero Insertion Utilizing Frequency Response of Inner Loops C13-3 17:05-17:30 National Chiao Tung Univ.: A Pseudo-Noise Coded Constant-Off-Time (PNC-COT) Control Switching Converter with Maximum 18.7 dBm Peak Spur Reduction and 92% Efficiency in 40 nm CMOS C13-4 17:30-17:55 Univ. of Florida: A 10V Fully-Integrated Bidirectional SC Ladder Converter in 0.13μm CMOS Using Nested-Bootstrapped Switch Cells C13-5 17:55-18:20 Intel Corp.: A 0.45-1V Fully Integrated Reconfigurable Switched Capacitor Step-Down DC-DC Converter with High Density MIM Capacitor in 22nm Tri-Gate CMOS	**(break)** JJ2-5 16:15-16:40 (Invited) AIST: Enhancing SRAM Performance by Advanced FinFET Device and Circuit Technology Collaboration for 14nm Node and Beyond JJ2-6 16:40-17:05 Intel: Dual-V_{CC} 8T-Bitcell SRAM Array in 22nm Tri-Gate CMOS for Energy-Efficient Operation across Wide Dynamic Voltage Range JJ2-7 17:05-17:30 National Nano Device Labs.: A 10 nm Si-Based Bulk FinFETs 6T SRAM with Multiple Fin Heights Technology for 25% Better Static Noise Margin JJ2-8 17:30-17:55 National Tsing Hua Univ.: A 210mV 7.3MHz 8T SRAM with Dual Data-Aware Write-Assists and Negative Read Wordline for High Cell- Stability, Speed and Area-Efficiency JJ2-9 17:55-18:20 Intel: A 22nm 2.5MB Slice On-Die L3 Cache for the Next Generation Xeon® Processor	**T16: Beyond CMOS** T16-1 16:15-16:40 GNC: Synthetic Electric Field Tunnel FETs: Drain Current Multiplication Demonstrated by Wrapped Gate Electrode Around Ultrathin Epitaxial Channel T16-2 16:40-17:05 Panasonic: Neural Network Based on a Three-Terminal Ferroelectric Memristor to Enable On-Chip Pattern Recognition T16-3 17:05-17:30 Samsung: Performance of Threshold Switching in Chalcogenide Glass for 3D Stackable Selector T16-4 17:30-17:55 LEAP: Bidirectional TaO-Diode-Selected, Complementary Atom Switch (DCAS) for Area-Efficient, Nonvolatile Crossbar Switch Block
20:00-22:00	**Circuits Rump Session 1** **The Best Logic and Memory Interface Technology for 2D/2.5D/3D Ics**		**Circuits Rump Session 2** **Analog Designer's Play-Ground Beyond 20nm, Is it Circuit Physics or Auto Place & Route?**		

2013 Symposia on VLSI Technology and Circuits June 14th (Friday)

Time	Suzaku I	Suzaku II	Suzaku III	Shunju I	Shunju II
8:00-15:00	**Circuits Registration**				
8:30-10:10	**C14: Image Processing**	**C15: All Digital Phase-Locked Loops**	**C16: Embedded Non-Volatile Memory**		
	C14-1 8:30-8:55	C15-1 8:30-8:55	C16-1 8:30-8:55		
	The Univ. of Manchester — A 100,000 fps Vision Sensor with Embedded 535GOPS/W 256x256 SIMD Processor Array	Broadcom — An 8.5 mW, 0.07 mm^2 ADPLL in 28 nm CMOS with Sub-ps Resolution TDC and < 230 fs RMS Jitter	Texas Instruments — A MCU Platform with Embedded FRAM Achieving 350nA Current Consumption in Real-Time Clock Mode with Full State Retention and 6.5μs System Wakeup Time		
	C14-2 8:55-9:20	C15-2 8:55-9:20	C16-2 8:55-9:20		
	KAIST — A 125,582 Vector/s Throughput and 95.1% Accuracy ANN Searching Processor with Neuro-Fuzzy Vision Cache for Real-Time Object Recognition	Univ. of Twente — A 12GHz 210fs 6mW Digital PLL with Sub-Sampling Binary Phase Detector and Voltage-Time Modulated DCO	ADESTO Technologies — A 0.6V 8 pJ/write Non-Volatile CBRAM Macro Embedded in a Body Sensor Node for Ultra Low Energy Applications		
	C14-3 9:20-9:45	C15-3 9:20-9:45	C16-3 9:20-9:45		
	Univ. of Zurich — A 240x180 10mW 12us Latency Sparse-Output Vision Sensor for Mobile Applications	Rambus — A 25GHz 100ns Lock Time Digital LC PLL with an 8-Phase Output Clock	Toshiba — A 38% Access Time Improvement in 40nm CMOS Technology with Triple-Wire-Program-Cell Scheme for High Density MROM		
	C14-4 9:45-10:10	C15-4 9:45-10:10	C16-4 9:45-10:10		
	National Taiwan Univ. — A 1062Mpixels/s 8192x4320p High Efficiency Video Coding (H.265) Encoder Chip	IBM T. J. Watson Research — A 28GHz Hybrid PLL in 32nm SOI CMOS	TSMC — A 28nm ROM with Two-Step Decoding Scheme and OD-Space-Effect Minimization to Achieve 30% Speed and 190mV Vmin Improvement		
10:30-12:35	**C17: Sensors**	**C18: Power Management Techniques**	**C19: Clocking and Memory Interface**		
	C17-1 10:30-10:55	C18-1 10:30-10:55	C19-1 10:30-10:55		
	Princeton Univ. — A Fully Self-Powered Hybrid System Based on CMOS Ics and Large-Area Electronics for Large-Scale Strain Monitoring	National Tsing Hua Univ. — An RF Energy Harvester with 35.7% PCE at P_{IN} of –15 dBm	KAIST — A 12Gb/s 0.92mW/Gb/s Forwarded Clock Receiver Based on ILO with 60MHz Jitter Tracking Bandwidth Variation Using Duty Cycle Adjuster in 65nm CMOS		
	C17-2 10:55-11:20	C18-2 10:55-11:20	C19-2 10:55-11:20		
	Texas Instruments — A ±0.4°C Accurate High-Speed Remote Junction Temperature Sensor with Digital Beta Correction and Series-Resistance Cancellation in 65nm CMOS	Delft Univ. of Tech. — A Self-Calibrating RF Energy Harvester Generating 1V at -26.3 dBm	Fujitsu Labs. — An 8-to-16GHz 28nm CMOS Clock Distribution Circuit Based on Mutual-Injection-Locked Ring Oscillators		
	C17-3 11:20-11:45	C18-3 11:20-11:45	C19-3 11:20-11:45		
	KAIST — A 70dB SNR Capacitive Touch Screen Panel Readout IC Using Capacitor-Less Trans-Impedance Amplifier and Coded Orthogonal Frequency-Division Multiple Sensing Scheme	Univ. of Michigan — A Ripple Voltage Sensing MPPT Circuit for Ultra-Low Power Microsystems	Samsung — A Sub-1.0V 20nm 5Gb/s/pin Post-LPDDR3 I/O Interface with Low Voltage-Swing Terminated Logic and Adaptive Calibration Scheme for Mobile Application		
	C17-4 11:45-12:10	C18-4 11:45-12:10	C19-4 11:45-12:10		
	KAIST — An Integrated Pulse Wave Velocity Sensor Using Bio-Impedance and Noise-Shaped Body Channel Communication	Hanyang Univ. — A 6.0-W Bi-Directional DC-DC Converter for Wireless Power Transceiver in 0.35-μm BCDMOS	Samsung — A Heterogeneous Dual DLL and Quantization Error Minimized ZQ Calibration for 30nm 1.2V 4Gb 3.2Gb/s/pin DDR4 SDRAM		
	C17-5 12:10-12:35	C18-5 12:10-12:35	C19-5 12:10-12:35		
	Columbia Univ. — Integrated CMOS Quantitative Polymerase Chain Reaction Lab-on-Chip	Texas Instruments — A Stackable, 6-Cell, Li-Ion, Battery Management IC for Electric Vehicles with 13, 12-bit ΣΔ ADCs, Cell Balancing, and Direct-Connect Current-Mode Communications	Rambus — A 400MHz - 1.6GHz Fast Lock, Jitter Filtering ADDLL Based Burst Mode Memory Interface		
13:55-16:00	**C20: Medical Processing**	**C21: Nyquist Converters**	**C22: Wireline Transceivers**		
	C20-1 13:55-14:20	C21-1 13:55-14:20	C22-1 13:55-14:20		
	National Taiwan Univ. — A Self-Powered CMOS Reconfigurable Multi-Sensor SoC for Biomedical Applications	IBM Research — A 35mW 8 b 8.8 GS/s SAR ADC with Low-Power Capacitive Reference Buffers in 32 nm Digital SOI CMOS	Texas A&M Univ. — A 10 Gb/s 2-IIR-Tap DFE Receiver with 35 dB Loss Compensation in 65-nm CMOS		
	C20-2 14:20-14:45	C21-2 14:20-14:45	C22-2 14:20-14:45		
	Princeton Univ — A Low-Power Microprocessor for Data-Driven Analysis of Analytically-Intractable Physiological Signals in Advanced Medical Sensors	Broadcom — A 13-Bit 9GS/s RF DAC-Based Broadband Transmitter in 28nm CMOS	Texas A&M Univ. — A 6b 10GS/s TI-SAR ADC with Embedded 2-Tap FFE/1- Tap DFE in 65nm CMOS		
	C20-3 14:45-15:10	C21-3 14:45-15:10	C22-3 14:45-15:10		
	National Chiao Tung Univ. — A 48.6-to-105.2μW Machine-Learning Assisted Cardiac Sensor SoC for Mobile Healthcare Monitoring	Carnegie Mellon Univ. — An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI	Broadcomp — A 2.8 mW/Gb/s Quad-Channel 8.5-11.4 Gb/s Quasi-Digital Transceiver in 28 nm CMOS		
	C20-4 15:10-15:35	C21-4 15:10-15:35	C22-4 15:10-15:35		
	National Chung Cheng Univ. — A 0.36V, 33.3μW 18-Band ANSI S1.11 1/3-Octave Filter Bank for Digital Hearing Aids in 40nm CMOS	Keio Univ. — A 0.0058mm^2 7.0 ENOB 24MS/s 17fJ/conv. Threshold Configuring SAR ADC with Source Voltage Shifting and Interpolation Technique	Oregon State Univ. — A 5Gb/s 2.6mW/Gb/s Reference-Less Half-Rate PRPLL-Based Digital CDR		
	C20-5 15:35-16:00	C21-5 15:35-16:00	C22-5 15:35-16:00		
	National Taiwan Univ. — A 401GFlops/W 16-Cores Signal Reconstruction Platform with a 4G Entries/s Matrix Generation Engine for Compressed Sensing and Sparse Representation	imec — A 2.1 mW 11b 410 MS/s Dynamic Pipelined SAR ADC with Background Calibration in 28nm Digital CMOS	Oregon State Univ. — A Fast Power-On 2.2Gb/s Burst-Mode Digital CDR with Programmable Input Jitter Filtering		
16:15-17:55	**C23: Embedded Processing**	**C24: Millimeter Wave Transceivers and**			
	C23-1 16:15-16:40	C24-1 16:15-16:40			
	ETH Zurich — A 1Gbps LTE-Advanced Turbo-Decoder ASIC in 65nm CMOS	National Taiwan Univ. — A Fully-Integrated 77GHz Phase-Array Radar System with 1TX/4RX Frontend and Digital Beamforming Technique			
	C23-2 16:40-17:05	C24-2 16:40-17:05			
	Waseda Univ — A 1.59Gpixel/s Motion Estimation Processor with -211-to- 211 Search Range for UHDTV Video Encoder	Hong Kong Univ. of Sci. &Tech. — A 4-Element 60-GHz CMOS Phased-Array Receiver with Transformer-Based Hybrid-Mode Mixing and Closed- Loop Beam-Forming Calibration			
	C23-3 17:05-17:30	C24-3 17:05-17:30			
	NTT Microsystem Integration Labs. — A 96.5% Energy-Reduced Lookup Engine with an Unused-Rules-Exception Scheme for Greening Networks	Texas Instruments — 160GHz Pulsed Transmitter with Packaged Antenna Array in 65nm CMOS			
	C23-4 17:30-17:55	C24-4 17:30-17:55			
	Univ. of Michigan — Shortstop: An On-Chip Fast Supply Boosting Technique	Univ. of California — A Low-Power 60-GHz CMOS Transceiver for WiGig Applications			