2013 VLSI TECHNOLOGY SYMPOSIUM KYOTO

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SECOND ANNOUNCEMENT AND CALL FOR PAPERS

Sponsored by the Japan Society of Applied Physics and the IEEE Electron Devices Society
in Cooperation with the IEEE Solid-State Circuits Society

2013 SYMPOSIUM ON VLSI TECHNOLOGY

Rihga Royal Hotel Kyoto, Kyoto, Japan
Monday - Thursday, June 10- 13, 2013
(June 10 Short Course, June 11 - 13 Technical Sessions)

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David Scott (USA)
DBS

Local Arrangements:
Masao Ito (Japan)
Renesas Electronics Corporation

Short Course Organizers:
Masami Hane (Japan)
Renesas Electronics Corporation

Geoffrey Yeap (USA)
Qualcomm

The 2013 Symposium on VLSI Technology welcomes the submission of original papers on all aspects of IC technology. The 2013 Symposium on VLSI Circuits (please see the reverse side) will be held at the same location, with two days of overlap, to facilitate synergistic interactions among participants in areas of joint interest. **A single registration fee allows participants to attend both of the Symposia.**

CONFERENCE SCOPE

- New concepts and breakthroughs in VLSI processes and devices including Memory, Logic, I/O, RF, Analog, Mixed-Signal, High-Voltage, Imager, and MEMS.
- Advanced gate stacks and interconnects in VLSI processes and devices
- Advanced lithography and fine-patterning technologies for high-density VLSI
- New functional devices beyond CMOS with a path for VLSI implementation
- Packing of VLSI devices including 3D-system integration
- Advanced device analysis, materials and modeling for VLSIs
- Reliability related to the above devices
- Theories and fundamentals related to the above devices
- New concepts and technologies for VLSI manufacturing
- Heterogeneous integration of non-Si substrates/materials on Si substrate

JOINT TECHNOLOGY AND CIRCUITS FOCUS SESSIONS

Joint technology and circuits focus sessions comprising invited and contributed papers will be offered in special areas of joint interest. Paper submissions highlighting **major innovations and advances in materials, processes, devices, integration, reliability and modeling** are strongly encouraged. The scope includes, but not limited to the following areas;

- **Design enablement including co-optimization and BEOL RC:** Impact of advanced device & interconnect materials or structures on digital circuit performance, power, density; device design & process/technology optimization for analog/mixed-signal circuits. Scaling of RC delay in future BEOL technology.
- **SRAM:** Cell size scaling, cell layout with 3D-transistors, static noise margin, V_{DDmin} improvement, reliability, ultra-low voltage/power operation.
- The following two sessions are planned as technology focus sessions, not as joint focus sessions.**3D-system and packaging:** 3D-packaging technologies and system co-optimization; power delivery and management; thermal management; inter-chip communications, test issues.
- **Emerging Memory:** novel RAM and NVRAM technology including 3D, atomic switch, phase change & RRAM.

SUBMISSION OF PAPERS

Prospective authors must upload their submission of a two-page camera-ready paper and a 150-word-abstract to www. vlsi symposium.org. The technical content beyond the 150-word-abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium. For details, please refer to the Author's Guide in the above website.

Paper Submission Deadline is 11:59 P.M. JST (2:59 P.M. GMT), January 21, 2013

BEST STUDENT PAPER AWARD

The student paper award selection will be based upon the quality of the paper and the presentation. The student who receives the Best Student Paper Award will be presented a financial prize and a certificate at the opening session of the 2014 Symposium. For a paper to be reviewed for this Award, the student must be the leading author and the presenter of the paper, and must indicate in the web submission form that the paper is a student paper.

LATE NEWS

In the 2013 Symposium on VLSI Technology, we invite you to submit late news abstracts announcing very recent results with high impact. **Deadline for the late news submission is March 26, 2013.** Note that only a very limited number of top quality late news papers will be accepted. Submission procedure will be announced on the 2013 VLSI Symposia website.

VLSI TECHNOLOGY SHORT COURSE

A one-day short course will be held on June 10, 2013. Details will be given in the VLSI Technology Symposium Advance Program, which will be posted on the web by the middle of April, 2013.

SATELLITE WORKSHOPS

The 2013 Silicon Nanoelectronics Workshop will be held on June 9-10, 2013 as a satellite workshop at the same location where Symposium takes place. In addition, the 2013 Spintronics Workshop focusing on VLSI-implementable Spintronics Technology will be held on June 10, 2013 also at the same location.

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