2014 Symposia on VLSI Technology and Circuits - Technology Short Course - June 9 Monday	SiNanoElectronics Workshop- Jun 8-9, Sunday / Monday	

2014 Symposia on VLSI Technology and Circuits June 10th - Tuesday

Time	Honolulu 1	Honolulu 2-3	Tapa I	Tapa II	Tapa III
7:30 am - 5:00 pm - Registration					
8:05-10:05	Circuits SC	Circuits SC	Technology Plenary and Welcome		
	8:30 am - 5:00 pm	8:30 am - 5:00 pm	8:05 am - 8:35 am: Welcome and Opening Remarks		
			T1-1: 8:35 a.m.-9:20 a.m.		
			ARM: Device and Technology Implications of the Internet of Things		
			T1-2: 9:20 am-10:05 a.m.		
			SONY: Customer Value Creation in the Information Explosion Era		
10:20 am -12:00 pm			T2: Highlights		
			T2-1: 10:20 am - 10:45 am		
			SONY: A Novel Curved CMOS Image Sensor Integrated with Imaging System		
			T2-2: 10:45 am - 11:10 am		
			IBM: A 10nm Platform Technology for Low Power and High Performance Application Featuring FINFET Devices with Multi Workfunction Gate Stack on Bulk and SOI		
			T2-3: 11:10 am - 11:35 am		
			STMicro: 14nm FDSOI Technology for High Speed and Energy Efficient Applications		
			T2-4: 11:35 am - 12:00 pm		
			IBM: Strained Si1-xGex-on-Insulator PMOS FinFETs with Excellent Sub-Threshold Leakage, Extremely-High Short-Channel Performance and Source Injection Velocity for 10nm Node and Beyond		
1:30 pm-5:30 pm			T3: 3D Memory & Emerging Devices I	T4: Advanced CMOS Technology I - *III-V Channels*	
			T3.1: 1:30 p.m.-1:55 p.m.	T4.1: 1:30 p.m.-1:55 p.m.	
			Macronix: Study of the Impact of Charge-Neutrality Level (CNL) of Grain Boundary Interface Trap on Device Variability and P/E Cycling Endurance of 3D NAND Flash Memory	IMEC: An InGaAs/InP Quantum Well FinFet Using the Replacement Fin Process Integrated in an RMG Flow on 300mm Si Substrates	
			T3.2: 1:55 p.m.-2:20 p;m	T4.2: 1:55 p.m.-2:20 p;m	
			imec: Laser Thermal Anneal of polysilicon channel to boost 3D memory performance	The Univ. of Tokyo: III-V single structure CMOS by using ultrathin body InAs/GaSb-OI channels on Si	
			T3.3: 2:20 p.m.-2:45 p.m.	T4.3: 2:20 p.m.-2:45 p.m.	
			Tokyo Inst. Tech.: Ultra Thinning down to 4-um using 300-mm Wafer proven by 40-nm Node 2Gb DRAM for 3D Multi-stack WOW Applications	KANC: Sub-100 nm Regrown S/D Gate-Last In0.7Ga0.3As QW MOSFETs with mobility > 5,500 cm2/V-s	
			T3.4: 2:45 p.m.-3:10 p.m.	T4.4: 2:45 p.m.-3:10 p.m.	
			Seoul Nat'l Univ.: Effect of Traps on Transient Bit-line Current Behavior in Word-line Stacked NAND Flash Memory with Poly-Si Body	The Univ. of Tokyo: High Performance InGaAs-On-Insulator MOSFETs on Si by Novel Direct Wafer Bonding Technology applicable to Large Wafer Size Si	
			T5: Focus - Embedded NVM	T6: Process Technology I	
			T5.1: 3:25 p.m.-3:50 p.m.	T6.1: 3:25 p.m.-3:50 p.m.	
			eMemory: A High-Density Logic CMOS Process Compatible Non-Volatile Memory for Sub-28nm Technologies	IBM Research: Simple Gate Metal Anneal (SIGMA) Stack for FinFET Replacement Metal Gate toward 14nm and beyond	
			T5.2: 3:50 p.m. - 4:15 p.m.	T6.2: 3:50 p.m. - 4:15 p.m.	
			Qualcomm: Embedded STT-MRAM for Energy-efficient and Cost-effective Mobile Systems	imec: Highly Scalable Bulk FinFET Devices with Multi-VT Options by Conductive Metal Gate Stack Tuning for the 10-nm Node and Beyond	
			T5.3: 4:15 p.m.-4:40 p.m.	T6.3: 4:15 p.m.-4:40 p.m.	
			Toshiba: Flash-Based Nonvolatile Programmable Switch for Low-Power and High-Speed FPGA by Adjacent Integration of MONOS/Logic and Novel	imec: Performance and Reliability of High-Mobility Si0.55Ge0.45 p-Channel FinFETs based on Epitaxial Cladding of Si Fins	
			T5.4: 4:40 p.m.-5:05 p.m.	T6.4: 4:40 p.m.-5:05 p.m.	
			GLOBALFOUNDRIES: Anti-Fuse Memory Array Embedded in 14nm FinFET CMOS with Novel Selector-Less Bit-Cell Featuring Self-Rectifying Characteristics	Purdue Univ.: III-V CMOS Devices and Circuits with High-Quality Atomic-Layer-Epitaxial La2O3/GaAs Interface	
			T5.5: 5:05 p.m.-5:30 p.m.	T6.5: 5:05 p.m.-5:30 p.m.	
			TDK: Demonstration of fully functional 8Mb perpendicular STT-MRAM chips with sub-5ns writing for non-volatile embedded memories	Tokyo Electron: A Novel Metallic Complex Reaction Etching for Transition Metal and Magnetic Material by Low-temperature and Damage-free Neutral Beam Process for Non-volatile MRAM Device Applications	
				T6.6: 5:30 p.m.-5:55 p.m.	
	Joint Reception - 6:30 pm - 7:30 pm		Joint Rump Session and Technology Rump Session - 8:00 pm - 10:00 pm	Univ. CA, Santa Barbara: Record Ion (0.50 mA/μm at VDD = 0.5 V and Ioff = 100 nA/μm) 25 nm-Gate-Length ZrO2/InAs/InAlAs MOSFETs	

2014 Symposia on VLSI Technology and Circuits June 11th - Wednesday

7:30 am - 5:00 pm - Registration

8:05-10:05

Honolulu Suite — T8: Beyond CMOS

T8.1	8:05 a.m.-8:30 a.m.
CEA LETI	First Demonstration of Strained SiGe Nanowires TFETs with Ion beyond 700μA/μm
T8.2	8:30 a.m.-8:55 a.m.
GNC-AIST	Band-to-Band Tunneling Current Enhancement Utilizing Isoelectronic Trap and its Application to TFETs
T8.3	8:55 a.m.-9:20 a.m.
Peking Univ.	Deep Insights into Low Frequency Noise Behavior of Tunnel FETs with Source Junction Engineering
T8.4	9:20 a.m.
Penn State	Inv. of InxGa1-xAs FinFET Architecture with Varying Indium (x) Concentration and Quantum Confinement
T8.5	9:45 a.m.-10:05 a.m.
L'-John Moores	Time-dependent variation: A new defect-based prediction methodology

Tapa I — T7: Memory Technology - Emerging Memory

T7.1	8:05 a.m.-8:30 a.m.
Nat'l Taiwan U	Paper Memory by All Printing Technology
T7.2	8:30 a.m.-8:55 a.m.
LEAP	A Highly Scalable STT-MRAM fabricated by a Novel Technique for Shrinking a Magnetic Tunnel Junction with reducing Processing Damage
T7.3	8:55 a.m.-9:20 a.m.
Samsung Electr.	Verification on the extreme scalability of STT-MRAM without loss of thermal stability below 15 nm MTJ cell
T7.4	8:55 a.m.-9:20 a.m.
Infineon Tech.	Comprehensive Statistical Investigation of STT-MRAM Thermal Stability
T7.5	9:45 a.m.-10:05 a.m.
Micron	A Copper ReRAM Cell for Storage Class Memory Applications

Tapa II — C1: Plenary and Welcome

8:05 am - 8:35 am	Welcome and Opening Remarks
C1.1	8:35 a.m. - 9:20 a.m.
Micron	DataCenter 2020: Near-memory Acceleration for Data-oriented Applications
T1-2	9:20 am- 10:05 a.m.
The Univ. Tokyo	Technology Development for Printed LSIs Based on Organic Semiconductors

Tapa III

10:20 am -12:05 pm

Honolulu Suite — C3: Power Mgt for Wireless Sensor Nodes

C3.1	10:25 a.m.-10:50 a.m.
Univ. of Michigan	Low Power Battery Supervisory Circuit with Adaptive Battery Health Monitor
C3.2	10:50 a.m.-11:15 a.m.
Texas Instr./Univ. of VA	A 1.2μW SIMO Energy Harvesting and Power Management Unit with Constant Peak Inductor Current Control Achieving 84-92% Efficiency Across Wide Input and Output Voltages
C3.3	11:15 a.m.-11:40 a.m.
Nt'l Chia Tung	A Direct AC-DC and DC-DC Cross-Source Energy Harvesting Circuit with Analog Iterating-Based MPPT Technique with 72.5% Conversion Efficiency and 94.6% Tracking Efficiency
C3.4	11:40 a.m.-12:05 a.m.
HKUST	A 13.56MHz Wireless Power Transfer System with Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices

Tapa I — C2: Ultra-High-Speed Wireline Transceivers

C2.1	10:25 a.m.-10:50 a.m.
Fujitsu	A 36 Gbps 16.9 mW/Gbps Transceiver in 20-nm CMOS with 1-tap DFE and Quarter-Rate Clock Distribution
C2.2	10:50 a.m.-11:15 a.m.
Broadcom	A Quad-Channel 112-128 Gb/s Coherent Transmitter in 40 nm CMOS
C2.3	11:15 a.m.-11:40 a.m.
Rambus	A 40-Gb/s Serial Link Transceiver in 28-nm CMOS Technology
C2.4	11:40 a.m.-12:05 a.m.
Rambus, Univ. of Alberta	A 4x40 Gb/s Quad-Lane CDR with Shared Frequency Tracking and Data Dependent Jitter Filtering

Tapa II — T9: Advance CMOS Technology III-Ge Devices

T9.1	10:25 a.m.-10:50 a.m.
Purdue Univ.	Ge CMOS: Breakthroughs of nFETs (Imax=714 mA/mm, gmax=590 mS/mm) by recessed channel and S/D
T9.2	10:50 a.m.-11:15 a.m.
NTU	The demonstration of colossal magneto-capacitance and "negative" capacitance effect with the promising characteristics of Jg-EOT and transistor's performance on Ge (100) n-FETs by the novel magnetic gate stack scheme design
T9.3	11:15 a.m.-11:40 a.m.
Chongqing Univ.	Undoped Ge0.92Sn0.08 Quantum Well PMOSFETs on (001), (011) and (111) Substrates with In Situ Si2H6 Passivation: High Hole Mobility and Dependence of Performance on Orientation
T9.4	11:40 a.m.-12:05 a.m.
KAIST	Demonstration of Ge pMOSFETs with 6 Å EOT using TaN/ZrO2/Zr-cap/n-Ge(100) Gate Stack Fabricated by Novel Vacuum Annealing and in-situ Metal Capping Method

Tapa III — T10: Design Technology Co-Optimization I

T10.1	10:25 a.m.-10:50 a.m.
G'Foundries	Analog, RF, and ESD Device Challenges and Solutions for 14nm FinFET Technology and Beyond
T10.2	10:50 a.m.-11:15 a.m.
Qualcomm	Novel Critical Path Aware Transistor Optimization for Mobile SoC Device-Circuit Co-design
T10.3	11:15 a.m.-11:40 a.m.
imec	Group IV channels for 7nm FinFETs: Performance for SoCs Power and Speed Metrics
T10.4	11:40 a.m.-12:05 a.m.
Qualcomm	High Performance Mobile SoC Design and Technology Co-Optimization to Mitigate High-K Metal Gate Process Induced Variations

1:30 pm-5:30 pm

Honolulu Suite — C5: Advanced ADC Techniques

C5.1	1:30 p.m. - 1:55 p.m.
Analog Devices	An 18 b 5 MS/s SAR ADC with 100.2 dB Dynamic Range
C5.2	1:55 p.m.- 2:20 p.m.
Nat'l Tsing Hua U.	A 0.4V 2.02fJ/Conversion-step 10-bit Hybrid SAR ADC with Time-domain Quantizer in 90nm CMOS
C5.3	2:20 p.m. - 2:45 p.m.
Oregon State	A 48 fJ/CS, 74 dB SNDR, 87 dB SFDR, 85 dB THD, 30 MS/s Pipelined ADC Using Hybrid Dynamic Amplifier
C5.4	2:45 p.m.- 3:10 p.m.
Keio Univ.	7-bit 0.8-1.2GS/s Dynamic Architecture and Frequency Scaling Subrange ADC with Binary-Search/Flash Live Configuration Technique

Tapa I — T11: 3D Memory & Emerging Devices - 2

T11.1	1:30 p.m. - 1:55 p.m.
Macronix	A Double-density Dual-mode Phase Change Memory Using a Novel Background Storage Scheme
T11.2	1:55 p.m.- 2:20 p.m.
Macronix	Towards the Integration of both ROM and RAM Functions Phase Change Memory Cells on a Single Die for System-On-Chip (SOC) Applications
T11.3	2:20 p.m. - 2:45 p.m.
Chuo Univ.	23% Faster Program and 40% Energy Reduction of Carbon Nanotube Non-volatile Memory with Over 10^11 Endurance
T11.4	2:45 p.m.- 3:10 p.m.
KAIST	Surface-controlled Ultrathin (2 nm) Poly-Si Channel Junctionless FET towards 3D NAND Flash Memory Applications

Tapa II — C4: 3D Circuits and Applications (JFS)

C4.1	1:30 p.m. - 1:55 p.m.
Samsung	Design Technologies for a 1.2V 2.4Gb/s/pin High Capacity DDR4 SDRAM with TSVs
C4.2	1:55 p.m.- 2:20 p.m.
SK Hynix	An Exact Measurement and Repair Circuit of TSV Connections for 128GB/s High-Bandwidth Memory(HBM) Stacked DRAM
C4.3	2:20 p.m. - 2:45 p.m.
Keio Univ.	A 352Gb/s Inductive-Coupling DRAM/SoC Interface Using Overlapping Coils with Phase Division Multiplexing and Ultra-Thin Fan-Out Wafer Level Package
C4.4	2:45 p.m.- 3:10 p.m.
TSMC	A peripheral switchable 3D stacked CMOS image sensor

Tapa III — T12: Devices Physics & Reliability I

T12.1	1:30 p.m. - 1:55 p.m.
IBM	Spatial Mapping of Non-Uniform Time-to-Breakdown and Physical Evidence of Defect Clustering
T12.2	1:55 p.m.- 2:20 p.m.
NIST	Device-Level PBTI-induced Timing Jitter Increase in Circuit-Speed Random Logic Operation
T12.3	2:20 p.m. - 2:45 p.m.
IBM	Physics Based PBTI Model for Accelerated Estimation of 10 Year Lifetime
T12.4	2:45 p.m.- 3:10 p.m.
Nat'l Chiao Tung U.	The Experimental Demonstration of the BTI-Induced Breakdown Path in 28nm High-k Metal Gate Technology CMOS Devices

Honolulu Suite — C7: Sensor Node Radios

C7.1	3:25 p.m. - 3:50 p.m.
UC Berkeley	A Power-Harvesting Pad-Less mm-Sized 24/60GHz Passive Radio with On-Chip Antennas
C7.2	3:50 p.m. - 4:15 p.m.
Univ. of CA	Energy-Recycling Integrated 6.78-Mbps Data 6.3-mW Power Telemetry over a Single 13.56-MHz Inductive Link
C7.3	4:15 p.m. - 4:40 p.m.
Panasonic	An Ultra-Low-Power 2-step Wake-Up Receiver for IEEE 802.15.4g Wireless Sensor Networks
C7.4	4:40 p.m. - 5:05 p.m.
N.Taiwan U	A 400MHz 10Mbps D-BPSK Receiver with a Reference-less Dynamic Phase-to-Amplitude Demodulation Technique
C7.5	5:05 p.m. - 5:30 p.m.
Oregon State	A 915MHz, 6Mb/s, 80pJ/b BFSK Receiver with -76dBm Sensitivity for High Data Rate Wireless Sensor Networks

Tapa I — C6: Design with Emerging Technologies

C6.1	3:25 p.m. - 3:50 p.m.
Intel	A 2GHz-to-7.5GHz Quadrature Clock Generator Using Digital Delay Locked Loops for Multi-Standard I/Os in 14nm CMOS
C6.2	3:50 p.m. - 4:15 p.m.
TSMC	A 0.7V Resistive sensor with temperature_voltage detection function in 16nm FinFet technologies
C6.3	4:15 p.m. - 4:40 p.m.
MIT	A Monolithically Integrated Chip-to-Chip Optical Link in Bulk CMOS
C6.4	4:40 p.m. - 5:05 p.m.
MIT	A Monolithically-Integrated Optical Transmitter and Receiver in a Zero-Change 45nm SOI Process
C6.5	5:05 p.m. - 5:30 p.m.
Semi. Energy Lab	A 32-bit CPU with Zero Standby Power and 1.5-clock Sleep/2.5-clock Wake-up Achieved by Utilizing a 180-nm C-axis Aligned Crystalline In-Ga-Zn Oxide Transistor

Tapa II — T14: 3D Systems & Packaging (JFS)

T14.1	3:25 p.m. - 3:50 p.m.
Xilinx	Applying a Redundancy Scheme to Address Post-assembly Yield Loss in 3D FPGAs
T14.2	3:50 p.m. - 4:15 p.m.
Skhynix	TSV Technology and Challenges for 3D Stacked DRAM
T14.3	4:15 p.m. - 4:40 p.m.
TSMC	A High-Performance Low-Cost Chip-on-Wafer Package with Sub-μm Pitch Cu RDL
T14.4	4:40 p.m. - 5:05 p.m.
Georgia Tech	Low-loss Silicon Interposer for Three-dimensional System Integration with Embedded Microfluidic Cooling
T14.5	5:05 p.m. - 5:30 p.m.
Macronix	A Novel Capacitive-coupled Floating Gate Antenna Protection Design and Its Application to Prevent In-Process Charging Effects for 3D NAND Flash Memory

Tapa III — T13: Advanced CMOS Technology II - FinFET

T13.1	3:25 p.m. - 3:50 p.m.
IBM	Bottom Oxidation through STI (BOTS) - A Novel Approach to Fabricate Dielectric Isolated FinFETs on Bulk Substrates
T13.2	3:50 p.m. - 4:15 p.m.
imec	15nm-WFIN High-Performance Low-Defectivity Strained-Germanium pFinFETs With Low Temp STI-Last Process
T13.3	4:15 p.m. - 4:40 p.m.
Globalf	Advanced RMG module to improve AC/DC performance for 14nm FinFETs and beyond
T13.4	4:40 p.m. - 5:05 p.m.
AIST	Lowest Variability SOI FinFETs Having Multiple Vt by Back-Biasing
T13.5	5:05 p.m. - 5:30 p.m.
U-. of Tokyo	Thermally Robust CMOS-aware Ge MOSFETs with High Mobility at High-carrier Densities on a Single Orientation Ge Substrate
T13.6	5:30 p.m.-6:05 p.m.
GNC-AIST	Demonstration of Ultimate CMOS based on 3D Stacked InGaAs-OI/SGOI Wire Channel MOSFETs with

Joint Banquet 7:00 pm - 9:00 pm

2014 Symposia on VLSI Technology and Circuits June 12th Thursday

Time	Honolulu Suite		Tapa I		Tapa II		Tapa III	
	7:30 am - 5:00 pm - Registration							
	C9: Phase-Locked Loops		**C8: Signal Processing**		**T15: Memory Technology - RRAM I**		**T16: Focus Session - Interconnect**	
8:05 a.m-10:05 a.m.	C9.1	8:05 a.m. - 8:30 a.m.	C8.1	8:05 a.m. - 8:30 a.m.	T15.1	8:05 a.m. - 8:30 a.m.	T16.1	8:05 a.m. - 8:30 a.m.
	Broadcom	A 2.7GHz to 7GHz Fractional-N LCPLL Utilizing Multimetal Layer SoC Technology in 28nm CMOS	Univ. of Michigan	A 6.67mW Sparse Coding ASIC Enabling On-Chip Learning and Inference	imec	Role of the Ta scavenger electrode in the excellent switching control and reliability of a scalable low-current operated TiN\Ta2O5\Ta RRAM device	Penn State	Impact of Contact and Local Interconnect Scaling on Logic Performance
	C9.2	8:30 a.m.-8:55 a.m.	C8.2	8:30 a.m.-8:55 a.m.	T15.2	8:30 a.m.-8:55 a.m.	T16.2	8:30 a.m.-8:55 a.m.
	Univ. of Illinois	A 3.7mW 3MHz Bandwidth 4.5GHz Digital Fractional-N PLL with -106dBc/Hz In-band Noise using Time Amplifier Based TDC	KAIST	A Vocabulary Forest-based Object Matching Processor with 2.07M-vec/s Throughput and 13.3pJ/vector Energy in Full-HD Resolution	NDL/NARLabs	Utilizing Sub-5 nm Sidewall Electrode Technology for Atomic-Scale Resistive Memory Fabrication	Intel	Process Technology Scaling in an Increasingly Interconnect Dominated World
	C9.3	8:55 a.m.-9:20 a.m.	C8.3	8:55 a.m.-9:20 a.m.	T15.3	8:55 a.m.-9:20 a.m.	T16.3	8:55 a.m.-9:20 a.m.
	U. of Illinois	A 4.4-5.4GHz Digital Fractional-N PLL Using ΔΣ Frequency-to-Digital Converter	Univ. of CA, LA	A 500MHz Blind Classification Processor for Cognitive Radios in 40nm CMOS	imec	Tailoring switching and endurance / retention reliability characteristics of HfO2 / Hf RRAM with Ti, Al, Si dopants	Tohoku Univ.	What Can We Do About Barrier Layer Scaling to 5 nm Node Technology?
	C9.4	9:20 a.m.-9:45 a.m.	C8.4	9:20 a.m.-9:45 a.m.	T15.4	9:20 a.m.-9:45 a.m.	T16.4	9:20 a.m.-9:45 a.m.
	TSMC	A 12mW All-Digital PLL Based on Class-F DCO for 4G Phones in 28nm CMOS	Univ. of CA LA	A 13.1GOPS/mW 16-Core Processor for Software-Defined Radios in 40nm CMOS	Stanford Univ.	A 1TnR Array Architecture using a One-Dimensional Selection Device	Tokyo Electron Ltd	In-situ Contact Formation for Ultra-low Contact Resistance NiGe Using Carrier Activation Enhancement (CAE) Techniques for Ge CMOS
	C9.5	9:45 a.m.-10:10 a.m.	C8.5	9:45 a.m.-10:10 a.m.	T15.5	9:45 a.m.-10:10 a.m.	T16.5	9:45 a.m.-10:10 a.m.
	HKUST	A 0.37-to-46.5GHz Frequency Synthesizer for Software-Defined Radios in 65nm CMOS	Mediatek Inc.	A 4K×2K@60fps Multi-standard TV SoC Processor with Integrated HDMI/MHL Receiver	SK Hynix Inc.	NbO2-based Low Power and Cost Effective 1S1R Switching for High Density Cross Point ReRAM Application	NTU	3D CMOS-MEMS Stacking with TSV-less and Face-to-Face Direct Metal Bonding
	C11: Advanced Wireline Techniques		**C10: Oversampled ADCs**		**T17: Design Technology Co-Opt. II (JFS)**		**T18: Devices Physics and Reliability II**	
10:20 a.m. -12:05 p.m.	C11.1	10:25 a.m.-10:50 a.m.	C10.1	10:25 a.m.-10:50 a.m.	T17.1	10:25 a.m.-10:50 a.m.	T18.1	10:25 a.m.-10:50 a.m.
	Oregon State Univ.	A 0.8V, 560fJ/bit, 14Gb/s Injection-Locked Receiver with Input Duty-Cycle Distortion Tolerable Edge-Rotating 5/4X Sub-Rate CDR in 65nm CMOS	Oregon State Univ.	A 75dB DR 50MHz BW 3rd Order CT-ΔΣ Using VCO-Based Integrators	U. o f Michigan	IoT Design Space Challenges: Circuits and Systems	CEA-LETI	Direct measurement of the dynamic variability of 0.120µm2 SRAM cells in 28nm FD-SOI technology
	C11.2	10:50 a.m.-11:15 a.m.	C10.2	10:50 a.m.-11:15 a.m.	T17.2	10:50 a.m.-11:15 a.m.	T18.2	10:50 a.m.-11:15 a.m.
	Fujitsu	A 56-Gb/s Receiver Front-End with a CTLE and 1-Tap DFE in 20-nm CMOS	MediaTek	A 23mW, 73dB Dynamic Range, 80MHz BW Continuous-Time Delta-Sigma Modulator in 20nm CMOS	Qualcomm	Chip Package Interaction with Fine Pitch Cu Pillar Bump Using Mass Reflow and Thermal Compression Bonding Assembly Process for 20nm/16nm and Beyond	Univ. of Tokyo	Ultra-Low Voltage (0.1V) Operation of Vth Self-Adjusting MOSFET and SRAM Cell
	C11.3	11:15 a.m.-11:40 a.m.	C10.3	11:15 a.m.-11:40 a.m.	T17.3	11:15 a.m.-11:40 a.m.	T18.3	11:15 a.m.-11:40 a.m.
	Univ. of Toronto	On-Chip Measurement of Data Jitter with Sub-Picosecond Accuracy for 10Gb/s Multilane CDRs	Analog Devices Inc.	A 97.3 dB SNR, 600 kHz BW, 31mW Multibit Continuous Time Δ∑ ADC	LEAP	Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era	Toshiba	Systematic Study of RTN in Nanowire Transistor and Enhanced RTN by Hot Carrier Injection and Negative Bias Temperature Instability
	C11.4	11:40 a.m.-12:05 a.m.	C10.4	11:40 a.m.-12:05 a.m.	T17.4	11:40 a.m.-12:05 a.m.	T18.4	11:40 a.m.-12:05 a.m.
	HKUST	A 48-mW 18-Gb/s Fully Integrated CMOS Optical Receiver with Photodetector and Adaptive Equalizer	Nat'l Taiwan Univ.	An 8.5MHz 67.2dB SNDR CTDSM with ELD Compensation Embedded Twin-T SAB and Circular TDC-based Quantizer in 90nm CMOS	Qualcomm	Cost and Power/Performance Optimized 20nm SoC Technology for Advanced Mobile Devices	Toshiba	Further Understandings on Random Telegraph Signal Noise through Comprehensive Studies on Large Time Constant Variation and its Strong Correlations to Thermal Activation Energies
	Executive Panel Discussion and Luncheon - 12:15 p.m. - 1:30 p.m. (Room to be announced)							
	C13: Medical Imaging		**C12: Non-Volatile and Emerging Memory (JFS)**		**T19: Emerging Device Technology II**		**T20: Process Technology II**	
1:30 p.m.-3:10 p.m.	C13.1	1:30 p.m. - 1:55 p.m.	C12.1	1:30 p.m. - 1:55 p.m.	T19.1	1:30 p.m. - 1:55 p.m.	T20.1	1:30 p.m. - 1:55 p.m.
	KAIST	An Impedance and Multi-wavelength Near-infrared Spectroscopy IC for Non-invasive Blood Glucose Estimation	Toshiba	Highly Reliable and Low-Power Nonvolatile Cache Memory with Advanced Perpendicular STT-MRAM for High-Performance CPU	Imec	In0.53Ga0.47As Quantum-Well MOSFET with Source/Drain Regrowth for Low Power Logic Applications	SEMATECH	Statistical demonstration of silicide-like uniform and ultra-low specific contact resistivity using a metal/high-k/Si stack in a sidewall contact test structure
	C13.2	1:55 p.m.- 2:20 p.m.	C12.2	1:55 p.m.- 2:20 p.m.	T19.2	1:55 p.m.- 2:20 p.m.	T20.2	1:55 p.m.- 2:20 p.m.
	UC Berkeley	A 6.5/11/17.5/30-GHz High Throughput Interferometer-based Reactance Sensors using Injection-Locked Oscillators and Ping-Pong Nested Chopping	Nat'l Tsing Hua Univ.	ReRAM-based 4T2R Nonvolatile TCAM with 7x NVM-Stress Reduction, and 4x Improvement in Speed-WordLength-Capacity for Normally-Off Instant-On Filter-Based Search Engines Used in Big-Data Processing	SEMATECH	Electrostatics and Performance Benchmarking using all types of III-V Multi-gate FinFETs for sub 7nm Technology Node Logic Application	NTU	The demonstration of D-SMT stressor on Si and Ge n-FinFETs
	C13.3	2:20 p.m. - 2:45 p.m.	C12.3	2:20 p.m. - 2:45 p.m.	T19.3	2:20 p.m. - 2:45 p.m.	T20.3	2:20 p.m. - 2:45 p.m.
	Nanyang Tech. U.	A 64×64 1200fps CMOS Ion-Image Sensor with Suppressed Fixed-Pattern-Noise for Accurate High-throughput DNA Sequencing	Phison Ele./ NCTU	A Low Power and Ultra High Reliability LDPC Error Correction Engine with DSP for Embedded NAND Flash Controller in 40nm COMS	Semi. Energy Lab	Scaling to 50-nm C-Axis Aligned Crystalline In-Ga-Zn Oxide FET with Surrounded Channel Structure and Its Application for Less-Than-5-nsec Writing Speed Memory	Toshiba	Design Methodology of Tri-Gate Poly-Si MOSFETs with 10nm Nanowire Channel to Enhance Short-Channel Performance and Reduce Vth & Id Variability
	C13.4	2:45 p.m.- 3:10 p.m.	C12.4	2:45 p.m.- 3:10 p.m.	T19.4	2:45 p.m.- 3:10 p.m.	T20.4	2:45 p.m.- 3:10 p.m.
	Univ. of Florida	A 4.7T/11.1T NMR compliant wirelessly programmable implant for bio-artificial pancreas in vivo monitoring	Chuo Univ.	Application-Aware Solid-State Drives (SSDs) with Adaptive Coding	Stanford Univ.	Monolithic Three-Dimensional Integration of Carbon Nanotube FETs with Silicon CMOS	Renesas Electronics	Enhanced Drivability of High-Vbd Dual-oxide-based Complementary BEOL-FETs for Compact On-chip Pre-driver
	C15: Millimeter-Wave & Cellular Radios		**C14: SRAM and DRAM (JFS)**		**T21: Emerging Device Technology I**		**T22: Memory Technology: RRAM II**	
3:10 p.m. - 6:05 p.m.	C15.1	3:25 p.m. - 3:50 p.m.	C14.1	3:25 p.m. - 3:50 p.m.	T21.1	3:25 p.m. - 3:50 p.m.	T22.1	3:25 p.m. - 3:50 p.m.
	Panasonic	A PVT-Variation Tolerant Fully Integrated 60GHz Transceiver for IEEE 802.11ad	Renesas Electronics	A 512-kb 1-GHz 28-nm Partially Write-Assisted Dual-Port SRAM with Self-Adjustable Negative Bias Bitline	Micron	Integration of Silicon Photonics in Bulk CMOS	imec	Lateral and vertical scaling impact on statistical performances and reliability of 10nm TiN/Hf(Al)O/Hf/TiN RRAM devices
	C15.2	3:50 p.m. - 4:15 p.m.	C14.2	3:50 p.m. - 4:15 p.m.	T21.2	3:50 p.m. - 4:15 p.m.	T22.2	3:50 p.m. - 4:15 p.m.
	Nat'l Taiwan Univ.	A 94GHz Duobinary Keying Wireless Transceiver in 65nm CMOS	ARM Inc.	Low VMIN 20nm Embedded SRAM with Multi-voltage Wordline Control based Read and Write Assist Techniques	Nat'l U. of Singapore	Germanium-Tin on Silicon Avalanche Photodiode for Short-Wave Infrared Imaging	Peking U	Towards High-Speed, Write-Disturb Tolerant 3D Vertical RRAM Arrays
	C15.3	4:15 p.m. - 4:40 p.m.	C14.3	4:15 p.m. - 4:40 p.m.	T21.3	4:15 p.m. - 4:40 p.m.	T22.3	4:15 p.m. - 4:40 p.m.
	UCLA	A Receiver Architecture for Intra-Band Carrier Aggregation	Univ. of Michigan	A 4.68Gb/s Belief Propagation Polar Decoder with Bit-Splitting Register File	TSMC	Advanced 1.1um Pixel CMOS Image Sensor with 3D Stacked Architecture	Fudan Univ.	Fast Step-Down Set Algorithm of Resistive Switching Memory with Low Programming Energy and Significant Reliability Improvement
	C15.4	4:40 p.m. - 5:05 p.m.	C14.4	4:40 p.m. - 5:05 p.m.	T21.4	4:40 p.m. - 5:05 p.m.	T22.4	4:40 p.m. - 5:05 p.m.
	Texas A&M U.	A +22dBm IIP3 and 3.5dB NF Wideband Receiver with RF and Baseband Blocker Filtering Technique	MoSys	Early detection and repair of VRT and aging DRAM bits by margined in-field BIST	Tokyo Inst. Tech.	High-Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits	LEAP	1T-1R Pillar-Type Topological-switching Random Access Memory (TRAM) and Data Retention of GeTe/Sb2Te3 Super-Lattice Films
			C14.5	5:05 p.m. - 5:30 p.m.	T21.5	5:05 p.m. - 5:30 p.m.	T22.5	5:05 p.m. - 5:30 p.m.
			Intel	2nd Generation Embedded DRAM with 4X Lower Self-Refresh Power in 22nm Tri-Gate CMOS Technology	POSTECH	Electrical and Reliability Characteristics of a Scaled (~30nm) Tunnel Barrier Selector (W/Ta2O5/TaOx/TiO2/TiN) with Excellent Performance (JMAX > 107A/cm2)	LEAP	A Fast and Low-Voltage Cu Complementary-Atom-Switch 1Mb Array with High-Temperature Retention
					T21.6	5:30 p.m. - 6:05 pm		
	Circuits Rump Sessions - 8:00 pm - 10:00 pm				Sematech	High-Performance MoS2 Field-Effect Transistors Enabled by Chloride Doping: Record Low Contact Resistance (0.5 kΩ•µm) and Record High Drain Current (460 µA/µm)		

2014 Symposia on VLSI Technology and Circuits June 13th Friday

Time	Honolulu Suite	Tapa I	Tapa II	Tapa III

7:30 am - 5:00 pm Registration

8:05 am - 10:10 am

C16: SOC Circuits & Processors		C17: Image Sensors	
C16.1	8:05 a.m. - 8:30 a.m.	C17.1	8:05 a.m. - 8:30 a.m.
Intel	340mV-1.1V, 289Gbps/W, 2090-gate NanoAES Hardware Accelerator with Area-optimized Encrypt/Decrypt GF(2^4)^2 Polynomials in 22nm tri-gate CMOS	Univ. of Michigan	A Millimeter-Scale Wireless Imaging System with Continuous Motion Detection and Energy Harvesting
C16.2	8:30 a.m.-8:55 a.m.	C17.2	8:30 a.m.-8:55 a.m.
Columbia Univ.	R-Processor: 0.4V Resilient Processor with a Voltage-Scalable and Low-Overhead In-Situ Error Detection and Correction Technique in 65nm CMOS	Univ. Catholique de Louvain	A 65-nm 0.5-V 17-pJ/frame.pixel DPS CMOS Image Sensor for Ultra-Low-Power SoCs achieving 40-dB Dynamic Range
C16.3	8:55 a.m.-9:20 a.m.	C17.3	8:55 a.m.-9:20 a.m.
Nat'l Chiao Tung Univ.	A 7.11mJ/Gb/Query Data-Driven Machine Learning Processor (D2MLP) for Big Data Analysis and Applications	Cornell U.	An On-chip 72×60 Angle-Sensitive Single Photon Image Sensor Array for Lens-Less Time-Resolved 3-D Fluorescence Lifetime Imaging,
C16.4	9:20 a.m.-9:45 a.m.	C17.4	9:20 a.m.-9:45 a.m.
Kobe Univ.	A Local EM-Analysis Attack Resistant Cryptographic Engine with Fully-Digital Oscillator-Based Tamper-Access Sensor	Univ. of Edinburgh	320x240 Oversampled Digital Single Photon Counting Image Sensor
C16.5	9:45 a.m.-10:10 a.m.	C17.5	9:45 a.m.-10:10 a.m.
MIT	A Self-Aware Microprocessor SoC using Energy Monitors Integrated into DC/DC Converters for System Adaptation	Renesas Electr.	A 3.7M-pixel 1300-fps CMOS Image Sensor with 5.0G-Pixel/s High-Speed Readout Circuit

10:25 am -12:05 pm

C18: Biomedical Circuits & Systems		C19: DACs and Mixed-Signal Techniques	
C18.1	10:25 a.m.-10:50 a.m.	C19.1	10:25 a.m.-10:50 a.m.
UC Berkeley	A 4.78mm2 Fully-Integrated Neuromodulation SoC Combining 64 Acquisition Channels with Digital Compression and Simultaneous Dual Stimulation	Univ. of Southern CA	A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator achieving >75dB SFDR over 500MHz in 65nm CMOS
C18.2	10:50 a.m.-11:15 a.m.	C19.2	10:50 a.m.-11:15 a.m.
U. of Michigan	A 266nW Multi-Chopper Amplifier with 1.38 Noise Efficiency Factor for Neural Signal Recording,	MediaTek	A 960MS/s DAC with 80dB SFDR in 20nm CMOS for Multi-Mode Baseband Wireless Transmitter
C18.3	11:15 a.m.-11:40 a.m.	C19.3	11:15 a.m.-11:40 a.m.
CA Inst. of Tech	An Implantable Continuous Glucose Monitoring Microsystem in 0.18µm CMOS,	Broadcom	A 3nV/√Hz Programmable Gain/BW Mixed-Signal 4th Order Chebyshev High-Pass Filter for ADSL/VDSL Analog Front End in 28nm CMOS
C18.4	11:40 a.m.-12:05 a.m.	C19.4	11:40 a.m.-12:05 a.m.
U. of Washington	A Single-chip Encrypted Wireless 12-Lead ECG Smart Shirt for Continuous Health Monitoring,	Univ. of Twente	A 110mW, 0.04mm2, 11GS/s 9-bit interleaved DAC in 28nm FDSOI with >50dB SFDR across Nyquist

1:30 pm-6:05 pm

C20: DC/DC Buck Converters		C21: Capacitive Transducers	
C20.1	1:30 p.m. - 1:55 p.m.	C21.1	1:30 p.m. - 1:55 p.m.
Intel	A 500 MHz, 68% efficient, Fully On-Die Digitally Controlled Buck Voltage Regulator on 22nm Tri-Gate CMOS	Princeton Univ.	An ASIC for Readout of Post-Processed Thin-film MEMS Resonators by Employing Capacitive Interfacing and Active Parasitic Cancellation
C20.2	1:55 p.m.- 2:20 p.m.	C21.2	1:55 p.m.- 2:20 p.m.
Oregon State Univ.	A 10-25MHz, 600mA Buck Converter using Time-Based PID Compensator with 2µA/MHz Quiescent Current, 94% Peak Efficiency, and 1MHz BW	Univ. of Michigan	15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR
C20.3	2:20 p.m. - 2:45 p.m.	C21.3	2:20 p.m. - 2:45 p.m.
The Univ. of Texas at Dallas	A 40-MHz 85.8%-Peak-Efficiency Switching-Converter-Only Dual-Phase Envelope Modulator for 2-W 10-MHz LTE Power Amplifier	Samsung Elect	A Fully-Differential Capacitive Touch Controller with Input Common-Mode Feedback for Symmetric Display Noise Cancellation
C20.4	2:45 p.m.- 3:10 p.m.	C21.4	2:45 p.m.- 3:10 p.m.
Nat'l Chiao Tung Univ	±3% Voltage Variation and 95% Efficiency 28nm Constant On-Time Controlled Step-down Switching Regulator Directly Supplying to Wi-Fi Systems	MIT	A Column-Row-Parallel ASIC Architecture for 3D Wearable / Portable Medical Ultrasonic Imaging

C22: Frequency Generation & Measurement Techniques		C23: High-Speed SAR ADCs	
C22.1	3:25 p.m. - 3:50 p.m.	C23.1	3:25 p.m. - 3:50 p.m.
Univ. of Illinois	A 4.25GHz-4.75GHz Calibration-free Fractional-N Ring PLL Using Hybrid Phase/Current-mode Phase Interpolator With 13.2dB Phase noise Improvement	imec	A 70 dB SNDR 200 MS/s 2.3 mW dynamic pipelined SAR ADC in 28nm digital CMOS
C22.2	3:50 p.m. - 4:15 p.m.	C23.2	3:50 p.m. - 4:15 p.m.
Samsung Electr	A 0.63ps, 12b, Synchronous Cyclic TDC using a Time Adder for On-chip Jitter Measurement of a SoC in 28nm CMOS Technology	Nat'l Taiwan U	A 12-bit 210-MS/s 5.3-mW Pipelined-SAR ADC with a Passive Residue Transfer Technique
C22.3	4:15 p.m. - 4:40 p.m.	C23.3	4:15 p.m. - 4:40 p.m.
Univ. of Michigan	An N-path Filter Enhanced Low Phase Noise Ring VCO	Broadcom	An 11.5-ENOB 100-MS/s 8mW Dual-Reference SAR ADC in 28nm CMOS
C22.4	4:40 p.m. - 5:05 p.m.	C23.4	4:40 p.m. - 5:05 p.m.
Univ. of Tokyo	92% Start-up Time Reduction by Variation-Tolerant Chirp Injection (CI) and Negative Resistance Booster (NRB) in 39MHz Crystal Oscillator	Univ. of Texas	A 12b 160MS/s Synchronous Two-Step SAR ADC Achieving 20.7fJ/step FoM with Opportunistic Digital Background Calibration
C22.5	5:05 p.m. - 5:30 p.m.		
Toshiba	A 2.9mW, +/- 85ppm Accuracy Reference Clock Generator Based on RC Oscillator with On-chip Temperature Calibration		

Spintronics Workshop - 5:00 pm - 10:00 pm (time tentative)