2014 Symposium on VLSI Circuits Short Course
HONOLULU I

Advanced Energy Efficient Digital Design

Tuesday, June 10

Co-Chairs: S. Sridhara, Texas Instruments
M. Takamiya, The University of Tokyo

8:30 a.m. Introduction

8:45 a.m. – Overview and Advances in Energy Efficient Digital Design, D. Blaauw, University of Michigan

9:45 a.m. – Low Power CPUs for SOC Integration, D. Flynn, ARM

10:45 a.m. – 11:00 a.m. – Break

11:00 a.m. – Energy Efficient System Architectures, M. Goel, Texas Instruments

12:00 p.m. – 1:30 p.m. – Lunch

1:30 p.m. – Fine-Grained Power Management Using Integrated DC-DC Converters, J. Douglas, Intel

2:30 p.m. – Challenges and Techniques for Ultra-Low Voltage Logic with Nearly-Minimum Energy, M. Alioto, National University of Singapore

3:30 p.m. – 3:45 p.m. – Break

3:45 p.m. – Advanced Energy Efficient SRAM Design, S. Miyano, Toshiba

4:45 p.m. – Closing Remarks

2014 Symposium on VLSI Circuits Short Course
HONOLULU II

Advanced Data Converter and Mixed-Signal Circuit Design

Tuesday, June 10

Co-Chairs: Y. Chiu, University of Texas, Dallas
M. Ito, Renesas Electronics Corporation

8:30 a.m. Introduction

8:45 a.m. – A/D Converter Trends: Power Efficiency and Digitally Assisted Architectures, B. Murmann, Stanford University

9:45 a.m. – System Design for Direct Sampling RF Front Ends, R. Gomez, Broadcom Corp.

10:45 a.m. – 11:00 a.m. – Break

11:00 a.m. – Advances in SAR ADCs with the Scaling of CMOS, R. Kapusta, Analog Devices, Inc.

12:00 p.m. – 1:30 p.m. – Lunch

1:30 p.m. – Ultra-Wideband Time-Interleaved SAR ADCs for Wireline/Optical Communications, L. Kull, IBM

2:30 p.m. – Digitally Assisted Wireless Transceivers and Synthesizers, K. Okada, Tokyo Institute of Technology

3:30 p.m. – 3:45 p.m. – Break

3:45 p.m. – Digital Error Correction of Time-Interleaved A/D Converters, A. Abidi, University of California, Los Angeles

4:45 p.m. – Closing Remarks

Technology / Circuits Joint Rump Session
Tuesday, June 10, 8:00 p.m. – 10:00 p.m.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 10
8:00 p.m. – 10:00 p.m.

RJ-1: Who gives up on scaling first: device and process technology engineers, circuit designers, or company executives? Which scaling ends first – memory, or logic?

Technology Organizers:
C. Mazure, SOITEC
Y.Y. Chia, National University of Singapore

Circuits Organizers:
E. Alon, University of California, Berkeley
M. Yamaoka, Hitachi

Moderators: E. Alon, University of California, Berkeley
Y.Y. Chia, National University of Singapore

While many past predictions of the end of CMOS scaling were proven to be incorrect, there is now no question that the nature of scaling today has shifted dramatically. In particular, energy, performance, and perhaps even cost no longer clearly/directly benefit from simple dimensional scaling. This panel will therefore address the now extremely timely question of who will finally drive the decision to stop CMOS scaling, and why will they do so. Will CMOS continue to scale as far as device and process engineers are able to develop cost-effective manufacturing infrastructure, or will circuit designers no being able to extract benefits from scaling due to power/thermal issues first? Or will executives decide that the returns from scaling in terms of cost – due for example to design costs or limited markets supporting the volume to amortize that cost – are no longer worth it? The panel will discuss these question in the context of both memory and logic technologies, and will further consider which of the two will end first.

Panelists:
M. Bohr, Intel
M. Cao, TSMC
J. Chen, nVidia
S-H Lee, Hynix
T-J King Liu, University of California, Berkeley
K. Nii, Renesas
R. Shrivastava, Sandisk
T. Skotnicki, STMicroelectronics

Session 1 – TAPA II
Plenary Session

Wednesday, June 11, 8:05 a.m.
Chairpersons: J. Gealow, Analog Devices
M. Motomura, Hokkaido University

8:05 a.m. **Welcome, Opening Remarks, and Awards**
V. De, Intel Corp.
H. Kabuo, Panasonic Corp.

1.1 – 8:35 a.m.
DataCenter 2020: Near-memory Acceleration for Data-oriented Applications, Ed Doller, Micron

In the years between now and 2020, we should expect continued exponential data growth. A number of ongoing advances in storage: the transition to solid-state drives (SSDs), the scaling of NAND flash capacity, and advanced silicon packaging techniques will dramatically increase the capacity of storage subsystems over the same timeframe. This will significantly reduce the ratio of storage bandwidth to storage density. Consequently, the majority of data in 2020 will either be cold or will require near-memory acceleration to pull rich information out of the sea of big data. We argue that, increasingly over time, value lies not merely in the size of the data, but rather in what one can do with it.

1.2 – 9:20 a.m.
Technology Development for Printed LSIs Based on Organic Semiconductors, Jun Takeya, The University of Tokyo

This presentation focuses on recent development of key technologies for printed LSIs which can provide future low-cost platforms for RFID tags, AD converters, data processors, and sensing circuitries. Such prospect bears increasing reality because of recent research innovations in the field of material chemistry, charge transport physics, and solution processes of printable organic semiconductors. Achieving band transport in state-of-the-art printable organic semiconductors, carrier mobility is elevated above 15 cm^2/Vs, so that reasonable speed in moderately integrated logic circuits can be available. With excellent chemical and thermal stability for such compounds, we are developing simple integrated devices based on CMOS using p-type and n-type printed organic FETs. Particularly important are new processing technologies for continuous growth of inch-size organic single-crystalline semiconductor “wafers” from solution and for lithographical patterning of semiconductors and metal electrodes. Successful rectification and identification are demonstrated at 13.56 MHz with printed organic CMOS circuits for the first time.

Session 2 - TAPA I
Ultra-High-Speed Wireline Transceivers

Wednesday, June 11
Chairpersons: P. Kumar Hanumolu, University of Illinois, Urbana-Champaign
C. Patrick Yue, Hong Kong University of Science and Technology

2.1 - 10:25 a.m.

A 36 Gbps 16.9 mW/Gbps Transceiver in 20-nm CMOS with 1-tap DFE and Quarter-Rate Clock Distribution, T. Hashida, Y. Tomita, Y. Ogata, K. Suzuki, S. Suzuki, T. Nakao, Y. Terao, S. Honda, S. Sakabayashi, R. Nishiyama, A. Konmoto, Y. Ozeki, H. Adachi, H. Yamaguchi, Y. Koyanagi and H. Tamura, Fujitsu Laboratories LTD.

A 36-Gbps transceiver with a continuous-time linear equalizer and a 1-tap DFE in 20-nm CMOS is demonstrated. The transceiver uses a quarter-rate (i.e., 9-GHz) differential-clock distribution to reduce the clock-delivery power. Multi-phase half-rate clock signals that drive the transceiver front-ends are generated by a delay-locked loop and frequency doublers that systematically reduce the impact of skew and jitter. The transceiver occupies 0.55 mm^2 and consumes 609.9 mW of power from a 0.9-V supply.

2.2 - 10:50 a.m.
A Quad-Channel 112-128 Gb/s Coherent Transmitter in 40 nm CMOS, A. Garg, U. Singh, N. Huang, W. Wong, B. Liu, Z. Huang, A. Momtaz and J. Cao, Broadcom Corporation

A quad-channel, 112-128 Gb/s coherent DP-QPSK transmitter in 40 nm CMOS is presented. The 27.9-32.1 Gb/s TX features a half-rate architecture with a 2-tap FIR. The measured output has an amplitude of $1.2V_{pp\text{-}diff}$ with 1.3 ps deterministic jitter (DJ). The DP-QPSK TX's precoded data alignment is maintained through the quad-lane transmitter by the use of an automatic synchronous feedback loop, removing the need for a master global reset. The PLL outputs the full-rate and half-rate clock with ±0.5 UI skew adjustment relative to the data. The power consumption of the transmitter and PLL is 712 mW.

2.3 - 11:15 a.m.
A 40-Gb/s Serial Link Transceiver in 28-nm CMOS Technology, E-H. Chen, M. Hossain*, B. Leibowitz, R. Navid, J. Ren, A. Chou, B. Daly, M. Aleksic, B. Su, S. Li, M. Shirasgaonkar, F. Heaton, J. Zerbe and J. Eble, Rambus Inc., *also with University of Alberta

A SerDes operating at 40 Gb/s optimized for chip-to-chip communication is presented. Equalization consists of 2-tap feed-forward equalizers (FFE) in both transmitter and receiver, a 3-stage continuous-time linear equalizer (CTLE) and discrete time equalizers including 17-tap decision feedback equalizer (DFE) and 3-tap sampled-FFE in the receiver. The SerDes is realized in 28-nm CMOS technology with 23.2 mW/Gb/s power efficiency at 40 Gb/s.

2.4 - 11:40 a.m.
A 4x40 Gb/s Quad-Lane CDR with Shared Frequency Tracking and Data Dependent Jitter Filtering, M. Hossain*, E-H. Chen, R. Navid, B. Leibowitz, A. Chou, S. Li, M.J. Park, J. Ren, B. Daly, B. Su, M. Sriasgaonkar, F. Heaton, J. Zerbe and J. Eble, Rambus, *also with University of Alberta

A 4x40 Gb/s collaborative digital CDR is implemented in 28nm CMOS. The CDR is capable of recovering a low jitter clock from a partially or un-equalized eye by using a phase detection scheme that inherently filters out edges with ISI. The CDR uses a split feedback architecture that allows wider bandwidth and lower recovered clock jitter at the same time. Finally, a shared frequency tracking is introduced that results in lower periodic jitter. Combining these techniques the CDR recovers clock from an eye in the presence of 0.8UIpp DDJ and still achieves 1-10 MHz of tracking bandwidth and adding less that 300fs of jitter. Per lane CDR occupies only .06 mm^2 and consumes 175 mW.

Session 3 - HONOLULU
Power Management for Wireless Sensor Nodes

Wednesday, June 11
Chairpersons: H.J. Bergveld, NXP Semiconductors
M. Takamiya, The University of Tokyo

3.1 - 10:25 a.m.
Low Power Battery Supervisory Circuit with Adaptive Battery Health Monitor, I. Lee, Y. Lee, D. Sylvester and D. Blaauw, University of Michigan

We propose a battery supervisory circuit (BSC) for wireless sensor nodes that automatically adapts to varying battery health, as reflected by its internal resistance (R_{BAT}), and establishes a constant effective threshold voltage. Compared to a conventional fixed-threshold BSC, the new design avoids oscillation and widens the usable range of battery voltages, independent of R_{BAT}. R_{BAT} is measured by inducing a test current using decaps and measuring the resulting battery RC response time. When tested with a 2µAh battery and 11µA sensor system, the BSC reduces the required hysteresis from 656mV to 77mV, increasing the usable battery voltage range by 2.7×.

3.2 - 10:50 a.m.
A 1.2µW SIMO Energy Harvesting and Power Management Unit with Constant Peak Inductor Current Control Achieving 84-92% Efficiency Across Wide Input and Output Voltages, A. Shrivastava, Y. Ramadass, S. Khanna, S. Bartling and B. Calhoun*, Texas Instruments, *University of Virginia

This paper presents a single inductor energy harvesting and power management unit for ultra-low power (ULP) systems. The proposed circuit harvests energy from solar cell from 0.38V input voltage (Vin) and provides 3 regulated output voltages at 3.3V, 1.5V, and 1.2V and a storage at 5V. A peak inductor current control scheme enables high efficiency operation across wide input and output voltage range. A cold start and maximum power point tracking scheme enables operation from 380mV Vin.

3.3 - 11:15 a.m.
A Direct AC-DC and DC-DC Cross-Source Energy Harvesting Circuit with Analog Iterating-Based MPPT Technique with 72.5% Conversion Efficiency and 94.6% Tracking Efficiency, T.-C. Huang, M.-J. Du, K.-L. Lin, S.S. Ng, K.-H. Chen, C.-L. Wey, Y.-H. Lin*, T.-Y. Tsai*, C.-C. Huang*, C.-C. Lee*, J.-L. Chen** and H.-W. Chen**, National Chiao Tung University, *Realtek Semiconductor Corp., **Vanguard Semiconductor Corp.

The proposed cross-source energy (CSE) harvesting system can accept universal energy sources, including AC and DC sources. The buck-boost conversion of CSE automatically converts AC or DC input into DC output without being limited by universal input voltage range. CSE provides dual outputs, a regulated output and a battery charging output, to optimally arrange harvest energy with 72.5% of power efficiency. A backup converter is designed to cooperate with CSE to guarantee the output voltage stability of the regulated output. The proposed analog iterating-based (AIB) maximum power point tracking (MPPT) technique achieves 94.6% tracking efficiency without complex data calculation and storage compared to previous techniques.

3.4 - 11:40 a.m.
A 13.56MHz Wireless Power Transfer System with Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices, X. Li, C.-Y. Tsui and W.-H. Ki, HKUST

A 13.56MHz wireless power transfer system with a 1X/2X reconfigurable resonant regulating (R3) rectifier and wireless power control for biomedical implants is presented. Output voltage regulation is achieved through two mechanisms: the local PWM loop of the secondary side controls the duty cycle of switching the rectifier between the 1X and 2X modes; and to adapt to load and coupling variations, the duty cycle information encoded in Manchester code is fed back wirelessly to the primary side using a novel backscattering uplink technique to adjust the transmitter power of the primary coil. The primary transmitter and the secondary R3 rectifier are fabricated in 0.35µm CMOS process. The measured maximum received power and receiver efficiency are 102mW and 92.6%, respectively.

Session 4 - TAPA II

Circuits / Technology Joint Focus Session: 3D Circuits and Applications

Wednesday, June 11

Chairpersons: F. Hamzaoglu, Intel Corporation
M. Yamaoka, Hitachi, Ltd.

4.1 - 1:30 p.m.

Design Technologies for a 1.2V 2.4Gb/s/pin High Capacity DDR4 SDRAM with TSVs, R. Oh, B. Lee, S.-W. Shin, W. Bae, H. Choi, I. Song, Y.-S. Lee, J.-H. Choi, C.-W. Kim, S-J Jang, J.S. Choi, Samsung Electronics

For the demand of sever systems with high performance, high density and low power consumption, 3-D DDR4 SDRAM with TSVs was developed. In order to achieve higher data rate at lower voltage in comparison with precedent DDR3 SDRAM with TSVs, the placements of TSVs have been optimized without the penalty of chip size and the calibration method for reducing process mismatch between stacked DRAM chips is proposed. Additionally, new cell test method for stacked dies is adopted to keep costs down and the skewed self-refresh is proposed to reduce power noise. The IO speed of new DDR4 SDRAM with TSVs is increased to 2.4Gb/s at 1.2V.

4.2 - 1:55 p.m.

An Exact Measurement and Repair Circuit of TSV Connections for 128GB/s High-Bandwidth Memory(HBM) Stacked DRAM, D.U. Lee, K.W. Kim, K.W. Kim, K.S. Lee, S.J. Byeon, J.H. Cho, H.H. Jin, S.K. Nam, J. Lee, J.H. Chun and S. Hong, SK Hynix

New TSV impedance measuring method using correlated double sampling, which supports under 0.1 ohm resolution. TSV repair method based on 4-to-1 chained redundant TSV has increased repair efficiency. Register-based repairing method guarantee test operation before blowing fuse. All above method and circuits are integraed and stacked on 8Gb High-Bandwidth Memory(HBM) with operation at 128GB/s at 1.1v. Measurement data and chip micrograph are included.

4.3 - 2:20 p.m.

A 352Gb/s Inductive-Coupling DRAM/SoC Interface Using Overlapping Coils with Phase Division Multiplexing and Ultra-Thin Fan-Out Wafer Level Package, A. Raziz Junaidi, Y. Take and T. Kuroda, Keio University

The area efficiency of an inductive-coupling interface is improved by 12 times for WIO2 standard (352Gb/s) and beyond. By using a quadrature phase division multiplexing, coils are overlapped and the density is increased by 4 times. It is further increased by 3 times by shortening communication distance with an ultra-thin fan-out wafer level package. The proposed DRAM/SoC interface at 356Gb/s

outperforms WIO2 with TSV in terms of area efficiency (4x better) and manufacturing cost (40% cheaper) and outperforms LPDDR4 in PoP in terms of power dissipation (5x lower) and timing control easiness.

4.4 - 2:45 p.m.
A Peripheral Switchable 3D Stacked CMOS Image Sensor, C.C.-M. Liu, C.-H. Chang, H.-Y. Tu, C.Y.-P. Chao, F.-L. Hsueh, S.-Y. Chen, V. Hsu, J.-C. Liu, D.-N. Yaung and S.-G. Wuu, Taiwan Semiconductor Manufacturing Company

A 1.1 um pitch pixel array fabricated by 45 nm 3D stacked technology, can be switched to peripheral circuits on same wafer or to other stacked wafer for process and signal integrity verification. It supports through silicon connection or direct connection to increase the flexibility by separating pixel array and sensing circuit. The novel wide operation range VCO and low power serializer are implemented to reduce the total power and noise.

Session 5 - HONOLULU
Advanced ADC Techniques

Wednesday, June 11
Chairpersons: Y. Chiu, University of Texas at Dallas
S. Dosho, Panasonic Corporation

5.1 - 1:30 p.m.
An 18 b 5 MS/s SAR ADC with 100.2 dB Dynamic Range, A. Bannon, C.P. Hurrell, D. Hummerston and C. Lyden, Analog Devices

This paper presents an 18 bit 5 MS/s SAR ADC. It has a dynamic range of 100.2 dB, SNR of 99 dB, INL of ±2 ppm and DNL of ±0.4 ppm. It has currently the lowest noise floor of any monolithic Nyquist converter relative to the full scale input (21.9 nV/rt(Hz), ±5V full scale) known to the author, all of this is achieved with an ADC core power of 30.52 mW giving a Schreier figure of merit of 179.3 dB. Architectural choices such as the use of a residue amplifier are outlined that enable the high sample rate, low noise and power efficiency. The design is implemented on 0.18 um CMOS with MIM capacitors and both 1.8 V and 5 V MOS devices. An LVDS interface is used to transfer the ADC result off chip.

5.2 - 1:55 p.m.
A 0.4V 2.02fJ/Conversion-Step 10-bit Hybrid SAR ADC with Time-Domain Quantizer in 90nm CMOS, Y.-J. Chen and C.-C. Hsieh, National Tsing Hua University

This paper presents an ultra-low voltage and power efficient 10-bit hybrid successive-approximation register (SAR) analog-to-digital converter (ADC). To reduce the total amount of capacitance and relieve requirement of comparator, we propose a hybrid architecture composed of coarse and fine conversions by 7-bit SAR ADC and 3.5-bit time domain quantizer, respectively. Using residue voltages generated by coarse ADC and converting it to time-domain, the fine ADC detects the least three bits by vernier delay structure. At 250KS/s and Nyquist rate input, the prototype ADC fabricated in 90nm CMOS consumes 0.2μW at 0.4V supply. It achieves a SNDR of 53.7db and a resulting FoM of 2.02-fJ/conv.-step.

5.3 - 2:20 p.m.

A 48 fJ/CS, 74 dB SNDR, 87 dB SFDR, 85 dB THD, 30 MS/s Pipelined ADC Using Hybrid Dynamic Amplifier, H. Venkatram, T. Oh, K. Sobue*, K. Hamashita* and U.-K. Moon, Oregon State University, *Asahi Kasei Microdevices

A hybrid dynamic amplifier is proposed which combines the desirable features of a dynamic amplifier and a class AB amplifier. This technique allows us to achieve a power efficient high resolution pipeline ADC. A proof of concept pipelined ADC in a 0.18 um CMOS process achieves 74.2 dB SNDR, 87 dB SFDR and 85 dB THD at 30 MS/s. The pipeline ADC consumes 6 mW from a 1.3 V supply and occupies 3.06 mm^2. The ADC achieves a FoM of 48 fJ/CS without any form of calibration.

5.4 - 2:45 p.m.
7-bit 0.8-1.2GS/s Dynamic Architecture and Frequency Scaling Subrange ADC with Binary-Search/Flash Live Configuring Technique, K. Yoshioka, R. Saito, T. Danjo*, S. Tsukamoto* and H. Ishikuro, Keio University, *Fujitsu Laboratories Ltd.

Subrange ADC with Dynamic Architecture and Frequency Scaling(DAFS) is presented, which has exponential power scaling against frequency with high-speed operation of over 1GS/s. We propose Live Configuring Technique(LCT) to adaptively configure the sub-ADC operation between binary-search and flash every clock cycle, reflecting the conversion delay. The power consumption is cut down significantly and retains high-speed operation. The prototype ADC fabricated in 65nm CMOS operates up to 1228MS/s and achieves an SNDR 36.2dB at nyquist. DAFS is active between 800-1200MS/s and when compared with the frequency power scaling with DAFS disabled, the peak power consumption cut down is 30%. Peak FoM of 85fJ/conv. was obtained at 820MS/s, which is nearly a 2x improvement compared with reported subrange ADCs.

Session 6 - TAPA I
Design with Emerging Technologies

Wednesday, June 11
Chairpersons: V. Chandra, ARM
B. Sheu, Taiwan Semiconductor Manufacturing Company

6.1 - 3:25 p.m.
A 2GHz-to-7.5GHz Quadrature Clock Generator Using Digital Delay Locked Loops for Multi-Standard I/Os in 14nm CMOS, A. Elshazly, A. Balankutty, Y.-Y. Huang, K. Yu and F. O'Mahony, Intel Corporation

A highly digital quadrature clock generator using a digital DLL that employs a digital loop filter and digitally-calibrated replica-based regulator is presented. The proposed DLL combines the advantages of both analog and digital loop-filters of conventional architectures to implement a wide-range, energy efficient, highly digital, and high performance quadrature clock generator. To suppress supply-noise, we propose an LDO that combines fast/slow paths with a replica-load to achieve better than 20dB rejection with small area and low power. Fabricated in Intel's 14nm CMOS process, the proposed digital DLL operates over a wide range of output frequencies (2GHz-to-7.5GHz). The proposed quadrature DLL-based clock generator achieves the best power efficiency (600µW/GHz) and the lowest reported jitter (176fs) compared to the previous ISSCC/JSSC/VLSI. Its area is 4X smaller than state-of-the-art DLLs, and 16X smaller than the low-power LC-based quadrature clock generators.

6.2 - 3:50 p.m.

A 0.7V Resistive Sensor with Temperature/Voltage Detection Function in 16nm FinFet Technologies, J.-J. Horng, S.-L. Liu, A. Kundu, C.-H. Chang, C.-H. Chen, H. Chiang and Y.-C. Peng, Taiwan Semiconductor Manufacturing Company

This paper reports a combination structure of temperature and voltage sensor in a 16nm FinFET technology. The circuit transforms PTAT voltage across a resistor into an output clock with PTAT pulse-width. Fabricated in a 16nm CMOS, the temperature sensor achieves 1°C resolution over -10 ~ 90°C range and the voltage sensor achieves 4mV output error over 0.38V to 0.56V. The total chip size is $0.01mm^2$ and draws 70uW total power from a 0.7V supply. Depending on resolution, the measurement time can change from 10µsec to 1.6msec. This approach is not restricted by forward junction bias (~0.7V) of conventional BJTs and diodes.

6.3 - 4:15 p.m.
A Monolithically Integrated Chip-to-Chip Optical Link in Bulk CMOS, C. Sun, M. Georgas, J. Orcutt, B. Moss, Y.-H. Chen, J. Shainline*, M. Wade*, K. Mehta, K. Nammari*, E. Timurdogan, D. Miller**, O. Tehar-Zahav**, Z. Sternberg**, J. Leu, J. Chong, R. Bafrali**, G. Sandhu**, M. Watts, R. Meade**, M. Popovic*, R. Ram and V. Stojanović*, Massachusetts Institute of Technology, *University of Colorado, Boulder, **Micron Technologies

A silicon-photonic link is monolithically-integrated in a bulk CMOS process for the first time. Deep-trench isolation enables polySi waveguide integration. PolySi resonant detectors remove the need for Ge integration. Split-diode design enables half-rate receivers, mitigating transistor speed limitations. An on-chip feedback loop locks the resonant defect detector to the laser wavelength, combating thermal upset. The 5m optical link achieves 5Gb/s at 3pJ/b electrical and 13pJ/b optical energy, in 0.18µm (100ps FO4) bulk CMOS memory periphery process.

6.4 - 4:40 p.m.
A Monolithically-Integrated Optical Transmitter and Receiver in a Zero-Change 45nm SOI Process, M. Georgas, B. Moss, C. Sun, J. Shainline*, J.S. Orcutt, M. Wade*, Y.-H. Chen, K. Nammari*, J. Leu, A. Srinivasan, R. Ram, M. Popovic* and V. Stojanović, Massachusetts Institute of Technology, *University of Colorado, Boulder

An optical transmitter and receiver with monolithically-integrated photonic devices and circuits are demonstrated together for the first time in a commercial 45nm SOI process, without any process changes. The transmitter features an interleaved-junction carrier-depletion ring modulator and operates at 3.5Gb/s with an 8dB extinction ratio and combined circuit and device energy cost of 70fJ/bit. The optical receiver connects to an integrated SiGe detector designed for 1180nm wavelength and performs at 2.5Gb/s with 15µA sensitivity and energy cost of 220fJ/bit.

6.5 - 5:05 p.m.
A 32-bit CPU with Zero Standby Power and 1.5-Clock Sleep/2.5-Clock Wake-up Achieved by Utilizing a 180-nm C-axis Aligned Crystalline In-Ga-Zn Oxide Transistor, A. Isobe, H. Tamura, K. Kato, T. Ohmaru, W. Uesugi, T. Ishizu, T. Onuki, K. Ohshima, T. Matsuzaki, A. Hirose, Y. Suzuki, N. Tsutsui, T. Atsumi, Y. Shionoiri, G. Goto, J. Koyama, M. Fujita* and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., *University of Tokyo

A flip-flop achieving high-speed backup utilizing a Si transistor and long-term retention with zero standby power by means of a transistor of c-axis aligned crystalline (CAAC) In-Ga-Zn oxide, a kind of

CAAC oxide semiconductor, featuring extremely low off-state current is proposed. Using the flip-flop, a 32-bit processor has been fabricated with 350-nm Si/180-nm CAAC oxide semiconductor technology, and demonstrated data backup and power shutdown in 1.5 clock cycles at a low power of 1.77 nJ, data recovery in 2.5 clock cycles, and data retention with zero standby power for at least a day. According to simulation results, fast backup and long-term retention can also be achieved with 45-nm Si/180-nm CAAC oxide semiconductor technology.

Session 7 - HONOLULU

Sensor Node Radios

Wednesday, June 11

Chairpersons: B.P. Ginsburg, Texas Instruments
H. Ishikuro, Keio University

7.1 - 3:25 p.m.

A Power-Harvesting Pad-Less mm-Sized 24/60GHz Passive Radio with On-Chip Antennas, M. Tabesh, M. Rangwala*, A.M. Niknejad and A. Arbabian*, University of California, Berkeley, *Stanford University

A wireless-powered pad-less single-chip dual-band mm-wave passive radio is implemented in 65nm CMOS for applications in sensor networks and wireless tagging. This fully self-sufficient system has no pads or external components (e.g. power supply), and the entire radio is a single 3.7mm X 1.2mm chip. To provide multi-access, and to mitigate interference, it uses two separate mm-wave bands for RX/TX and integrates both antennas to provide a measured communication range of 50cm. Compared to mm-sized passive radio solutions in the same category this system provides an order of magnitude range enhancement while improving input sensitivity by >14dB. Wideband pulse transmission enables real-time localization with time-of-flight. The entire system operates with standby harvested power below 1.5μW and aggregate rate >12Mbps.

7.2 - 3:50 p.m.

Energy-Recycling Integrated 6.78-Mbps Data 6.3-mW Power Telemetry over a Single 13.56-MHz Inductive Link, S. Ha, C. Kim, J. Park, S. Joshi and G. Cauwenberghs, University of California, San Diego

We present a power/data telemetry IC with a new data modulation scheme and simultaneous power transfer through a single inductive link. Data-driven synchronized single-cycle shorting of the secondary LC tank conserves reactive power while inducing an instantaneous voltage change at the primary side. Cyclic on-off keying time-encoded symbol mapping of the shorting cycle allows transmission of two data bits per four carrier cycles with simultaneous power transfer during non-shorting cycles. All timing control signals for rectification and data transmission are generated from a low-power clock recovery comparator and 22-phase 2× PLL. The 1-mm^2 65-nm CMOS IC delivers up to 6.3-mW power and transmits 6.78-Mbps data with a BER of less than 5.9×10^{-7} over a single 1-cm 13.56-MHz inductive link.

7.3 - 4:15 p.m.

An Ultra-Low-Power 2-step Wake-Up Receiver for IEEE 802.15.4g Wireless Sensor Networks, T. Abe, T. Morie, K. Satou, D. Nomasaki, S. Nakamura, Y. Horiuchi and K. Imamura, Panasonic Corporation

This paper presents an ultra-low-power 2-step wake-up receiver for the IEEE 802.15.4g. The receiver is composed of an ultra-low-power energy-detection receiver (EDRX) and an address-detection FSK receiver (ADRX). The ADRX is activated only when the EDRX detects a wakeup packet which minimizes power consumption. Fabricated in a 65 nm CMOS process, the receiver achieves an excellent receiver sensitivity of -87 dBm while consuming only 45.5 μW average power.

7.4 - 4:40 p.m.

A 400MHz 10Mbps D-BPSK Receiver with a Reference-less Dynamic Phase-to-Amplitude Demodulation Technique, Y.-L. Tsai, J.-Y. Chen, B.-C. Wang, T.-Y. Yeh and T.-H. Lin, National Taiwan University

A 400MHz 10Mbps differential BPSK (D-BPSK) receiver (RX) is presented. This RX adopts a proposed reference-less dynamic phase-to-amplitude demodulation scheme, which converts signal phase transition to distinct amplitude variation. The proposed RX can support a data rate up to 10Mbps. It achieves -63dBm sensitivity at 0.1% BER and draws 1.77mW in 0.18µm CMOS. Take sensitivity, data rate and power consumption into consideration, the RX achieves an FOM more than 160 under various data rate operation.

7.5 - 5:05 p.m.
A 915MHz, 6Mb/s, 80pJ/b BFSK Receiver with -76dBm Sensitivity for High Data Rate Wireless Sensor Networks, R. Ni, K. Mayaram and T. Fiez, Oregon State University

A mixer-less low energy BFSK receiver for wireless sensor networks is presented. Q-enhanced frequency-to-amplitude conversion and linear amplification at RF frequencies provide a large conversion gain and high data rates, leading to improved sensitivity and energy efficiency. Fabricated in a 0.13 µm CMOS process, the 915 MHz receiver, with integrated digital calibration, demonstrates a sensitivity of -90 dBm at 500 kb/s and an energy efficiency of 80 pJ/b at 6 Mb/s.

Session 8 - TAPA I
Signal Processing

Thursday, June 12
Chairpersons: E. Yeo, Marvell
M. Hashimoto, Osaka University

8.1 - 8:05 a.m.
A 6.67mW Sparse Coding ASIC Enabling On-Chip Learning and Inference, J.K. Kim, P. Knag, T. Chen and Z. Zhang, University of Michigan

A sparse coding ASIC is designed to learn visual receptive fields and infer the sparse representation of images for encoding, feature detection and recognition. 256 leaky integrate-and-fire neurons are connected in a 2-layer network of 2D local grids linked in a 4-stage systolic ring to reduce the communication latency. Spike collisions are kept sparse enough to be tolerated to save power. Memory is divided into a core section to support inference, and an auxiliary section that is only powered on for learning. An approximate learning tracks only significant neuron activities to save memory and power. The 3.06mm^2 65nm CMOS ASIC achieves an inference throughput of 1.24Gpixel/s at 1.0V and 310MHz, and on-chip learning can be completed in seconds. Memory supply voltage can be reduced to 440mV to exploit the soft algorithm that tolerates errors, reducing the inference power to 6.67mW for a 140Mpixel/s throughput at 35MHz.

8.2 - 8:30 a.m.
A Vocabulary Forest-based Object Matching Processor with 2.07M-vec/s Throughput and 13.3nJ/vector Energy in Full-HD Resolution, K. Lee, G. Kim, J. Park and H.-J. Yoo, KAIST

A Vocabulary Forest-based object matching processor is proposed to speed up the feature matching stage for the object recognition system with high accuracy. Adopting Reusable-Vocabulary Tree architecture and hardware sharing technique reduces area, as well as adopting propagate-and-compute-array architecture in the combiner and external database elimination enhances the matching speed

more than 16x compared to Approximate Nearest Neighbor searching processors. The proposed Vocabulary Forest processor, implemented in 65nm CMOS process, achieves 2.07M-vec/s throughput and 13.3nJ/vector energy efficiency, and successfully matches 100 objects with 95.7% matching accuracy.

8.3 - 8:55 a.m.
A 500MHz Blind Classification Processor for Cognitive Radios in 40nm CMOS, F.-L. Yuan, T.-H. Yu* and D. Marković, University of California, Los Angeles, *Qualcomm

A blind classification processor for cognitive radios is realized in 40nm CMOS, featuring three-step parameter estimation for up to 59x energy saving compared to an exhaustive method, and multi-algorithm feature extraction to distinguish five modulation classes: multicarrier, single-carrier PSK/QAM/MSK, and spread-spectrum signals. The chip consumes 17µJ within 2ms sensing time per classification, achieving 95% detection probability (P_D) and 0.5% false-alarm rate (P_{FA}) at 10dB SNR in a 500MHz channel.

8.4 - 9:20 a.m.
A 13.1GOPS/mW 16-Core Processor for Software-Defined Radios in 40nm CMOS, F.-L. Yuan and D. Marković, University of California, Los Angeles

A 16-core processor for software-defined radios is realized in 40nm CMOS. Featuring domain-specific kernels, flexible control and multi-scale interconnects, the processor achieves a peak energy efficiency of 13.1GOPS/mW (76fJ/OP) at 415mV, 25MHz, and a peak performance of 1.17TOPS at 1V, 500MHz, showing >2.4x higher energy efficiency than state-of-the-art communication chip multiprocessors, and closing the gap with functionally-equivalent ASICs to within 2.6x.

8.5 - 9:45 a.m.
A 4K×2K@60fps Multi-standard TV SoC Processor with Integrated HDMI/MHL Receiver, C.-C. Ju, T.-M. Liu, H. Wang, Y.-C. Chang, C.-M. Wang, C.-L. Hsieh, B. Liu, H.-M. Lin, C.-Y. Cheng, C.-C. Chen, M.-H. Chiu, S.-J. Wang, P. Chao, M.J. Hu, R. Yeh, T. Chuang, H.-Y. Lin and C.-H. Tsai, Mediatek Inc.

A first-reported 4K×2K@60fps digital TV SoC processor supporting 9 video formats and integrating HDMI/MHL receiver is fabricated in a 40nm CMOS process. It adopts error compensation processor (ECP) to improve the visual quality, and designs a memory management unit and resource sharing technique to improve the throughput and area efficiency by 38.5% and 34.3%, respectively. Moreover, a lossless compression processor (LCP) is newly designed to reduce 30% and 45% of external data accesses in playback and gaming scenario, respectively. The proposed TV SoC processor includes multi-standard 4K×2K@60fps playback and 3.4Gbps HDMI receiver (Rx), and both scenario dissipates 198.15mW at 1.2V core and 3.3V I/O.

Session 9 - HONOLULU
Phase-Locked Loops

Thursday, June 12
Chairpersons: N. Kurd, Intel Corporation
J. Lee, National Taiwan University

9.1 - 8:05 a.m.
A 2.7GHz to 7GHz Fractional-N LCPLL Utilizing Multimetal Layer SoC Technology in 28nm CMOS, C.-H. Lee, L. Kabalican, Y. Ge, H. Kwantono, G. Unruh, M. Chambers and I. Fujimori, Broadcom

A fractional-N LCPLL in 28nm CMOS that uses vertical layout integration techniques to achieve area reduction is proposed. The design utilizes a multimetal layer interposed inductor pair that is stacked on top of the active PLL circuit elements, resulting in an area of 0.07mm^2. The PLL covers a wide-frequency range from 2.7GHz to 7GHz, consuming a total power of 14mW. At 7GHz, the RMS jitter is 0.56ps at integer mode and 1.1ps at fractional mode.

9.2 - 8:30 a.m.
A 3.7mW 3MHz Bandwidth 4.5GHz Digital Fractional-N PLL with -106dBc/Hz In-band Noise using Time Amplifier Based TDC, A. Elkholy, T. Anand, W.-S. Choi, A. Elshazly* and P.K. Hanumolu, University of Illinois, *Intel Corporation

A digital fractional-N PLL that employs a time amplifier based TDC and a truly fractional divider to achieve low in-band noise with a wide bandwidth of 3MHz is presented. Fabricated in 65nm CMOS process, the prototype PLL consumes 3.7mW at 4.5GHz output frequency and achieves better than -106dBc/Hz in-band noise and 490fs$_{rms}$ integrated jitter. This translates to a FoMJ of -240.5dB, which is the best among the reported fractional-N PLLs.

9.3 - 8:55 a.m.
A 4.4-5.4GHz Digital Fractional-N PLL Using ΔΣ Frequency-to-Digital Converter, M. Talegaonkar, T. Anand, A. Elkholy, A. Elshazly**, R.K. Nandwana, S. Saxena, B. Young*, W.-S. Choi and P.K. Hanumolu, University of Illinois at Urbana-Champaign, *Oregon State University, **Intel Corporation

A phase interpolator (PI) based fractional divider is used to improve the quantization noise shaping properties of a 1-bit ΔΣ frequency-to-digital converter (FDC). Fabricated in 65nm CMOS process, the prototype calibration-free fractional-N Type-II PLL employs the proposed FDC in place of a high resolution TDC and achieves -102dBc/Hz in-band phase noise and 852fs$_{rms}$ integrated jitter (1k-40M) while generating 5.054GHz output from 31.25MHz input.

9.4 - 9:20 a.m.
A 12mW All-Digital PLL Based on Class-F DCO for 4G Phones in 28nm CMOS, F.-W. Kuo, R. Chen, K. Yen, H.-Y. Liao, C.-P. Jou, F.-L. Hsueh, M. Babaie*, and R.B. Staszewski*, TSMC, *Delft University

We propose a new architecture of an all-digital PLL (ADPLL) for advanced cellular radios that is optimized for 28nm CMOS. It is based on a wide tuning range, fine-resolution class-F DCO with only switchable metal capacitors and a phase-predictive TDC. The 8mW DCO emits -157dBc/Hz at 20MHz offset at ~2GHz carrier, while fully satisfying metal density rules. The 0.4mW TDC clocked at 40MHz achieves PVT-stabilized 6ps resolution for -108dBc/Hz in-band phase noise. FREF spur is ultra-low at <-94 dBc. The ADPLL supports a 2-point modulation and consumes 12mW while occupying 0.22mm^2, thus demonstrating both 72% power and 38% area reductions over prior records.

9.5 - 9:45 a.m.
A 0.37-to-46.5GHz Frequency Synthesizer for Software-Defined Radios in 65nm CMOS, J. Yin and H.C. Luong, Hong Kong University of Science and Technology

Employing a switched-transformer-based triple-band Q-VCO and a magnetically-tuned multi-mode triple-push x4 injection-locked frequency multiplier (ILFM), a CMOS SDR frequency synthesizer generates IQ LO signals continuously from 0.37GHz to 23.25GHz and differential LO signals from 23.25GHz to 46.5GHz. Implemented in 65-nm CMOS, the synthesizer measures phase noise of -94dBc/Hz in band and of -136dBc/Hz at 10MHz offset from 7.2GHz and RMS jitters between 0.43ps and 0.55ps across the whole frequency range while consuming 36 to 90mW and occupying an active area of 1.82mm2.

Session 10 - TAPA I
Oversampled ADCs

Thursday, June 12
Chairpersons: J. Paramesh, Carnegie Mellon University
M. Ito, Renesas Electronics Corporation

10.1 - 10:25 a.m.
A 75dB DR 50MHz BW 3rd Order CT-ΔΣ Modulator Using VCO-Based Integrators, B. Young, K. Reddy, S. Rao, A. Elshazly, T. Anand* and P.K. Hanumolu*, Oregon State University, *University of Illinois, Urbana-Champaign

A wide bandwidth, high sample rate 3rd order continuous-time delta sigma modulator using VCO-based integrators is presented. Non-idealities caused by VCOs at the modulator frontend are addressed using both circuit- and architecture-level techniques. Fabricated in a 65nm CMOS, the prototype modulator operates at 1.28GS/s and achieves a dynamic range of 75dB, SNR of 71dB in 50MHz bandwidth, while consuming 38mW of total power.

10.2 - 10:50 a.m.
A 23mW, 73dB Dynamic Range, 80MHz BW Continuous-Time Delta-Sigma Modulator in 20nm CMOS, S. Ho, C.-L. Lo, Z. Ru and J. Zhao*, MediaTek, *Analog Devices

A 23mW, 80MHz BW, 73dB dynamic range continuous-time ΔΣ modulator in 20nm CMOS is presented. The modulator operates from 1.0/1.2/1.5V supplies. Power is minimized by combining a low OSR, fast digital excess loop delay compensation scheme, and several techniques to minimize delay in the feedback path. The result is a highly power efficient modulator that achieves an FOM(DR) of 168dB.

10.3 - 11:15 a.m.
A 97.3 dB SNR, 600 kHz BW, 31mW Multibit Continuous Time Δ∑ ADC, A. Bandyopadhyay, R. Adams, K. Nguyen, P. Baginski, D. Lamb and T. Tansley, Analog Devices Inc.

A continuous time 5-bit feed forward Δ∑ ADC architecture is presented, which measures 97.3 dB SNR, over 600 kHz bandwidth while consuming 31 mW/channel. This performance is achieved by using an ISI mitigation scheme and a 2nd-order DEM for 3-level DACs along with analog low power techniques. The 0.99mm^2/channel chip was fabricated in 0.18um CMOS process, and achieves a FOM of 171.8 dB.

10.4 - 11:40 a.m.
An 8.5MHz 67.2dB SNDR CTDSM with ELD Compensation Embedded Twin-T SAB and Circular TDC-based Quantizer in 90nm CMOS, C.-H. Weng, T.-A. Wei, E. Alpman, C.-T. Fu*, Y.-T. Tseng and T.-H. Lin, National Taiwan University, *Intel Corporation

A power-efficient continuous-time delta-sigma modulator (CTDSM) employing a single-amplifier biquad (SAB) based topology is proposed. The modulator incorporates a proposed twin-T SAB topology where the excess loop delay (ELD) is compensated by injecting a feedback signal into an internal node of the SAB while cooperating with an additional phase-compensation resistor. A low-power time-to-digital converter (TDC) with an embedded data weighted averaging (DWA) function is proposed as the quantizer, which mitigates the mismatch issue in the feedback DACs. Fabricated in 90nm CMOS, the proposed CTDSM achieves peak SNDR of 67.2dB over an 8.5MHz signal bandwidth, while consuming 4.3mW at 300MHz sampling frequency, and scores a FoM of 135fJ/conv.-step.

Session 11 - HONOLULU

Advanced Wireline Techniques

Thursday, June 12

Chairpersons: R. Navid, Rambus Inc.
K. Sunaga, NEC Corporation

C11.1 - 10:25 a.m.

A 0.8V, 560fJ/bit, 14Gb/s Injection-Locked Receiver with Input Duty-Cycle Distortion Tolerable Edge-Rotating 5/4X Sub-Rate CDR in 65nm CMOS, H. Li, S. Chen*, L. Yang*, R. Bai, W. Hu*, F. Zhong^, S. Palermo** and P. Chiang, Oregon State University, *Chinese Academy of Sciences,**Texas A&M University, ^ LSI Corporation

A quarter-rate forwarded-clock receiver utilizes an edge- rotating 5/4X sub-rate CDR for improved jitter tolerance with low power overhead relative to conventional 2X oversampling CDR systems. Low-voltage operation is achieved with efficient quarter-rate clock generation from an injection-locked oscillator (ILO) and through automatic independent phase rotator control that optimizes timing margin of each input quantizer in the presence of receive-side clock static phase errors and transmitter duty-cycle distortion (DCD). Fabricated in GP 65nm CMOS, the receiver operates up to 16Gb/s with a BER<10^{-12}, achieves a 1MHz phase tracking bandwidth, tolerates ±50%UI_{pp} DCD on input data, and has 14Gb/s energy efficiency of 560fJ/bit at V_{DD}=0.8V.

11.2 - 10:50 a.m.

A 56-Gb/s Receiver Front-End with a CTLE and 1-Tap DFE in 20-nm CMOS, T. Shibasaki, W. Chaivipas, Y. Chen, Y. Doi, T. Hamada, H. Takauchi, T. Mori, Y. Koyanagi and H. Tamura, Fujitsu Laboratories Ltd.

A 56-Gb/s receiver front-end suited for baud-rate clock recovery is demonstrated in 20-nm CMOS. Sharing the comparators for the data decision and phase detection minimizes the number of comparators in the front-end and reduces the power consumption. The front-end has a continuous-time linear equalizer followed by a 1-tap speculative decision-feedback equalizer. The front-end operates at 56Gb/s with a bit error rate of less than 10^{-12} with a 0.4UI margin in the bathtub curve. It occupies 0.27mm^2 and consumes 177mW of power from a 0.9-V supply.

11.3 - 11:15 a.m.

On-Chip Measurement of Data Jitter with Sub-Picosecond Accuracy for 10Gb/s Multilane CDRs, J. Liang, M.S. Jalali, A. Sheikholeslami, M. Kibune* and H. Tamura*, University of Toronto, *Fujitsu Laboratories Limited

On-chip jitter measurement is demonstrated in a 10Gb/s CDR by correlating the phase detector outputs of two adjacent CDR lanes. The RMS jitter of the received data and an estimate of the jitter's power spectral density are then extracted without using an external reference clock. Circuits implemented in 65nm CMOS measure random jitter ranging from 0.85ps to 1.89ps in PRBS31 data with no more than 100fs error compared to an 80GS/s real-time oscilloscope. Sinusoidal jitter of 0.89ps to 5.1ps is measured with a worst-case error of 580fS compared to the oscilloscope.

11.4 - 11:40 a.m.
A 48-mW 18-Gb/s Fully Integrated CMOS Optical Receiver with Photodetector and Adaptive Equalizer,
Q. Pan, Z. Hou, Y. Wang, Y. Lu, W.-H. Ki, K.C. Wang* and C.P. Yue, The Hong Kong University of Science and Technology, *Applied Science and Technology Research Institute

A 65-nm CMOS monolithic optical receiver IC with on-chip photodetector (PD) using the p-well/deep-n-well (PW/DNW) junction is presented for short-range optical communication using 850-nm wavelength. An adaptive continuous-time linear equalizer (CTLE) with 33-dB tunable gain is employed to compensate for the limited PD responsivity and bandwidth. For 850-nm optical PRBS-15 inputs, the receiver achieves record data rates and efficiencies of 9 Gb/s at 5.35 pJ/bit and 18 Gb/s at 2.7 pJ/bit with the PD biased in 0.5-V standard mode and 12.3-V avalanche mode, respectively. The core chip occupies 0.23 mm^2 and consumes 48 mW.

Luncheon & Executive Panel Discussion

Thursday 6/12, 12:15 pm

Emerging Semiconductor Industry Trends and Implications

Moderator: Dan Hutcheson, CEO and Chairman of VLSI Research Inc and author of The Chip Insider

Looking past traditional scaling that has driven semiconductor industry over the last few decades, we see a new paradigm unfolding around us. Emerging trends and applications information technology are fueling unprecedented demands on information ubiquity – user-friendly, mobile anywhere, any time. This has opened up the need for a new class of systems – both mobile and fixed – which are in turn driving the need for a new class of device technologies, circuits and designs. The impact of this paradigm shift on semiconductor industry professionals and researchers in the academic community is profound. For example, if wearable computing or IoT become increasingly larger segments of application space - what technology/system/ manufacturing/economic implications does this have? Will we need to push harder on new materials and low power technologies? Will we need to think of new ways to integrate dissimilar components (wireless, NVM, RF/Analog/digital, MEMS, batteries etc.) or traditional SOC/SIP suffice? The panel will deliberate on this topic and discuss trends, applications that are shaping around us, industry needs, infrastructural/manufacturing gaps and economic challenges.

Panelists:

Scott DeBoer, Micron
Venu Menon, Texas Instruments
Om Nalamasu, AMAT
Yoshifumi Okamoto, Panasonic
Gary Patton, IBM
Jack Sun, TSMC

Session 12 - TAPA I

Circuits / Technology Joint Focus Session: Non-Volatile and Emerging Memory

Thursday, June 12
Chairpersons: J. DeBrosse, IBM
H. Yamauchi, Fukuoka Institute of Technology

12.1 - 1:30 p.m.

Highly Reliable and Low-Power Nonvolatile Cache Memory with Advanced Perpendicular STT-MRAM for High-Performance CPU, H. Noguchi, K. Ikegami, N. Shimomura, T. Tetsufumi, J. Ito and S. Fujita, Toshiba Corporation

This paper presents a novel nonvolatile last level cache (LLC) based on the advanced perpendicular STT-MRAM to reduce the total power consumption of LLC. The presented LLC has novel readout circuit with the dual-sensing salvation scheme that enhances reliability of STT-MRAM along with typical error-correcting code (ECC). The comparison of CPU performance per power with SRAM-based, embedded

DRAM-based and conventional STT-MRAM-based LLCs indicates that the presented novel nonvolatile LLC is the most suitable for large LLC.

12.2 - 1:55 p.m.

ReRAM-based 4T2R Nonvolatile TCAM with 7x NVM-Stress Reduction, and 4x Improvement in Speed-WordLength-Capacity for Normally-Off Instant-On Filter-Based Search Engines Used in Big-Data Processing, L.-Y. Huang, M.-F. Chang, C.-H. Chuang, C.-C. Kuo, C.-F. Chen, G.-H. Yang*, H.-J. Tsai*, T.-F. Chen*, S.-S. Sheu**, K.-L. Su**, F.T. Chen**, T.-K. Ku**, M.-J. Tsai**, M.-J. Kao**, National Tsing Hua University, *National Chiao Tung University, **ITRI

This study proposes an RC-filtered stress-decoupled (RCSD) 4T2R nonvolatile TCAM (nvTCAM) to 1) suppress match-line (ML) leakage current from match cells ($I_{ML\text{-}M}$), 2) reduce ML parasitic load (C_{ML}), 3) decouple NVM-stress from wordlength (WDL) and $I_{ML\text{-}MIS}$. RCSD reduces NVM-stress by 7+x, and achieves a 4+x improvement in speed-WDL-capacity-product. A 128x32b RCSD nvTCAM macro was fabricated using HfO ReRAM and an 180nm CMOS. This paper presents the first ReRAM-based nvTCAM featuring the shortest (1.2ns) search delay (T_{SD}) among nvTCAMs with WDL≧32b.

12.3 - 2:20 p.m.

A Low Power and Ultra High Reliability LDPC Error Correction Engine with Digital Signal Processing for Embedded NAND Flash Controller in 40nm CMOS, W. Lin, S.-W. Yen, Y.-C. Hsu, Y.-H. Lin, L.-C. Liang, T.-C. Wang, P.-Y. Shih, K.-H. Lai, K.-Y. Cheng and C.-Y. Chang*, Phison Electronics Corp., *National Chiao Tung University

A multi-mode Low-Density Parity-Check (LDPC) error correction engine with a Digital Signal Processing (DSP) module is presented for low power and ultra high reliability NAND Flash memory controllers. The DSP module improves the reliability of the storage systems via calculating the adaptive reliability information and translating the information into Log-Likelihood Ratio (LLR) for soft bit decoding. According to the experiment results on sub-20nm Triple Level per Cell (TLC) NAND Flash memory, the retention ability of LDPC with DSP is a 20 times improvement over BCH code and 2 to 5 times improvement over conventional LDPC. Moreover, the proposed decoder reaches a throughput over 400MB/s as well as a power consumption of 21.8mW under 40nm CMOS technology at 45 bit errors.

12.4 - 2:45 p.m.

Application-Aware Solid-State Drives (SSDs) with Adaptive Coding, S. Tanakamaru, Y. Kitamura, S. Yamazaki, T. Tokutomi and K. Takeuchi, Chuo University

Application-aware solid-state drives (SSDs) with 2 adaptive coding schemes to improve reliability are presented. In NAND flash memory, a direct reliability trade-off exists between write/erase (W/E) cycle and data-retention (DR) time. Thus, SSDs can be used for applications that have long DR time and low W/E cycles, or short DR time with high W/E cycles. The n-out-of-8 level cell (nLC) scheme is proposed for low-cost, long-term, archive storage which is indispensable to preserve human digital data. nLC eliminates the memory states of the Triple-Level Cell (TLC) NAND flash memory from 8 to 7…4 levels. Universal asymmetric coding (UAC) is also proposed for cloud/security camera/enterprise storage environments which require high endurance but shorter DR time. Both nLC and UAC optimize coding based on the applications' required W/E cycle and DR. Bit-error rates (BERs) are improved by 79% and 52% with *n*LC and UAC, respectively.

Medical Imaging

Thursday, June 12
Chairpersons: D. Sylvester, University of Michigan
M. Ikeda, The University of Tokyo

13.1 - 1:30 p.m.
An Impedance and Multi-wavelength Near-infrared Spectroscopy IC for Non-invasive Blood Glucose Estimation, K. Song, U. Ha, S. Park and H.-J. Yoo, KAIST

A multi-modal spectroscopy IC combining the impedance spectroscopy (IMPS) and the multi-wavelength near-infrared spectroscopy (mNIRS) is proposed for high precision non-invasive glucose level estimation. A frequency sweep (10kHz - 76kHz) sinusoidal oscillator (FSSO) is proposed for high resolution (500 steps) for IMPS. The proposed FSSO uses both linear digital frequency switching and continuous analog frequency sweep. The output voltage swing of the FSSO is stabilized by an adaptive gain control (AGC). The measurement results of IMPS and mNIRS are combined by an artificial neural network (ANN) in external smart device so that mean absolute relative difference (mARD) is enhanced to 8.3% from 15% of IMPS, 15% - 20% of mNIRS. A proposed 12.5mm^2 0.18um CMOS chip consumes peak power of 38mW at 1.5V.

13.2 - 1:55 p.m.
A 6.5/11/17.5/30-GHz High Throughput Interferometer-based Reactance Sensors using Injection-Locked Oscillators and Ping-Pong Nested Chopping, J.-C. Chien, M. Anwar*, E.-C. Yeh, L. Lee and A. Niknejad, University of California, Berkeley, *University of California, San Francisco

A series of high-sensitivity reactance sensors at 6.5/11/17.5/30-GHz is demonstrated for dielectric spectroscopy sensing on a single micron-size biological specimen. SNR is enhanced with the combination of interferometry and injection-locked oscillator sensors while the offset incurred by chopping-ripple is reduced through ping-pong nested chopping. The sensors achieve a sensitivity of less than 1.25 aF at 100-kHz, enabling label-free cellular detection as a new analytical tool.

13.3 - 2:20 p.m.
A 64×64 1200fps CMOS Ion-Image Sensor with Suppressed Fixed-Pattern-Noise for Accurate High-throughput DNA Sequencing, X. Huang, F. Wang, J. Guo, M. Yan, H. Yu and K.S. Yeo, Nanyang Technological University

A 64x64 CMOS ion-image sensor is demonstrated towards accurate high-throughput DNA sequencing. Dual-mode (pH/ image) sensing is performed with ion-sensitive field-effect transistor (ISFET) fabricated in standard CMOS image sensor (CIS) process. After addressing physical locations of DNA slices by optical contact imaging, local pH for one DNA slice can be mapped to its physical address with accurate correlation. Moreover, pixel-to-pixel ISFET threshold voltage mismatch is reduced by correlated double sampling (CDS) readout. Measurements show a sensitivity of 103.8mV/pH and fixed-pattern-noise (FPN) reduction from 4% to 0.3% with speed of 1200fps.

13.4 - 2:45 p.m.
A 4.7T/11.1T NMR Compliant Wirelessly Programmable Implant for Bio-Artificial Pancreas *in vivo* Monitoring, W. Turner and R. Bashirullah, University of Florida

This paper presents the design, implementation, and nuclear magnetic resonance (NMR) measurements of a wireless, magnetic compliant, implant for the noninvasive monitoring of a bio-artificial pancreas post-implantation. The device increases NMR image signal sensitivity by 3.8dB and 2.6dB in 4.7T (200MHz) and 11.1T (470MHz) magnetic field strengths respectively. The device supports sustained reliable operation through a strongly coupled resonance wireless powering scheme in addition to improving high-resolution image SNR up to 73%.

Session 14 - TAPA I
Circuits / Technology Joint Focus Session: SRAM and DRAM

Thursday, June 12
Chairpersons: L. Cheng, Oracle
K. Sohn, Samsung Electronics Co., Ltd.

14.1 - 3:25 p.m.
A 512-kb 1-GHz 28-nm Partially Write-Assisted Dual-Port SRAM with Self-Adjustable Negative Bias Bitline, S. Tanaka, Y. Ishii, M. Yabuuchi, T. Sano*, K. Tanaka, Y. Tsukamoto, K. Nii and H. Sato, Renesas Electronics, *Renesas System Design

We propose partially write-assisted 2-read/write dual-port (DP) SRAM in 28-nm technology. Our write-assist circuit with metal-coupled capacitance can generate such negative bitline bias that is adjustable to any bit-word configurations, flexibly. Effectively applying assist biases only to sub-blocks with margin-less bits can reduce power overhead with Vmin improved. A test chip including proposed 512-kb DP SRAM macro is designed using 28nm HKMG technology, from which we successfully observed 120 mV Vmin improvement and 21% power reduction compared to a conventional assist.

14.2 - 3:50 p.m.
Low V_{MIN} 20nm Embedded SRAM with Multi-voltage Wordline Control Based Read and Write Assist Techniques, M. Bhargava, Y.K. Chong, V. Schuppe, B. Maiti, M. Kinkade, H.-Y. Chen, A.W. Chen, S. Mangal, J. Wiatrowski, G. Gouya, A. Baradia, S. Thyagarajan and G. Yeung, ARM Inc.

Measured results of V_{MIN} from 20nm SRAM arrays with read and write assist techniques are presented for multiple flavors of bitcell. A novel assist technique is presented, that provides both read and write assist by controlling only the voltage of wordline (WL) and without using a separate supply voltage. The WL-drivers use a WL float technique to reduce the dc-path current compared to existing WL under-drive read assist designs. The assist technique resulted in a V_{MIN} improvement of 143mV for the high-density 6T (6T-HD) SRAM, 96mV for the high-speed 6T (6T-HS) SRAM, and 86mV for the 8T dual-port (DP) SRAM.

14.3 - 4:15 p.m.
A 4.68Gb/s Belief Propagation Polar Decoder with Bit-Splitting Register File, Y.S. Park, Y. Tao, S. Sun and Z. Zhang, University of Michigan

A 1.48mm^2 1024-bit belief propagation polar decoder is designed in 65nm CMOS. A unidirectional processing reduces the memory size to 45Kb, and simplifies the processing element. A double-column 1024-parallel architecture enables a 4.68Gb/s throughput. A bit-splitting latch-based register file accommodates logic in memory for an 85% density. The architecture and circuit techniques reduce the

power to 478mW for an efficiency of 15.5pJ/b/iteration at 1.0V. At 475mV, the efficiency is improved to 3.6pJ/b/iteration for a throughput of 780Mb/s.

14.4 - 4:40 p.m.
Early Detection and Repair of VRT and Aging DRAM Bits by Margined in-field BIST, B. Kleveland, J. Choi, J. Kumala, P. Adam, P. Chen, R. Chopra, A. Cruz, R. David, A. Dixit, S. Doluca, M. Hendrickson, B. Lee, M. Liu, M. Miller, M. Morrison, B. Na, J. Patel, D. Sikdar, M. Sporer and C. Szeto, A. Tsao, J. Wang, D. Yau, W. Yu, MoSys, Inc.

Studies on DRAMs in high performance computing clusters and servers have concluded that memory errors in the field are dominated by hard faults, which cannot be fixed by scrubbing. Our accelerated life testing of embedded DRAM products shows that bits can degrade gradually. We propose improving system availability by performing in-field repair at the chip level. One page at a time, user data is copied to a temporary page and the page is stress tested with a long effective refresh time. Degrading memory cells are detected and repaired before any errors occur. Our 576 Mb embedded DRAM at 1.5 GHz in a 40nm CMOS technology with 8 metal layers achieves improved resilience to both aging memory cells and cells with variable retention time (VRT). Un-interrupted user access of 6 billion 72-bit read and write operations per second is maintained during background repair.

14.5 - 5:05 p.m.
2nd Generation Embedded DRAM with 4X Lower Self Refresh Power in 22nm Tri-Gate CMOS Technology, M. Meterelliyoz, F.H. Al-amoody, U. Arslan, F. Hamzaoglu, L. Hood, M. Lal, J.L. Miller, A. Ramasundar, D. Soltman, I. Wan, Y. Wang and K. Zhang, Intel Corporation

2nd generation 1Gbit 2GHz Embedded DRAM (eDRAM) with 4X lower self refresh power compared to prior generation is developed in 22nm Tri-Gate CMOS technology. Retention time has been improved by 3X (300us@95°C) by process and design optimizations. Source synchronous clocking is integrated in the design to reduce clock power without penalizing bandwidth. Charge pump power is reduced by 4X by employing comparator based regulation. Temperature controlled refresh enables minimum refresh power at all temperature conditions.

Session 15 - HONOLULU
Millimeter-Wave & Cellular Radios

Thursday, June 12
Chairpersons: A. Cathelin, STMicroelectronics
K. Agawa, Toshiba Corporation

15.1 - 3:25 p.m.
A PVT-Variation Tolerant Fully Integrated 60 GHz Transceiver for IEEE 802.11ad, T. Tsukizawa, A. Yoshimoto, H. Komori, K. Miyanaga, R. Kitamura, Y. Morishita, M. Irie, Y. Nagaso, T. Watanabe, K. Takinami and N. Saito, Panasonic Corporation

A PVT tolerant fully integrated 60GHz transceiver for IEEE 802.11ad is presented. By introducing a newly proposed self-sensing LDO, the transceiver adjusts bias currents and the LDO output voltage for the PA to minimize the output power variation while relaxing the hot carrier injection (HCI) degradation. The

measurement shows excellent robustness against PVT variations, demonstrating only 5dB output power variation over -20°C to 85°C across process corners.

15.2 - 3:50 p.m.
A 94GHz Duobinary Keying Wireless Transceiver in 65nm CMOS, Y.-L. Chen, C. Kao, P.-J. Peng and J. Lee, National Taiwan University

This paper introduces a 94GHz duobinary keying wireless transceiver for point-to-point communications. It presents bandwidth efficiency twice as much as an OOK system and requires no carrier recovery and baseband circuitry to reduce power consumption. Designed and fabricated in 65nm CMOS, the transceiver achieves a 2.0-Gb/s data link with BER < 10^{-9} while consuming a total power of 265mW.

15.3 - 4:15 p.m.
A Receiver Architecture for Intra-Band Carrier Aggregation, S.-C. Hwu and B. Razavi, University of California, Los Angeles

Carrier aggregation is an attractive approach to increasing the data rate in wireless communication. For example, Release 10 of the LTE mobile phone standard supports both intra-band and inter-band aggregation. A receiver supporting several carriers may simply employ multiple signal paths and corresponding frequency synthesizers but at the cost of high power and extremely stringent isolation requirements among the local oscillators. This research introduces an efficient carrier aggregation receiver architecture that employs one receive path and a single synthesizer. The block-downconversion scalable receiver translates all of the channels to the baseband and utilizes a new digital image rejection technique to reconstruct the signals. A receiver prototype realized in 45-nm CMOS technology along with an FPGA back end provides an image rejection ratio of at least 70 dB across the entire band with a noise figure of 3.8 dB while consuming 15 mW.

15.4 - 4:40 p.m.
A +22dBm IIP3 and 3.5dB NF Wideband Receiver with RF and Baseband Blocker Filtering Techniques, H. Hedayati, V. Aparin* and K. Entesari, Texas A&M University, *Qualcomm

The real challenge in designing wide-band receivers is the ability to tolerate out of band blockers. In this paper, different blocker rejection techniques are proposed to significantly improve the linearity. The blockers are first rejected prior to the LNA, then, a novel base-band blocker filtering technique further rejects the blockers at the TIA input. A dual mixer architecture is also employed to further attenuate blockers. Finally, a very low impedance TIA is designed to improve the linearity of the entire receiver chain. The receiver has an IIP3 of +22 dBm, which is improved by 20 dB, IIP2 of +70dBm and a NF of 3.5 dB in 0.18 μm CMOS technology.

Circuits Rump Session
Thursday, June 12, 8:00 p.m. – 10:00 p.m.

R-1: Lessons and Challenges for Future Mixed-Signal, RF, and Memory Circuits

Organizers: P. Hanumolu, University of Illinois, Urbana-Champaign
N. Lu, Etron Technology, Inc.

Moderators: T. Lee, Stanford University
N. Lu, Etron Technology, Inc.

Designing mixed-signal circuits is prone with pitfalls. Degrading transistor performance combined with lack of poor models and fast large-scale simulators further exacerbate classical circuit problems. Is it possible to achieve 1st silicon success under this uncertainty or some of the mistakes inevitable? Experts from industry and academia will address this question and present their perspectives. They will share lessons learned in their own careers and present challenges for mixed-signal, RF and memory chips going forward. Each of the panelists will be asked to highlight the key bottlenecks in achieving 1st silicon success and outline ways to address them. The panelists will also discuss these circuits when applied to interconnect technologies such as the 3D/2.5D integration.

Panelists:
A. Abidi, UCLA
M. Bauer, Micron
J.S Choi, Samsung
C. Mangelsdorf, ADI
A. Matsuzawa, Tokyo Institute of Technology
U-K Moon, Oregon State University
B. Nauta, University of Twente
K. Zhang, Intel

R-2: What Should Circuit Designers Do in an Era of System Level Design?

Organizers: S. Dillen, Qualcomm
S. Dosho, Panasonic Corporation

Moderator: J. Rabaey, University of California, Berkeley

As technology scaling continues to follow Moore's law, both the manufacturing cost and time to market (TTM) are becoming exorbitant. Conversely, system-based design using licensed IP in an ASIC flow, or FPGA-based design can significantly reduce design time and thus time to market. There are two parts to this complicated problem. First, board-level system designers can switch to using a reconfigurable FPGA chip rather than going through the expensive, time-consuming process of developing a custom ASIC solution. While FPGA power, performance and area (PPA) are generally worse, the increasing cost and TTM of a custom solution combined with improving FPGA PPA metrics may result in higher adoption of this solution. Similarly, even in a custom ASIC design, foundry and foundry-partners offer many IP solutions directly to customers which can lead to a reduction in full-custom IP design, reduce risk and TTM.

On the other hand, deep sub-micron technology challenges and designing circuits with good PPA metrics require more detailed circuit design and understanding. Also, adapting quickly to new design

requirements and interface standards could require custom solutions in order to capture or maintain a market leadership position.

Will custom VLSI design be confined to a niche market or will VLSI circuit designers still play an integral role in the design process as this design evolution continues? A panel of VLSI circuit design experts will present their opinions on this topic and discuss what is the future of VLSI circuit design.

Panelists:

S. Goto, Waseda University
C-M Hung, MediaTek
S. Naffziger, AMD
B. Nikolic, University of California, Berkeley
S. Ryu, Samsung
J. Savoj, Xilinx
E. Terzioglu, Qualcomm
J. Warnock, IBM

Session 16 - TAPA I
SOC Circuits & Processors

Friday, June 13
Chairpersons: T. Burd, Advanced Micro Devices
K. Fujii, NTT Microsystem Integration Labs

16.1 - 8:05 a.m.

340mV-1.1V, 289Gbps/W, 2090-gate NanoAES Hardware Accelerator with Area-Optimized Encrypt/Decrypt GF(2^4)^2 Polynomials in 22nm Tri-gate CMOS, S. Mathew, S. Satpathy, V. Suresh, H. Kaul, M. Anders, G. Chen, A. Agarwal, S. Hsu, and R. Krishnamurthy, Intel Corporation

An on-die, lightweight nanoAES hardware accelerator is fabricated in 22nm tri-gate CMOS, targeted for ultra-low power mobile SOCs. Compared to conventional 128-bit AES implementations, this design uses an 8-bit Sbox daTAPAth along with ShiftRow byte-order processing to compute all AES rounds in native GF(2^4)^2 composite-field. This approach along with a serial-accumulating MixColumns circuit, area-optimized encrypt and decrypt Galois-field polynomials and integrated on-the-fly key generation circuit results in a compact 2090-gate design, enabling peak energy-efficiency of 289Gbps/W and AES-128 encrypt/decrypt throughput of 432/671Mbps with total energy consumption of 4.7/3nJ measured at 0.9V, 25°C.

16.2 - 8:30 a.m.

R-Processor: 0.4V Resilient Processor with a Voltage-Scalable and Low-Overhead In-Situ Error Detection and Correction Technique in 65nm CMOS, S. Kim and M. Seok, Columbia University

This paper presents a design approach for upgrading the resiliency of ultra-low-voltage (ULV) microprocessors through a voltage-scalable and low-overhead in-situ error detection and correction (EDAC) technique. Particular efforts are made to overcome the poor voltage scalability and area/energy/throughput overhead of the existing EDAC techniques when applied to ULV designs. The 0.4V, 16b microprocessor employing the proposed EDAC and dynamic frequency scaling schemes is demonstrated in 65nm. The microprocessor can (1) automatically modulate fCLK based on error flags across static/slow variations and (2) in-situ detect and correct the errors from fast dynamic variations, virtually eliminating timing margins. At a typical process/voltage/temperature (PVT) corner, the

proposed design achieves 4.9× throughput and 59% energy efficiency improvement at only 9.5% area overhead over the baseline design under the worst-case timing margin.

16.3 - 8:55 a.m.

A 7.11mJ/Gb/Query Data-Driven Machine Learning Processor (D^2MLP) for Big Data Analysis and Applications, C.-H.Tsai, T.-Y. Wu*, S.-Y. Hsu, C.-C. Chu, F.-J. Ku, Y.-S. Laio, C.-L. Chen, W.-H. Wong*, H.-C. Chang and C.-Y. Lee, National Chiao Tung University, *Stanford University

A data-driven machine learning processor (D^2MLP) with MIMD architecture is designed for big data analysis. Adopting the configurable counting engine array with 3-layer dimension merging, the D^2MLP processes maximal 1-128/1024 dimensional data with parallel 64/8 queries in learning stage. Implement in 90nm CMOS technology, the D^2MLP achieves 219.9x and 8.2x faster processing time than CPU and GPGPU, respectively. In application phase, maximal 22.7k 128-class classifications/s are performed with the learned density model. Operated at 1.0V and 165MHz, the D^2MLP demonstrates an energy-efficient solution for learning and classification with 7.11mJ/Gb/query and 2.3μJ/classification, respectively.

16.4 - 9:20 a.m.

A Local EM-Analysis Attack Resistant Cryptographic Engine with Fully-Digital Oscillator-Based Tamper-Access Sensor, N. Miura, D. Fujimoto, D. Tanaka, Y.-i. Hayashi*, N. Homma*, T. Aoki* and M. Nagata, Kobe University, *Tohoku University

A cryptographic engine (CE) resistant to local EM-analysis attacks (L-EMAs) is developed. An LC-oscillator-based tamper-access sensor detects a micro EM-probe approach and therefore protects the secret key information. A fully-digital sensor circuit with a reference-free dual-coil sensing scheme and a ring-oscillator-based one-step digital sensor calibration reduces the sensor area overhead to 1.6%. The sensor intermittently operates in interleave between CE operations, which saves power and performance penalty to 7.6% and 0.2%. A prototype in 0.18μm CMOS successfully demonstrates L-EMA attack detection and key protection for the first time.

16.5 - 9:45 a.m.

A Self-Aware Microprocessor SoC using Energy Monitors Integrated into Power Converters for Self-Adaptation, Y. Sinangil, S.M. Neuman, M.E. Sinangil*, N. Ickes, G. Bezerra, E. Lau, J.E. Miller, H.C. Hoffmann**, S. Devadas and A.P. Chandraksan, Massachusetts Institute of Technology, *NVIDIA, **University of Chicago

This paper presents a self-aware processor with energy monitoring circuits that can measure actual energy consumption of the key blocks. The monitors are embedded into on-chip DC/DC converters and generate results within 10% of accuracy with minimal power (<0.1%) and area (<1%) overhead. Our system, which is implemented in 0.18μm technology, is designed to be voltage scalable from 1.8V down to 0.6V. Low-voltage SRAM operation is made possible through the use of 8T bit-cells and write-assists. The d-caches are designed to be re-configurable in associativity and size to adapt to compute- versus cache-bound phases of applications. Cache configuration is performed in < 3 clock cycles including tag invalidation. These hardware features enable a software self-aware computation engine (SEEC) to dynamically adapt the processor to meet performance and energy goals. Measurement results show that up to 8.4× energy savings can be achieved with DVFS and self-adaptation.

Session 17 - TAPA II

Image Sensors

Friday, June 13

Chairpersons: J. Tschanz, Intel Corporation
H. Wakabayashi, Sony Corporation

17.1 - 8:05 a.m.

A Millimeter-Scale Wireless Imaging System with Continuous Motion Detection and Energy Harvesting, G. Kim, Y. Lee, Z. Foo, P. Pannuto, Y.-S. Kuo, B. Kempke, M. Ghaed, S. Bang, I. Lee, Y. Kim, S. Jeong, P. Dutta, D. Sylvester and D. Blaauw, University of Michigan

We present a 2×4×4mm^3 imaging system complete with optics, wireless communication, battery, power management, solar harvesting, processor and memory. The system features a 160×160 resolution CMOS image sensor with 304nW continuous in-pixel motion detection mode. System components are fabricated in five different IC layers and die-stacked for minimal form factor. Photovoltaic (PV) cells face the opposite direction of the imager for optimal illumination and generate 456nW at 10klux to enable energy autonomous system operation.

17.2 - 8:30 a.m.

A 65-nm 0.5-V 17-pJ/frame.pixel DPS CMOS Image Sensor for Ultra-Low-Power SoCs Achieving 40-dB Dynamic Range, D. Bol, G. de Streel, F. Botman, A.K. Lusala and N. Couniot, Université catholique de Louvain

We propose a CMOS image sensor operating at ultra-low voltage (ULV) in a 65-nm low-power (LP) CMOS logic process for ultra-low-power SoC integration. Energy of 17-pJ/frame.pixel and 4×4-µm pixel size with 57-% fill factor are achieved at 0.5 V with digital pixel sensor (DPS) and time-based readout while reaching 40-dB dynamic range (DR) despite high leakage currents and Vt variability, thanks to delta-reset sampling (DRS) as well as gating and adaptive body biasing (ABB) of the 2-transistor (2-T) in-pixel comparator.

17.3 - 8:55 a.m.

An On-chip 72×60 Angle-Sensitive Single Photon Image Sensor Array for Lens-Less Time-Resolved 3-D Fluorescence Lifetime Imaging, C. Lee, B. Johnson and A. Molnar, Cornell University

We present a 72×60, angle-sensitive single photon avalanche diode (A-SPAD) array, able to perform lens-less 3-D fluorescent lifetime imaging. The pixels use integrated diffraction gratings to extract incident angle, enabling 3-D localization and SPADs to resolve timing information, rejecting high-powered UV stimulus and mapping the lifetimes of different fluorescent sources. The chip integrates pixel-level counters, and shared timing circuitry, and is implemented in unmodified 180nm CMOS.

17.4 - 9:20 a.m.

320x240 Oversampled Digital Single Photon Counting Image Sensor, N.A.W. Dutton, L. Parmesan, A.J. Holmes*, L.A. Grant* and R.K. Henderson, University of Edinburgh, *STMicroelectronics Imaging Division

A 320x240 single photon avalanche diode (SPAD) based single photon counting image sensor is implemented in 0.13µm imaging CMOS with state of the art 8µm pixel pitch at 26.8% fill factor. The imager is demonstrated operating as a global shutter (GS) oversampled binary image sensor reading out

at 5.14kFPS. Frames are accumulated in real time on FPGA to construct a 256 photon/8bit output image at 20FPS.

17.5 - 9:45 a.m.
A 3.7M-pixel 1300-fps CMOS Image Sensor with 5.0G-Pixel/s High-Speed Readout Circuit, S. Okura, O. Nishikido, Y. Sadanaga, Y. Kosaka, N. Araki, K. Ueda, M. Tachibana and F. Morishita, Renesas Electronics Corporation

A 5.0G-pixel/s readout circuit for 15.3mm×8.6mm optical size, 3.7M-pixel, 1300 fps, and digital output image sensor is presented. To achieve 5.0G-pixel/s readout rate, the high speed column readout circuit is introduced. The novel pixel readout, A/D conversion, and digital data transfer schemes are introduced to realize the readout rate and to reduce the interference noise. The 1 horizontal (1H) readout time is realized to be 1.0us.

Session 18 - TAPA I
Biomedical Circuits & Systems

Friday, June 13
Chairpersons: N. Van Helleputte, imec
C.-Y. Lee, National Chiao Tung University

18.1 - 10:25 a.m.
A 4.78mm^2 Fully-Integrated Neuromodulation SoC Combining 64 Acquisition Channels with Digital Compression and Simultaneous Dual Stimulation, D. Yeager, W. Biederman, N. Narevsky, J. Leverett, R. Neely, J. Carmena, E. Alon and J. Rabaey, University of California, Berkeley

A 65nm CMOS 4.78mm^2 integrated neuromodulation SoC consumes 417µW from a 1.2V supply while operating 64 acquisition channels with epoch compression at an average firing rate of 50Hz and engaging two stimulators with a pulse width of 250µs/phase, differential current of 150µA, and a pulse frequency of 100Hz. Compared to the state of the art, this represents the lowest area and power for the highest integration complexity achieved to date.

18.2 - 10:50 a.m.
A 266nW Multi-Chopper Amplifier with 1.38 Noise Efficiency Factor for Neural Signal Recording, Y.-P. Chen, D. Blaauw and D. Sylvester, University of Michigan

A low power high efficiency neural signal recording amplifier with a novel multi-chopper technique is proposed and implemented in 180nm CMOS. The input referred rms noise is 1.54µV (1-500Hz) with 266nA tail current and PSRR/CMRR of 92/89dB. The result corresponds to a 1.38 noise efficiency factor, which is the best reported among current state-of-the-art amplifiers.

18.3 - 11:15 a.m.
An Implantable Continuous Glucose Monitoring Microsystem in 0.18µm CMOS, M.H. Nazari, M. Mujeeb-U-Rahman and A. Scherer, California Institute of Technology

We present a fully implantable subcutaneous continuous glucose monitoring (CGM) microsystem on CMOS platform. The proposed design incorporates electrochemical sensing technique using an ultra-low-power potentiostatic system. It is wirelessly powered through an inductive coupling at 900MHz and

supports bidirectional data communication with an outside reader. A low-power potentiostat and an ADC record the on-chip sensor glucose readout. Pt and Ag/AgCl on-chip electrodes are post-fabricated and functionalized *in situ* by glucose oxidase enzyme to enable glucose measurement. The 1.4×1.4×0.25mm^3 prototype fabricated in a 0.18µm CMOS technology was validated in glucose measurements. Total power consumption of the system is 6µW.

18.4 - 11:40 a.m.
A Single-chip Encrypted Wireless 12-Lead ECG Smart Shirt for Continuous Health Monitoring, T. Morrison, J. Silver and B. Otis, University of Washington

An electrocardiography SoC is integrated into a form-fitting textile along with flexible electrodes, battery and antenna. Clinically standard 12-lead ECG is recorded from this "smart shirt." The data is encrypted and wirelessly transmitted via an on-chip ISM band radio and flexible antenna allowing secure, continuous cardiac monitoring on a smartphone while dissipating less than 1mW.

Session 19 - TAPA II
DACs and Mixed-Signal Techniques

Friday, June 13
Chairpersons: G. Van der Plas, imec
Y. Tomita, Fujitsu Laboratories, Ltd.

19.1 - 10:25 a.m
A 12-bit Hybrid DAC with 8GS/s Unrolled Pipeline Delta-Sigma Modulator Achieving >75dB SFDR Over 500MHz in 65nm CMOS, S. Su, T.-I Tsai, P. Sharma and M. Chen, University of Southern California

1. This paper proposes new architechture(Hybrid structre with split Nyqist and Delta-Sigma Paths) of DAC that minimizes the complexity of analog circuit, such as current steerin cell, and leveraging high-speed digital computation. 2. This DAC has SFDR 91-75dB covers the Nyquist Band(0-500MHz). 3. Digital Calibration for MSB mismatch via LSB through delta sigma path relax the matching requirement of these current steering cells.

19.2 - 10:50 a.m.
A 960MS/s DAC with 80dB SFDR in 20nm CMOS for Multi-Mode Baseband Wireless Transmitter, W.-H. Tseng and P.-C. Chiu, MediaTek

A 960MS/s calibrated digital-to-analog converter (DAC) and low pass reconstruction filter are fabricated in 20nm CMOS. The calibration is implemented without an extra analog-to-digital converter (ADC) by reconfiguring the filter as the integrator for an incremental ADC which is used to digitize DAC cell mismatch. The digital input to the DAC is compensated by a look-up table to correct DAC mismatch in real-time. Before calibration, DNL is -1.1/+0.7LSB and INL is -2.1/+0.3LSB. After calibration DNL and INL are improved to -0.2/+0.2LSB and -0.3/+0.2LSB respectively. This 10b DAC achieves 80dB SFDR after calibration, and occupies 0.01mm^2 for an I/Q DAC pair which is 12.5% of the area for an uncalibrated I/Q DAC pair.

19.3 - 11:15 a.m.

A 3nV/√Hz Programmable Gain/BW Mixed-Signal 4th Order Chebyshev High-Pass Filter for ADSL/VDSL Analog Front End in 28nm CMOS, H. Mehta, G. Krishnamurthy, M. Inerfield, F. Lin and T. Kwan, Broadcom Corporation

A fourth-order Chebyshev high-pass filter (HPF) that achieves input-referred noise of 3nV/sqrt(Hz), MTPR greater than 72dB, and power consumption of less than 81mW with 0.7mm^2 area in 28nm CMOS is presented. Area and power reductions are realized via a mixed-signal filter topology.

19.4 - 11:40 a.m.
A 110mW, 0.04mm^2, 11GS/s 9-bit Interleaved DAC in 28nm FDSOI with >50dB SFDR Across Nyquist, E. Olieman, A.-J. Annema and B. Nauta, University of Twente

A 9-bit 11GS/s current-steering (CS) digital-to-analog converter (DAC) is designed in 28nm FDSOI. The DAC uses two-times interleaving to suppress the effects of the main error mechanisms of CS DACs while its clock timing can be tuned by the back gates bias voltage of the multiplexer transistors. The DAC achieves higher than 50dB SFDR and less than -50dBc IM3 over Nyquist at a sampling rate of 11GS/s, occupying only 0.04mm2 and consuming 110mW from a single 1V supply.

Session 20 - TAPA I
DC/DC Buck Converters

Friday, June 13
Chairpersons: J.L. Nilles, Texas Instruments
C. Yoo, Hanyang University

20.1 - 1:30 p.m..
A 500 MHz, 68% Efficient, Fully On-Die Digitally Controlled Buck Voltage Regulator on 22nm Tri-Gate CMOS, H. Krishnamurthy, V. Vaidya, P. Kumar, G. Matthew, S. Weng, B. Thiruvengadam, W. Proefrock, K. Ravichandran and V. De, Intel Corporation

A fully on-die, digitally controlled, 500MHz switching, 250mA rated output buck Voltage Regulator (VR) implemented in 22nm Tri-Gate CMOS is presented. The silicon measured a peak efficiency of 68% and consumed an area of 0.6mm^2 (without output decoupling) with a power density of about 410 mW/mm^2. The paper also demonstrates a controller bandwidth of 43MHz; the highest reported to date for any digital controller, resulting in output voltage ramp rates as high as 10V/usec.

20.2 - 1:55 p.m.
A 10-25MHz, 600mA Buck Converter using Time-Based PID Compensator with 2µA/MHz Quiescent Current, 94% Peak Efficiency, and 1MHz BW, Q. Khan, S.J. Kim*, M. Talegaonkar*, A. Elshazly, A. Rao**, N. Griesert**, G. Winter**, W. McIntyre** and P.K. Hanumolu*, Oregon State University, *University of Illinois, Urbana-Champaign, **Texas Instruments

A time-based PID compensator that combines the advantages of both analog and digital controllers is used to implement a high frequency low quiescent current buck converter. Fabricated in 180nm CMOS process, the proposed buck converter operates over a wide range of switching frequencies (10-25MHz) and achieves better than 94% peak efficiency while consuming a quiescent current of only 2µA/MHz.

20.3 - 2:20 p.m.
A 40-MHz 85.8%-Peak-Efficiency Switching-Converter-Only Dual-Phase Envelope Modulator for 2-W 10-MHz LTE Power Amplifier, J. Sankman, M.K. Song and D. Ma, The University of Texas at Dallas

In conventional envelope modulators, a linear regulator is required to attain fast tracking, but it is a significant source of efficiency degradation. To eliminate the linear regulator, a dual-phase switching converter with synchronized adaptive voltage tracking (SAVT) control is employed. The SAVT control enables synchronization and fast hysteretic response for voltage tracking. To overcome the switching converter slew rate limit, a push-pull slew rate enhancer is implemented. The modulator is fabricated with a 0.18μm process and achieves 85.8% peak efficiency tracking a 10MHz LTE envelope.

20.4 - 2:45 p.m.
±3% Voltage Variation and 95% Efficiency 28nm Constant On-Time Controlled Step-Down Switching Regulator Directly Supplying to Wi-Fi Systems, W.-C. Chen, Y.-S. Huang, M.-W. Chien, Y.-W. Chou, H.-C. Chen, Y.-P. Su, K.-H. Chen, C.-L. Wey, Y.-H. Lin*, T.-Y. Tsai*, C.-C. Huang* and C.-C. Lee*, National Chiao Tung University, *Realtek Semiconductor Corp.

For high efficiency, the proposed constant on-time controlled switching regulator (SWR) directly supplies to Wi-Fi systems without cascading any low dropout regulators. On-time value adjusted by the proposed transient-enhanced technique greatly reduces transient voltage variations. Besides, an asynchronous auto-zero technique is used to minimize offset voltage effect to ±0.5% in steady state. Experimental results show voltage variation is smaller than ±3% and peak efficiency is 95% with a small silicon area of 0.0019mm^2, which is only one-twentieth of conventional design. The proposed well-regulated SWR can improve error vector magnitude (EVM) from -27.2dB to -33.6dB.

Session 21 - TAPA II
Capacitive Transducers

Friday, June 13
Chairpersons: S. Sridhara, Texas Instruments
N. Miura, Kobe University

21.1 - 1:30 p.m.
An ASIC for Readout of Post-Processed Thin-Film MEMS Resonators by Employing Capacitive Interfacing and Active Parasitic Cancellation, L. Huang, W. Rieutort-Louis, A. Gualdino*, L. Teagno*, Y. Hu, J. Mouro*, J. Sanz-Robinson, J.C. Sturm, S. Wagner, V. Chu*, J.P. Conde* and N. Verma, Princeton University, *Instituto Superior Técnico

Thin-film MEMS bridges as micro-resonators have proven attractive for various sensing applications (acceleration, mass, chemical, pressure, etc.) by using frequency shift as a basis for sensing. Low-temperature processing of amorphous-silicon (a-Si:H) enables low-cost fabrication of high-Q MEMS bridges having excellent compatibility with CMOS post processing. However, the a-Si:H bridges have weak motional conductances. Parasitic feed-through capacitances (several pF), both due to the device structure and routing, can easily drown out the resonant behavior. This paper proposes a non-contact MEMS interfacing and readout system in standard CMOS which enables robust integration while substantially rejecting the effects of parasitic feed-through capacitance. Measurements with multiple a-Si:H MEMS bridges having various parameters (frequencies from 1.3-2.89MHz, resonant conduction from 0.3-1.2MOhm), show that robust readout is achieved with an SNR greater than 20dB for detecting

the resonant peaks. A complete pressure-readout system is demonstrated using a MEMS bridge as the sensor with the CMOS IC.

21.2 - 1:55 p.m.
15.4b Incremental Sigma-Delta Capacitance-to-Digital Converter with Zoom-in 9b Asynchronous SAR, S. Oh, W. Jung, K. Yang, D. Blaauw and D. Sylvester, University of Michigan

An incremental zoom-in capacitance-to-digital converter (CDC) is proposed. A 9b op-amp free asynchronous SAR is followed by a 2nd order sigma-delta modulator with OSR of 32. A matrix based unit-cap structure is integrated for the 9b capacitive-DAC. It achieves 94.7 SNR and 33.7µW power consumption with 175fJ/conv-step at 1.4V supply.

21.3 - 2:20 p.m.
A Fully-Differential Capacitive Touch Controller with Input Common-Mode Feedback for Symmetric Display Noise Cancellation, K.-D. Kim, S. Kang, Y.-K. Choi, K.-H. Lee, C.-H. Lee, J.-c. Lee, M. Choi, K. Ko, J. Jung, N. Park, H. Park and G.-C. Hwang, Samsung Electronics

A fully-differential capacitive touch sensing method is proposed in which common-mode noise currents are symmetrically subtracted at the differential input of the first stage such that it doesn't contribute to dynamic range reduction in the later stages. And, for better sensitivity, the proposed method could accumulate signal charges in continuous time domain, and does not suffer from aliasing issues observed in many discrete-time charge integrating methods. Measurement results showed 42 dB SNR for a 1-mm diameter stylus on a 5-inch full-HD on-cell touch display panel.

21.4 - 2:45 p.m.
A Column-Row-Parallel ASIC Architecture for 3D Wearable / Portable Medical Ultrasonic Imaging, K. Chen, H.-S. Lee and C. Sodini, Massachusetts Institute of Technology

A Column-Row-Parallel ASIC architecture is proposed to enable 3D wearable / portable medical ultrasound. It offers linear-scaling interconnection, acquisition and programming time, while supporting rich functionality. High voltage MUX in Tx and specially sized source follower in Rx are used to implement parallelization for improved SNR. Fault-tolerant transceiver handles defective transducer elements to increase assembly yield and allow successful system demonstration.

Session 22 - TAPA I
Frequency Generation & Measurement Techniques

Friday, June 13
Chairpersons: T. Chan Carusone, University of Toronto
S.H. Cho, KAIST

22.1 - 3:25 p.m.
A 4.25GHz-4.75GHz Calibration-free Fractional-N Ring PLL Using Hybrid Phase/Current-mode Phase Interpolator With 13.2dB Phase Noise Improvement, R.K. Nandwana, T. Anand, S. Saxena, S.-J. Kim, M. Talegaonkar, A. Elkholy, W.-S. Choi, A. Elshazly* and P.K. Hanumolu, University of Illinois, Urbana-Champaign, *Intel Corporation

A calibration-free ring oscillator based fractional-N clock multiplier using hybrid phase/current-mode phase interpolator is presented. Fabricated in 65nm CMOS process, the prototype generates fractional frequencies from 4.25GHz-to-4.75GHz with in-band noise floor of -104dBc/Hz and 1.5ps integrated jitter. The clock multiplier achieves power efficiency of 2.4mW/GHz and FoM of -225.8dB.

22.2 - 3:50 p.m.
A 0.63ps, 12b, Synchronous Cyclic TDC using a Time Adder for On-chip Jitter Measurement of a SoC in 28nm CMOS Technology, S.-J. Kim, T. Kim and H. Park, Samsung Electronics

A time amplifier (TA)-based TDC used in the several TDC circuits is an attractive architecture that employs a multi-step data conversion scheme to increase the time resolution. However, architectures in tend to be power hungry or to require complex calibration circuitries owing to inaccurate gain of the TA and its asynchronous data conversion nature. In consequence, they pose considerable overhead from chip area or power consumption. In this paper, we present the first synchronous cyclic TDC which is implemented by a time adder based differential 2x TA with small size and low power consumption. The novel 2x time amplifier whose gain is insensitive to variations and noise is proposed by using time conservative nature of the proposed synchronous time adder. The implemented 12b TDC occupies 0.01mm^2, consumes 820μW and it achieves 0.63ps of resolution over 2.6ns of input range.

22.3 - 4:15 p.m.
An N-path Filter Enhanced Low Phase Noise Ring VCO, C. Zhai, J. Fredenburg, J. Bell and M. Flynn, University of Michigan

A novel self-filtering scheme breaks the typical tradeoff between noise and power, enabling a ring oscillator to approach the phase noise performance of an LC oscillator. The prototype N-path filter enhanced voltage-controlled ring oscillator (NPFRVCO) achieves a measured phase noise of -110dBc/Hz at a 1MHz offset frequency for an oscillation frequency of 1.0GHz. The self-clocked N-path filter reduces the phase noise by 10dB and 28dB for 1.0GHz and 300MHz oscillation frequencies, respectively. Implemented in 65nm CMOS, the NPFRVCO occupies a die area of 0.015 mm^2 and consumes 4.7mW from 1.2V power supply when operating at 1.0GHz. The NPFRVCO has a measured frequency tuning range from 300MHz to 1.6GHz and achieves a FoM of 163dB at 1MHz offset.

22.4 - 4:40 p.m.
92% Start-up Time Reduction by Variation-Tolerant Chirp Injection (CI) and Negative Resistance Booster (NRB) in 39MHz Crystal Oscillator, S. Iguchi, H. Fuketa, T. Sakurai and M. Takamiya, University of Tokyo

To reduce the start-up time of a crystal oscillator (XO), a chirp injection (CI) and a negative resistance booster (NRB) are proposed. By combining CI and NRB, the measured start-up time of a 39-MHz XO in 180-nm CMOS is reduced by 92% from 2.1ms to 158μs, which is the shortest time in the published XO's. The measured start-up time variations due to the ±20% supply voltage change or the temperature change are less than 13%.

22.5 - 5:05 p.m.
A 2.9mW, +/- 85ppm Accuracy Reference Clock Generator Based on RC Oscillator with On-chip Temperature Calibration, Y. Satoh, H. Kobayashi, T. Miyaba and S. Kousai, Toshiba Corporation, *Toshiba Microelectronics Corporation

A novel on-chip frequency calibration of temperature dependency is proposed for CMOS reference frequency generator. High-order temperature coefficients are rapidly extracted by employing a carefully designed on-chip heater, so that the frequency deviation due to the temperature variation is accurately estimated, and compensated in digitally by means of all-digital PLL (ADPLL). The proposed technique was implemented in a 0.18um CMOS and achieved ±85ppm accuracy at 24MHz, consuming a power of 2.9mW.

Session 23 - TAPA II
High-Speed SAR ADCs

Friday, June 13
Chairpersons: E. Fogleman, MaxLinear
Y.-S. Shu, MediaTek, Inc.

23.1 - 3:25 p.m.
A 70 dB SNDR 200 MS/s 2.3 mW Dynamic Pipelined SAR ADC in 28nm Digital CMOS, B. Verbruggen, K. Deguchi*, B. Malki and J. Craninckx, imec, *Renesas Electronics

We present a 200 MS/s 2x interleaved 14 bit pipelined SAR ADC in 28nm digital CMOS. The ADC uses a new residue amplifier for low noise at low power, and incorporates interleaved channel time-constant calibration. The ADC achieves a peak SNDR of 70.7 dB at 200 MS/s while consuming 2.3 mW from an 0.9 V supply.

23.2 - 3:50 p.m.
A 12-bit 210-MS/s 5.3-mW Pipelined-SAR ADC with a Passive Residue Transfer Technique, C.-Y. Lin and T.-C. Lee, National Taiwan University

A 210 MS/s dual-channel 12-bit analog-to-digital converter (ADC) employing a pipelined successive approximation (SAR) architecture is presented. The ADC is partitioned into 3 stages with passive residue transferring between the 1^{st} and the 2^{nd} stages and active residue amplification between the 2^{nd} and the 3^{rd} stages. The ADC consumes 5.3 mW from a 1-V supply and achieves an SNDR of 63.48 dB at a 5-MHz input and 60.1 dB near Nyquist-rate.

23.3 - 4:15 p.m.
An 11.5-ENOB 100-MS/s 8mW Dual-Reference SAR ADC in 28nm CMOS, M. Inerfield, A. Kamath, F. Su, J. Hu, X. Yu, V. Fong, O. Alnaggar, F. Lin and T. Kwan, Broadcom Corporation

Recent publications have demonstrated ENOB > 11 bit, sampling frequencies > 50MHz, with power < 50mW, making the SAR ADC architecture an attractive alternative to the traditional pipeline. This paper presents a production quality 11.5 ENOB, 89dB SFDR, 100MS/s SAR ADC which consumes 8mW power and occupies $0.1mm^2$ area in 28nm CMOS, including the voltage reference and digital calibration circuitry. It uses a unique dual-reference, dual unit-cap architecture with a regulated DAC switch, providing a 2Vppd input swing, while utilizing low-voltage transistor implementation of the core ADC.

23.4 - 4:40 p.m.
A 12b 160MS/s Synchronous Two-Step SAR ADC Achieving 20.7fJ/step FoM with Opportunistic Digital Background Calibration, Y. Zhou, B. Xu and Y. Chiu, University of Texas at Dallas

A 12b two-step pipelined SAR ADC reports a 66.7dB SNDR and an 86.9dB SFDR for a 5MHz sinusoidal input at 160MS/s. A digital background calibration based on opportunistic PN injection treats both DAC mismatch and residue-amplifier gain errors. The calibration enables a significant downsizing of the ADC input capacitance to yield a wideband, highly linear input network and an over-80dB SFDR while digitizing inputs from DC to 300MHz at full speed. The conversion FoM of this ADC is 20.7fJ/step at Nyquist. The prototype occupies an active area of 0.042mm^2 in a 40nm CMOS low-leakage digital process.