2014 Symposium on VLSI Technology Short Course
TAPA I and II

High Performance Mobile SoCs Enabled by 10nm SoC Technology

Monday, June 9

Co-Chairs: G. Yeap, Qualcomm
K. Uchida, Keio University

8:00 a.m. - Introduction & Overview of Mobile SoC Technology Environment, G. Yeap, Qualcomm

8:15 a.m. – Key Semiconductor Products, Applications and Device Drivers
- CPU applications: Key tech/design drivers, R. Aitken, ARM
- GPU applications: Key tech/design drivers, L. Bair, AMD
- DSP/VPE applications: Key tech/design drivers, M. Saint-Laurent, Qualcomm
- FPGA applications: Key tech/design drivers, X. Wu, Xilinx

10:00 a.m. – 10:20 a.m. – Break

10:20 a.m. – System on Chip – Applications and Key Aspects
- System on Chip – Applications and Key Aspects for RF/MS Transceiver and Connectivity, M. Zargari, Qualcomm
- System on Chip – Applications and Key Aspects for RF-Frontend, G. Yeap, Qualcomm

11:15 a.m. – FEOL Scaling & Integration, 3rd gen FINFET Devices & Architectures, A. Wei, GLOBALFOUNDRIES

12:15 p.m. – 1:30 p.m. – Lunch

1:30 p.m. – BEOL Interconnect Scaling, Processes and Integration, T. Spooner, IBM

2:15 p.m. – Technology/Design Co-optimization, C. Young, TSMC

3:00 p.m. – 3:20 p.m. - Break

3:20 p.m. – Embedded SoC Memory: eSRAM, eNVM and eDRAM, G. Kim, Samsung

4:00 p.m. – Variability and DFM PDF, A. Strojwas, PDF Solutions

4:45 p.m. – 2.5D or 3D Packaging for Mobile SIP, G. Van der Plaas, IMEC

Session 1 – TAPA I & II

Plenary Session

Tuesday, June 10, 8:05 a.m.

Chairs: R. Jammy, Intermolecular
S. Inaba, Toshiba Electronics Korea Corporation

8:05 a.m. **Welcome and Opening Remarks**
K. Schruefer, Intel Mobile Communications
T. Hiramoto, The University of Tokyo

1.1 – 8:35 a.m.
Device and Technology Implications of the Internet of Things (Invited), R. Aitken, Fellow, ARM

We live in an interconnected world. Computing power once reserved for server rooms now resides in our pockets. Tablets now outsell PCs. As marked as these changes have been, we are now entering a new era of vastly greater connectivity, where people interact with the world around them in entirely new ways. The Internet of Things is in its infancy, so predictions of precisely what it will become are dangerous, but several things are clear. First, the leaf nodes of the network will share some device and technology properties in terms of cost and computing capability, but also analog and wireless functionality. These nodes will interact with people and with the cloud. The "little data" of these interactions needs to integrate seamlessly with the "big data" of the world around them. The trust, security and service components of these interactions lead to further device and technology requirements. This talk looks at the trends and discusses some likely paths forward.

1.2 – 9:20 a.m.
Customer Value Creation in the Information Explosion Era (Invited), K. Shimada, Senior Vice President, Sony Corporation

This talk focuses on the impact of the information explosion and semiconductor technology on consumer electronics and information industries. The progress of semiconductor technology under Moore's Law and information transmission technology has eased various limitations for customers, such as place, time and preparations. The television, the video recorder, and on-demand broadcasting are technologies that have helped to overcome these limitations and realize new customer values.

The amount of communication is still rapidly growing due to the explosion of data contents (such as 4K) and data creators (such as CGM and IoT). This trend will create another industry and new customer values.

Session 2 - TAPA I & II

Highlights

Tuesday, June 10

Chairpersons: M. Khare, IBM
S. Yamakawa, Sony Corporation

2.1 - 10:20 a.m.

A Novel Curved CMOS Image Sensor Integrated with Imaging System, K. Itonaga, T. Arimura*, K. Matsumoto*, G. Kondo**, K. Terahata*, S. Makimoto*, M. Baba*, Y .Honda*, S. Bori*, T. Kai*, K. Kasahara*, M. Nagano**, M. Kimura**, Y. Kinoshita**, E. Kishida**, T. Baba, S. Baba, Y. Nomura, N. Tanabe, N. Kimizuka, Y. Matoba, T. Takachi, E. Takagi**, T. Haruta, N. Ikebe**, K. Matsuda*, T. Niimi*, T. Ezaki and T. Hirayama, Sony R&D Platform, *Sony Semiconductor Oita, **Sony Semiconductor Kumamoto

We realized an ultimately advanced imaging system that comprises a curved, back-illuminated CMOS image sensor (BIS) and integrated lens which doubles the sensitivity at the edge of the image circle and increases the sensitivity at the center of the image circle by a factor of 1.4 with one-fifth lower dark current than that of a planar BIS. Because the lens field curvature aberration was overcome in principle by the curved sensor itself, the curved BIS enables higher system sensitivity through design of a brighter lens with a smaller F number than is possible with a planar BIS. At the same time, we controlled the tensile stress of the BIS chip to produce a curved shape that widens the energy band-gap to obtain a lower dark current. The curved CIS can be applied to an ultimately advanced imaging system that is validated by the evolution of the animal eye in Nature.

2.2 - 10:45 a.m.

A 10nm Platform Technology for Low Power and High Performance Application Featuring FINFET Devices with Multi Workfunction Gate Stack on Bulk and SOI, K.-I. Seo*, B. Haran, D. Gupta, D. Guo, T. Standaert, R. Xie***, H. Shang, E. Alptekin, D.-I. Bae*, G. Bae*, C. Boye, H. Cai***, D. Chanemougame**, R. Chao, J. Cho***, B. Hamieh**, J.G. Hong*, T. Hook, L. Jang***, J. Jung*, R. Jung, D. Lee*, B. Lherron**, R. Kambhampati***, B. Kim*, H. Kim***, K. Kim*, T.S. Kim*, S.-B. Ko, F.L. Lie, D. Liu, H. Mallela, E. Mclellan, S. Mehta, P. Montanini**, M. Mottura**, J. Nam, S. Nam***, F. Nelson, I. Ok, C. Park***, Y. Park*, A. Paul***, C. Prindle***, R. Ramachandran, M. Sankarapandian, V. Sardesai, A. Scholze, S.-C. Seo, J. Shearer, R. Southwick, S. Stieg, J. Strane, X. Sun, M.G. Sung***, S. Surisetty, G. Tsutsui, N. Tripathi***, R. Vega, C. Waskiewicz, M. Weybright, C.-C. Yeh, H. Bu, S. Burns, D. Canaperi, M. Celik**, M. Colburn, H. Jagannathan, S. Kanakasabaphthy, W. Kleemeier**, L. Liebman, D. Mcherron, P. Oldiges, V. Paruchuri, T. Spooner, J. Stathis, R. Divakaruni, T. Gow, J. Iacoponi***, J. Jenq^, R. Sampson**, M. Khare, IBM Microelectronics, *Samsung Electronics, **STMicroelectronics, ***GLOBALFOUNDRIES, ^UMC

A 10nm logic platform technology is presented for low power and high performance application with the tightest contacted poly pitch (CPP) of 64nm and metallization pitch of 48nm ever reported in the FinFET technology on both bulk and SOI substrate. A 0.053 μm^2 SRAM bit-cell is reported with a corresponding Static Noise Margin (SNM) of 140mV at 0.75V. Intensive multi-patterning technology and various self-aligned processes have been developed with 193i lithography to overcome optical patterning limit. Multi-workfunction (WF) gate stack has been enabled to provide Vt tunability without the variability degradation induced by channel dopants.

2.3 - 11:10 a.m.

14nm FDSOI Technology for High Speed and Energy Efficient Applications, O. Weber*, E. Josse, F. Andrieu*, A. Cros, E. Richard, P. Perreau*, E. Baylac, N. Degros**, C. Gallon, E. Perrin, S. Chhun, E. Petitprez, S. Delmedico, J. Simon**, G. Druais, S. Lasserre**, J. Mazurier*, N. Guillot, E. Bernard, R. Bianchini, L. Parmigiani, X. Gerard, C. Pribat, O. Gourhant, F. Abbate, C. Gaumer, V. Beugin*, P. Gouraud, P. Maury, S. Lagrasta, D. Barge, N. Loubet, R. Beneyton, D. Benoit, S. Zoll, J.-D. Chapon, L. Babaud, M. Bidaud, M. Gregoire, C. Monget, B. Le-Gratiet, P. Brun*, M. Mellier, A. Pofelski, L.R. Clement, R. Bingert, S. Puget, J-F. Kruck, D. Hoguet, P. Scheer, T. Poiroux*, J.-P. Manceau**, M. Rafik, D. Rideau, M.-A. Jaud*, J. Lacord, F. Monsieur, L. Grenouillet*, M. Vinet*, Q. Liu, B. Doris**, M. Celik, S. Fetterolf**, O. Faynot* and M. Haond, STMicroelectronics, *CEA-LETI, **IBM

This paper presents a 14nm technology designed for high speed and energy efficient applications using strain-engineered FDSOI transistors. Compared to the 28nm FDSOI technology, this 14nm FDSOI technology provides 0.55x area scaling and delivers a 30% speed boost at the same power, or a 55% power reduction at the same speed, due to an increase in drive current and low gate-to-drain capacitance. Using forward back bias (FBB) we experimentally demonstrate that the power efficiency of this technology provides an additional 40% dynamic power reduction for ring oscillators working at the same speed. Finally, a full single-port SRAM offering is reported, including an 0.081µm^2 high-density bitcell and two 0.090µm^2 bitcell flavors used to address high performance and low leakage-low Vmin requirements.

2.4 - 11:35 a.m.

Strained $Si_{1-x}Ge_x$-on-Insulator PMOS FinFETs with Excellent Sub-Threshold Leakage, Extremely-High Short-Channel Performance and Source Injection Velocity for 10nm Node and Beyond, P. Hashemi, K. Balakrishnan, A. Majumdar, A. Khakifirooz, W. Kim, A. Baraskar*, L. Yang*, K. Chan, S. Engelmann, J. Ott, D. Antoniadis**, E. Leobandung and D.-G. Park, IBM Research, T.J. Watson Research Center, *GLOBALFOUNDRIES, **Massachusetts Institute of Technology

We demonstrate high performance (HP) s-SiGe pMOS finFETs with I_{on}/I_{eff} of ~1.05/0.52mA/µm and ~1.3/0.71mA/µm at I_{off}=100nA/µm at V_{DD}=0.8 and 1V, extremely high intrinsic performance and source injection velocity. Compared to earlier work, an optimized process flow and a novel interface passivation scheme, result in ~30% mobility enhancement and dramatic sub-threshold-swing reduction to 65mV/dec. We also demonstrate the most aggressively scaled s-SiGe finFET reported to date, with W_{FIN}~8nm and L_G~15nm, while maintaining high current drive and low leakage. With their very low GIDL-limited $I_{D,\ min}$ and more manufacturing-friendly process compared to high-Ge content SiGe devices, as well as impressive Ion~0.42mA/µm at I_{off} =100nA/µm and $g_{m,\ int}$ as high as 2.4mS/µm at V_{DD}=0.5V, s-SiGe finFETs are strong candidates for future HP and low-power applications.

Session 3 - TAPA I

3D Memory & Emerging Devices I

Tuesday, June 10

Chairpersons: H. Jaouen, STMicroelectronics
T. Yamashita, Renesas Electronic Corporation

3.1 - 1:30 p.m.

Study of the Impact of Charge-Neutrality Level (CNL) of Grain Boundary Interface Trap on Device Variability and P/E Cycling Endurance of 3D NAND Flash Memory, W.-C. Chen, H.-T. Lue, Y.-H. Hsiao, X.-W. Lin*, J. Huang*, Y.-H. Shih and C.-Y. Lu, Macronix International Co., Ltd., *Synopsys Inc.

Poly-Si thin-film transistor (TFT) is the key building element for high-density 3D NAND Flash memory. Random grain boundary (GB) location and interface traps (Dit) density have been shown as the major root cause of variability [1]. However, with CNL pinned at midgap our previous model cannot adequately address experimental results – especially the cause of very low Vt TFT devices. In this work we point out that to accurately model the TFT device, CNL should not be restricted at the mid-gap only, as in the conventional assumption for Si/SiO_2 interface trap, but should be randomly distributed inside the bandgap for GB trap. This makes donor-type Dit active besides the acceptor-type Dit. Simulation including the random CNL can well explain the very low-Vt devices and gives better TFT variability model. Furthermore, GB trap CNL plays an important role in governing the device subthreshold behavior during PE cycling for 3D NAND Flash.

3.2 - 1:55 p.m.

Laser Thermal Anneal of Polysilicon Channel to Boost 3D Memory Performance, J. Lisoni, A. Arreghini, G. Congedo, M. Toledano-Luque, I. Toqué-Tresonne*, K. Huet*, E. Capogreco, L. Liu**, C.-L. Tan, R. Degraeve, G. Van den bosch and J. Van Houdt, imec, *Excico, **Now on leave from Tsinghua University

We demonstrate that channel current boosting and improved memory performance can be achieved by engineering the polySi channel grain microstructure of 3D vertical NAND nonvolatile memory devices. Different polySi channels are screened, obtained either by deposition or post-deposition anneals such as conventional furnace anneal and laser thermal techniques. Link between material characteristics and device performance is presented. Laser anneal provides the best results leading to 10 times higher ID, 3 times steeper subthreshold slope, tighter ID and STS distributions, better channel-oxide interface, less defective grain boundaries and larger memory window. These improvements are not only a consequence of optimal grain size distribution, but also related to their defectivity as clearly pointed out by the transconductance and its temperature activation, and the amount of conduction percolating paths measured. This learning is crucial for the successful fabrication of advanced vertical devices stacks.

3.3 - 2:20 p.m.

Ultra Thinning Down to 4-µm using 300-mm Wafer Proven by 40-nm Node 2Gb DRAM for 3D Multi-Stack WOW Applications, Y.S. Kim, S. Kodama, Y. Mizushima, N. Maeda, H. Kitada, K. Fujimoto, T. Nakamura**, D. Suzuki^, A. Kawai*, K. Arai* and T. Ohba, Tokyo Institute of Technology, *DISCO CORPORATION **Fujitsu Laboratories, ^PEZY Computing Ltd.

An ultra-thinning down to 4-µm using 300-mm wafer proven by 40-nm Node 2Gb DRAM has been developed for the first time. Three different types of thinning process including coarse grinding, fine grinding, and stress relief were optimized and an atomic level vacancy less than 10-nm in depth at backside of wafer was formed successively. Thickness uniformity even after thinning down to 4-µm was approximately 1-µm within 300-mm wafer. No degradation in terms of retention characteristics and distribution employing 2Gb DRAM wafer was found after ultra-thinning. This suggests that no damage occurred due to thinning processes including wafer bonding and debonding steps. These results indicate good feasibility for multi-stack Wafer-on-Wafer (WOW) processes with the lowest aspect ratio of TSVs and parasitic capacitance, and enable multi-stacking for Tera-scale high density memory.

3.4 - 2:45 p.m.

Effect of Traps on Transient Bit-line Current Behavior in Word-line Stacked NAND Flash Memory with Poly-Si Body, H.-J. Kang, M.-K. Jeong, S.-M. Joe, J.-H. Seo*, S.-K. Park*, S.H. Jin, B.-G. Park and J.-H. Lee, Seoul National University, *SK hynix Inc.

We characterized the behavior of transient bit-line current during reading after giving a pre-bias to two different cells in 3-D stacked NAND flash memory having poly-Si body. Depending on the dominance of charge trapping in blocking dielectric or the interface between the tunneling oxide and the poly-Si body, opposite behavior was observed. To identify the cause, we systematically analyzed the capture and emission of charges in two trap sites by investigating transient bit-line current behaviors during reading with various pre-biases and fast & pulsed I-Vs. The carrier life time and trap density associated with grain size were extracted to substantiate different trap density with the vertical position of cells.

Session 4 - TAPA II

Advanced CMOS Technology I - *III-V Channels*

Tuesday, June 10

Chairpersons: W. Maszara, GLOBALFOUNDRIES
S. Takagi, The University of Tokyo

4.1 - 1:30 p.m.

An InGaAs/InP Quantum Well FinFet Using the Replacement Fin Process Integrated in an RMG Flow on 300mm Si Substrates, N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar*, D. Tsvetanova, F. Sebaai, D. van Dorp, A. Milenin, D. Lin, L. Nyns, J. Mitard, A. Pourghaderi,B. Douhard, O. Richard, H. Bender, G. Boccardi, M. Caymax, M. Heyns, W. Vandervorst, K. Barla, N. Collaert and A. Thean, IMEC, *BASF

InGaAs FinFETs fabricated by an unique Si fin replacement process have been demonstrated on 300mm Si substrates. The devices are integrated by process modules developed for a Si-IIIV hybrid 300mm R&D pilot line, compatible for future CMOS high-volume manufacturing. First devices with a SS of 178 mV/dec and extrinsic gm of 558 µS/µm are achieved for an EOT of 1.9nm, L_g of 50nm and fin width of 55nm. A trade-off between off state leakage and mobility for different p-type doping levels of the InP and InGaAs layers is found and the RMG high-κ last processing is demonstrated to offer significant performance improvements over that of high-κ first.

4.2 - 1:55 p.m.

III-V Single Structure CMOS by Using Ultrathin Body InAs/GaSb-OI Channels on Si, M. Yokoyama, H. Yokoyama*, M. Takenaka and S. Takagi, The University of Tokyo, *NTT Corporation

We propose and demonstrate the operation of single structure III-V CMOS transistors by using metal S/D ultrathin body (UTB) InAs/GaSb-on-insulator (-OI) channels on Si wafers. It is found that the CMOS operation of the InAs/GaSb-OI channel is realized by using ultrathin InAs layers, because of the quantum confinement of the InAs channel and the tight gate control. The quantum well (QW) InAs/GaSb-OI on Si structures are fabricated by using direct wafer bonding (DWB). We experimentally demonstrate both n- and p-MOSFET operation for an identical InAs/GaSb-OI transistor by choosing the appropriate thickness of InAs and GaSb channel layers. The channel mobilities of both InAs n- and GaSb p-MOSFET are found to exceed those of Si MOSFETs.

4.3 - 2:20 p.m.

Sub-100 nm Regrown S/D Gate-Last$_{In\ 0.7}$Ga$_{0.3}$As QW MOSFETs with $\mu_{n,eff}$ > 5,500 cm^2/V-s, C. Shin, W. Park, S.H. Shin*, Y. Cho*, D. Ko*, T.-W. Kim**, D. Koh**, H. Kwon**, R. Hill**, P. Kirsch**, W. Maszara***, and D.-H. Kim**, KANC, *Yonsei University, **SEMATECH, ***GLOBALFOUNDRIES

This paper reports on gate-last (GL) $In_{0.7}Ga_{0.3}As$ QW MOSFETs with regrown S/D by MOCVD. Long-channel devices exhibit $\mu_{n,eff}$ = 5,500 cm^2/V-s at room temperature. Short-channel device with L_g = 40 nm also exhibit excellent electrostatic integrity of SS = 105 mV/dec., and DIBL = 150 mV/V, together with g_{m_max} = 2 mS/μm at VDS = 0.5 V.

4.4 - 2:45 p.m.

High Performance InGaAs-On-Insulator MOSFETs on Si by Novel Direct Wafer Bonding Technology Applicable to Large Wafer Size Si, S. Kim, Y. Ikku, M. Yokoyama, R. Nakane, J. Li*, Y.-C. Kao*, M. Takenaka and S. Takagi, The University of Tokyo, *IntelliEPI, Inc.

In this paper, we present first demonstration of InGaAs-on-insulator (-OI) MOSFETs with wafer size scalability up to Si wafer size of 300 mm and larger by direct wafer bonding (DWB) process using InGaAs channels grown on Si donor substrates with III-V buffer layers instead of InP donor substrates. It is found that this DWB process can provide the high quality InGaAs thin films on Si. The fabricated InGaAs-OI MOSFETs have exhibited the high electron mobility of 1700 cm^2/Vs and large mobility enhancement factor of 3 × against Si MOSFETs.

Session 5 - TAPA I

Focus Session - Embedded Non-Volatile Memory Technologies

Tuesday, June 10

Chairpersons: J. Cheek, Freescale
S. Chung, National Chiao Tung University

5.1 - 3:25 p.m.

A High-Density Logic CMOS Process Compatible Non-Volatile Memory for Sub-28nm Technologies (Invited), R. S-J Shen, M-Y Wu, H-M Chen and C. C-H Lu, eMemory Technology Inc.

Various product applications bring up with increasing demands of logic NVM IP in advanced technology nodes. Encryption, security, functionality, and identification setting become indispensable in communication and high-end consumer electronics. A non-volatile memory cell, using anti-fuse programming mechanism to achieve high density and excellent data storage lifetime, is proposed. The unique cell design and operation scheme realize low programming-inhibit leakage current, fast program speed, and robust data retention. The memory macro is successfully demonstrated for one-time and multi-time programming applications with its full compatibility to sub-28nm and FinFET processes.

5.2 - 3:50 p.m.

Embedded STT-MRAM for Energy-efficient and Cost-effective Mobile Systems (Invited), S.H. Kang, Qualcomm Technologies Incorporated

STT-MRAM is a logic-friendly nonvolatile memory that can realize a combination of high speed, low energy, and high endurance. Embedded STT-MRAM is positioned attractively not only for emerging low standby-power connectivity systems such as wearables, IOT (Internet-of-Things), and secure elements,

but also for high-performance mobile SOC as an embedded nonvolatile working memory. With recent breakthroughs in CoFeB-based perpendicular magnetic tunnel junctions (MTJ), embedded STT-MRAM has become more energy-efficient and cost-effective in conjunction with robust data retention, scalable for advanced logic nodes.

5.3 - 4:15 p.m.

Flash-Based Nonvolatile Programmable Switch for Low-Power and High-Speed FPGA by Adjacent Integration of MONOS/Logic and Novel Programming Scheme, K. Zaitsu, K. Tatsumura, M. Matsumoto, M. Oda, S. Fujita and S. Yasuda, Toshiba Corporation

Novel nonvolatile programmable switch for low-power and high-speed FPGA where MONOS flash is adjacently integrated to CMOS logic is demonstrated for the first time. FPGA has been in high demand due to increase in development cost of customized LSI, and particularly flash-based FPGA offers low-power operation. However, conventional flash-based FPGA needs large chip area, and small on-current in switching transistor increases delay. In this work, we have developed integration process of MONOS flash so that the MONOS transistors and low-voltage switching transistors are fabricated close to each other without deteriorating each performance. Memory programming scheme is also optimized to realize selective writing with no damage in the switching transistors. The MONOS-based configuration memory has a half area of conventional one. Since the MONOS flash can be placed in each block in FPGA, operation power can be reduced by efficient power gating techniques.

5.4 - 4:40 p.m.

Anti-Fuse Memory Array Embedded in 14nm FinFET CMOS with Novel Selector-Less Bit-Cell Featuring Self-Rectifying Characteristics, Y. Liu, M.-H. Chi, A. Mittal, G. Aluri, S. Uppal, P. Paliwoda, E. Banghart, K. Korablev, B. Liu, M.H. Nam, M. Eller and S. Samavedam, GLOBALFOUNDRIES

A novel one-capacitor-per-cell anti-fuse memory array compatible with 14nm FinFET CMOS technology is presented for the first time. The unique structural properties of FinFET facilitate a rectifying I-V characteristic of the programmed bit. At forward word-line bias region, the enhanced electrical field at curved Fin tip allows controllable break-down at the interfacial layer (IL) only of the IL/HiK gate dielectric stack, leading to boosted forward tunneling current post programming. At reverse word-line bias region, the fully depleted silicon Fin caused by negatively-biased word-line wrapping around clamps the read current. This rectifying I-V characteristic prevents the sneak current in the cross-point array, therefore no need for select transistor in each cell. Thus enables simplified memory array design and the smallest reported bit-cell with area measuring 0.036 μm^2. The life time of the programmed bits under stress and the array size allowed are evaluated as well.

5.5 - 5:05 p.m.

Demonstration of Fully Functional 8Mb Perpendicular STT-MRAM Chips with Sub-5ns Writing for Non-Volatile Embedded Memories, G. Jan, L. Thomas, S. Le, Y.-J. Lee, H. Liu, J. Zhu, R.-Y. Tong, K. Pi, Y.-J. Wang, D. Shen, R. He, J. Haq, J. Teng, V. Lam, K. Huang, T. Zhong, T. Torng and P.-K. Wang, TDK-Headway Technologies, Inc.

We present major breakthroughs in MTJ design for STT-MRAM applications allowing reliable write for pulse lengths down to 1.5ns, data retention up to 125°C for 10 years and full compatibility with BEOL process up to 400°C for 1 hour. We have successfully integrated the novel structure onto an 8Mbit test chip. We demonstrate writing of every single cell in the array using sub-5ns pulses over a wide temperature range without using any error correction. We also show that sensing times of 4ns are

sufficient to read every data cell. The inherent scalability of the design makes it a prime candidate for universal embedded non-volatile memories down to the 28nm node and beyond.

Session 6 - TAPA II
Process Technology I

Tuesday, June 10
Chairpersons: C.-P. Chang, Applied Materials, Inc.
K. Miyashita, Toshiba Corporation

6.1 - 3:25 p.m.
Simple Gate Metal Anneal (SIGMA) Stack for FinFET Replacement Metal Gate Toward 14nm and Beyond, T. Ando, B. Kannan*, U. Kwon*, W.L. Lai*, B.P. Linder, E.A. Cartier, R. Haight, M. Copel, J. Bruley, S.A. Krishnan and V. Narayanan, IBM T. J. Watson Research Center, *IBM Semiconductor Research and Development Center

We demonstrate a Simple Gate Metal Anneal (SIGMA) stack for FinFET Replacement Metal Gate technology with a 14nm design rule. The SIGMA stack uses only thin TiN layers as workfunction (WF)-setting metals for CMOS integration. The SIGMA stack provides 100x PBTI lifetime improvement via band alignment engineering. Moreover, the SIGMA stack enables 9nm more gate length (L_g) scaling compared to the conventional stack with matched gate resistance due to absence of high resistivity WF-setting metal and more room for W in the gate trench. This gate stack solution opens up pathways for aggressive L_g scaling toward the 14nm node and beyond.

6.2 - 3:55 p.m.
Highly Scalable Bulk FinFET Devices with Multi-V_T Options by Conductive Metal Gate Stack Tuning for the 10-nm Node and Beyond, L.-Å. Ragnarsson, S.-A. Chew, H. Dekkers, M. Toledano Luque, B. Parvais, A. De Keersgiester, K. Devriendt, A. Van Ammel, T. Schram, N. Yoshida*, A. Phatak*, K. Han*, B. Colombeau*, A. Brand*, N. Horiguchi and A. Thean, imec, *Applied Materials

A scalable multi-V_T enabled CMOS RMG integration process with highly conformal ALD TiN/TiAl/TiN is described. The multi-V_T is implemented by metal gate tuning using two different options. The first relies on bottom-barrier thickness control, the second on implantation of nitrogen into a work function metal. A shift in the effective work function (eWF) of ~400 *m*V is realized by adjusting the TiN bottom barrier thickness underneath TiAl, while over 200 *m*V shifts are achieved by means of implantation of nitrogen into ALD TiN/TiAl/ TiN. The gate-stack T_{inv}, J_G, D_{It} and reliability as well as the device performance are shown to be unaffected by the multi V_T process.

6.3 - 4:15 p.m.
Performance and Reliability of High-Mobility $Si_{0.55}Ge_{0.45}$ p-Channel FinFETs Based on Epitaxial Cladding of Si Fins, H. Mertens, R. Ritzenthaler, A. Hikavyy, J. Franco, J.W. Lee, D. Brunco*, G. Eneman, L. Witters, J. Mitard, S. Kubicek, K. Devriendt, D. Tsvetanova, A. Milenin, C. Vrancken, J. Geypen, G. Groeseneken, W. Vandervorst, K. Barla, N. Collaert, N. Horiguchi and A. Thean, imec, *GLOBALFOUNDRIES

We present a comprehensive study of $Si_{0.55}Ge_{0.45}$-cladded p-channel FinFETs, including a comparison with planar SiGe quantum-well devices. The SiGe-cladded FinFETs exhibit ~2x higher hole mobility, ~2x better I_{ON}/I_{OFF}, and improved DIBL compared to Si control devices. Superior NBTI reliability over equivalent Si FinFETs is demonstrated for cladding thicknesses down to 3 nm. The dependencies of drive

current and hole mobility on both SiGe thickness and device width are examined in detail. This analysis shows that SiGe thickness conformality and epitaxial facet control are crucial for the optimization of SiGe-cladded FinFETs.

6.4 - 4:40 p.m.
III-V CMOS Devices and Circuits with High-Quality Atomic-Layer-Epitaxial La_2O_3/GaAs Interface, L. Dong, X. Wang*, J. Zhang, X. Li, X. Lou*, N. Conrad, H. Wu, R. Gordon* and P. Ye, Purdue University, *Harvard University

GaAs, as the most studied III-V semiconductor, has been long-time considered to replace Si n logic applications. In order to achieve a thermodynamically stable dielectric on GaAs with a high quality interface, tremendous efforts have been made by different passivation techniques since its first publication in 1965. Recently, we reported high-performance GaAs nMOSFETs with single crystalline La-based oxide dielectrics, showing breakthrough in the drive current. In this work, we demonstrate, for the first time, high-performance GaAs-based CMOS devices and circuits (inverters, NAND and NOR logic gates, and five-stage ring oscillators). These devices were enabled by the high-quality interface of single-crystalline La_2O_3 grown on GaAs(111)A by atomic layer epitaxy (ALE).

6.5 - 5:05 p.m.
A Novel Metallic Complex Reaction Etching for Transition Metal and Magnetic Material by Low-Temperature and Damage-Free Neutral Beam Process for Non-Volatile MRAM Device Applications, X. Gu, Y. Kikuchi, T. Nozawa and S. Samukawa*, Tokyo Electron Limited, *Tohoku University

A new oxidation reaction at ultralow temperature (-30ºC) by bombardment of O_2 neutral beam can be enhanced at the extremely low activation energy, which can efficiently form a thin oxide film of all transition metal, such as platinum and ruthenium. Meanwhile, a novel neutral beam enhanced chemical etching for transition metals and magnetic materials was proposed without chemical and physical damages at ultralow temperature through Metallic Complex Reaction process. Highly anisotropic etching profile without both any sidewall re-deposition and damages on magnetic properties could be achieved just with a pure chemical reaction between ethanol and metallic oxide with low kinetic energy by neutral beam for the first time. This new etching technology has been considered as a breakthrough technology to develop next generation MRAM devices.

6.6 – 5:30 p.m.
Record Ion (0.50 mA/µm at VDD = 0.5 V and I_{off} = 100 nA/µm) 25 nm-Gate-Length ZrO2/InAs/InAlAs MOSFETs (Late News), S. Lee, V. Chobpattana, C.-Y. Huang, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, M. J. W. Rodwell, University of California, Santa Barbara

We report MOSFETs with 25-nm gate length (Lg), extremely thin 2.5 nm InAs channels and 0.7/3.0 nm (physical) Al2OxNy/ZrO2 gate dielectrics, and 12 nm In0.53Ga0.47As vertical spacers in the raised epitaxial source/drain. The FETs establish key new DC performance records, at VLSI-relevant gate lengths (25nm), including 0.50 mA/um on-current (at 100 nA/um Ioff and 0.5 V VDD) and 77 mV/dec. subthreshold swing (SS) at VDS=0.5 V. At 1 um Lg and VDS=0.1 V, the minimum subthreshold swing is 61 mV/dec., a record low for InAs/InGaAs, indicating high interface quality.

Technology / Circuits Joint Rump Session
Tuesday, June 10, 8:00 p.m. – 10:00 p.m.

JOINT TECHNOLOGY/CIRCUITS RUMP SESSION
Tuesday, June 10
8:00 p.m. – 10:00 p.m.

RJ-1: Who gives up on scaling first: device and process technology engineers, circuit designers, or company executives? Which scaling ends first – memory, or logic?

Technology Organizers:
C. Mazure, SOITEC
Y.-C. Yeo, National University of Singapore

Circuits Organizers:
E. Alon, University of California, Berkeley
M. Yamaoka, Hitachi

Moderators: E. Alon, University of California, Berkeley
Y.-C. Yeo, National University of Singapore

While many past predictions of the end of CMOS scaling were proven to be incorrect, there is now no question that the nature of scaling today has shifted dramatically. In particular, energy, performance, and perhaps even cost no longer clearly/directly benefit from simple dimensional scaling. This panel will therefore address the now extremely timely question of who will finally drive the decision to stop CMOS scaling, and why will they do so. Will CMOS continue to scale as far as device and process engineers are able to develop cost-effective manufacturing infrastructure, or will circuit designers no being able to extract benefits from scaling due to power/thermal issues first? Or will executives decide that the returns from scaling in terms of cost – due for example to design costs or limited markets supporting the volume to amortize that cost – are no longer worth it? The panel will discuss these question in the context of both memory and logic technologies, and will further consider which of the two will end first.

Panelists:
M. Bohr, Intel
M. Cao, TSMC
J. Chen, Nvidia
S-H Lee, Hynix
T-J King Liu, University of California, Berkeley
K. Nii, Renesas
R. Shrivastava, Sandisk
T. Skotnicki, STMicroelectronics

R-2: 450 mm, EUV, III-V, 3D; All in 7nm? Are you serious?!

Organizers: C. Mazure, SOITEC
Y.-C. Yeo, National University of Singapore

Moderator: A. Strojwas, PDF

The IC industry in its pursuit of technology scaling has an excellent track record of innovations and breakthroughs. In particular, the industrial ecosystem supporting IC manufacturing has had an enabling role in the making of ever denser, faster and cheaper IC products. The materials, substrate, equipment industries have introduced very successfully innovations at an incredible pace at all the levels: material, equipment, and manufacturing.

But as the IC industry moves towards the 7nm technology node it faces the challenge of mastering simultaneously several technologies and manufacturing disruptions. The whole of the semiconductor industry is discussing moving away from the well proven Si channel, introducing III-V and/or Ge based transistors while maintaining a CMOS approach, which may request gate-all-around device architecture to control channel on/off. The stacking of wafers and chips to integrate higher level in development today may become essential to fulfill the ever increasing performance and bandwidth demands. The EUV lithography is targeted to be introduced with the 7nm technology but probably in combination with double patterning techniques. In parallel the IC makers, in order to reduce manufacturing cost, are pressuring the substrate and equipment makers to introduce a larger wafer size, shifting from the established standard of 300mm to 450mm. A simultaneous transition from decades old Silicon channel, a very mature immersion lithography and wafer size creates significant challenges for our industry. This panel discussion will focus on the degree of disruptions and challenges to overcome what will be necessary for this transition to occur.

Panelists:
W. Arnold, ASML
R. Gottscho, Lam RESEARCH
K. Hasserjian, AMAT
S. Iyer, IBM
C. Maleville, SOITEC
A. Steegen, IMEC

Session 7 - TAPA I
Memory Technology - Emerging Memory

Wednesday, June 11
Chairpersons: M. Jurczak, imec
J.S. Roh, SK Hynix Inc.

7.1 - 8:05 a.m.
Paper Memory by All Printing Technology, D.-H. Lien, Z.-K. Kuo, T.-H. Huang, Y.-C. Liao, S.-C. Lee and J.-H. He, National Taiwan University

Printed and flexible electronics is expected to reach $45 billion by 2016, and paper-based electronics shows great potential to meet this increasing demand for its popularity, flexibility, low cost, mass productivity, disposability, and ease of processing. Recently, diverse electronic components on paper substrates have been invented, including conducting wires, resistors, capacitors, transistors and diodes. However, to fully activate a paper-based circuit, the memory device, a key component taking charge of programing, data storage and system setting, is still needed. In this study, nonvolatile memory electronics are implanted into conventional data storage medium, “paper,” to demonstrate the first all-printed electronic paper memory. The printed paper-based memory devices (PPMDs) can be labeled on electronics or living objects for multi-functional, wearable, on-skin, and biocompatible applications. The PPMDs would be a key electronic component to fully activate a paper-based circuit and can be directly implemented in medical biosensors, multi-functional devices, and self-powered systems.

7.2 - 8:30 a.m.
A Highly Scalable STT-MRAM Fabricated by a Novel Technique for Shrinking a Magnetic Tunnel Junction with Reducing Processing Damage, Y. Iba, A. Takahashi, A. Hatada, M. Nakabayashi, C. Yoshida, Y. Yamazaki, K. Tsunoda and T. Sugii, Low-power Electronics Association & Project

A “shrink process” for reducing the size of a magnetic tunnel junction (MTJ) and mitigating the MTJ processing damage by using a sequence of oxidation and covering silicon dioxide (SiO_2) film after MTJ etching is proposed. Using the novel process, MR (magneto-resistance) ratio was improved more than 10% and junction size was able to be reduced to 20-nm diameter in a MTJ with processing size of 35-nm diameter and, as a result, the switching current was successfully reduced more than 60%.

7.3 - 8:55 a.m.
Verification on the Extreme Scalability of STT-MRAM without Loss of Thermal Stability Below 15 nm MTJ Cell, J.H. Kim, W.C. Lim, U.H. Pi, J.M. Lee, W.K. Kim, J.H. Kim, K.W. Kim, Y.S. Park, S.H. Park, M.A. Kang, Y.H. Kim, W.J. Kim, S.Y. Kim, J.H. Park, S.C. Lee, Y.J. Lee, J.M. Yoon, S.C. Oh, S.O. Park, S. Jeong, S.W. Nam, H.K. Kang and E.S. Jung, Samsung Electronics Co., Ltd.

Scalability of interface driven perpendicular magnetic anisotropy (i-PMA) magnetic tunnel junctions (MTJs) has been improved down to 1X node which verifies STT-MRAM for future standalone memory. With developing a novel damage-less MTJ patterning process, robust magnetic and electrical performances of i-PMA MTJ cell down to 15 nm node could be achieved.

7.4 - 9:20 a.m.
Comprehensive Statistical Investigation of STT-MRAM Thermal Stability, K. Hofmann, K. Knobloch, C. Peters and R. Allinger, Infineon Technologies AG

The thermal stability Δ is a key parameter of the MRAM technology. It determines the current induced switching behavior as well as the reliability performance of e.g. data retention and read-disturb. Therefore a highly accurate assessment of Δ is mandatory for a successful MRAM technology development. In this paper we present a verification methodology based on the statistical data of a 8Mb test vehicle revealing a wide Δ distribution of ~17%.

7.5 - 9:45 a.m.
A Copper ReRAM Cell for Storage Class Memory Applications, S. Sills, S. Yasuda*, J. Strand, A. Calderoni, K. Aratani*, A. Johnson and N. Ramaswamy, Micron Technology Inc., *Sony Corporation

Hybrid memory systems that incorporate Storage Class Memory (SCM) as non-volatile cache or DRAM data backup are expected to bolster system efficiency and cost because SCM promises higher density than DRAM cache and higher speed than the storage I/F. This paper demonstrates a Cu-based resistive random access memory (ReRAM) cell that meets the SCM performance specifications for a 16Gb ReRAM with 200MB/s write and 1GB/s read.

Session 8 - HONOLULU

Beyond CMOS

Wednesday, June 11
Chairpersons: L. Selmi, University of Udine
Y.C. Yeo, National University of Singapore

8.1 - 8:05 a.m.
First Demonstration of Strained SiGe Nanowires TFETs with I_{ON} Beyond 700µA/µm, A. Villalon, C. Le Royer, P. Nguyen, S. Barraud, F. Glowacki, A. Revelant*, L. Selmi*, S. Cristoloveanu**, L. Tosti, C. Vizioz,

J.-M. Hartmann, N. Bernier, B.C. Prévitali, C.A. Tabone, F. Allain, S. Martinie, O. Rozeau and M. Vinet, CEA LETI, *University of Udine, **IMEP-LAHC

We present for the first time high performance Nanowire (NW) Tunnel FETs (TFET) obtained with a CMOS-compatible process flow featuring compressively strained $Si_{1-x}Ge_x$ (x=0, 0.2, 0.25) nanowires, $Si_{0.7}Ge_{0.3}$ Source and Drain and High-K/Metal gate. Nanowire architecture strongly improves electrostatics, while low bandgap channel (SiGe) provides increased band-to-band tunnel (BTBT) current to tackle low ON current challenges. We analyse the impact of these improvements on TFETs and compare them to MOSFET ones. Nanowire width scaling effects on TFET devices are also investigated, showing a $1/W^3$ dependence of ON current I_{ON} per wire. The fabricated devices exhibit higher Ion than any previously reported TFET, with values up to 760µA/µm and average subthreshold slopes (SS) of less than 80mV/dec.

8.2 - 8:30 a.m.
Band-to-Band Tunneling Current Enhancement Utilizing Isoelectronic Trap and its Application to TFETs, T. Mori, Y. Morita, N. Miyata, S. Migita, K. Fukuda, M. Masahara, T. Yasuda and H. Ota, National Institute of Advanced Industrial Science and Technology (AIST)

For the first time, we propose a new ON current boosting technology for TFETs utilizing an isoelectronic trap (IET), which is formed by introducing electrically inactive impurities. We have demonstrated tunneling current enhancement by 735 times in Si-based diodes and 11 times enhancement in SOI-TFETs owing to non-thermal tunneling component by the Al-N isoelectronic impurity complex. The IET technology would be a breakthrough for ON current enhancement by a few orders in magnitude in indirect-transition semiconductors such as Si and SiGe.

8.3 - 8:55 a.m.
Deep Insights into Low Frequency Noise Behavior of Tunnel FETs with Source Junction Engineering, Q. Huang, R. Huang, C. Chen, C. Wu, J. Wang, C. Wang and Y. Wang, Peking University

The detailed LFN mechanism of Tunnel FETs with different source tunnel junction design is experimentally studied for the first time, including the 1/f noise and RTS noise. The active traps located in the area where electron-hole pairs generated by non-local BTBT are found to be the main contribution to the noise mechanism. With more abrupt tunnel junction design, large noise in TFETs can be effectively reduced with lower device to device variability, which raises more requirement for the TFET device and circuit design.

8.4 - 9:20 a.m.
Investigation of $In_xGa_{1-x}As$ FinFET Architecture with Varying Indium (x) Concentration and Quantum Confinement, A. VT, N. Agrawal, G. Lavallee, M. Cantoro*, S.-S. Kim*, D.-W. Kim* and S. Datta, The Pennsylvania State University, *Samsung Electronics Co.

$In_xGa_{1-x}As$ FinFETs with varying indium percentage, x, and vertical body thicknesses, are fabricated in a closely packed fin configuration (10 fins per micron of layout area) and their relative performance analyzed and benchmarked. $In_{0.7}Ga_{0.3}As$ quantum well FinFET (QWFF) exhibits peak field effect mobility of 3,000 cm^2/V-sec at a fin width of 38nm with highest performance. Short channel $In_{0.7}Ga_{0.3}As$ QWFF (L_g=120nm) exhibits I_{DSAT} of 1.16mA/µm at V_G-V_T=1V and extrinsic peak g_m=1.9mS/µm at V_{DS}=0.5V and I_{OFF}=30 nA/µm. Components of external resistance (R_{Ext}), side wall D_{IT}, fin profile are analyzed to investigate feasibility of $In_xGa_{1-x}As$ FinFET for beyond 10nm technology node.

8.5 - 9:45 a.m.
Time-Dependent Variation: A New Defect-Based Prediction Methodology, M. Duan, J.F. Zhang, Z. Ji, W. Zhang, B. Kaczer*, T. Schram*, R. Ritzenthaler*, A. Thean*, G. Groeseneken* and A. Asenov**, Liverpool John Moores University, *imec, **University of Glasgow

The discreteness of aging-induced charges causes a Time-Dependent Variation (TDV) for nm-sized devices, which has received many attentions recently, but a widely-accepted technique for predicting the long-term TDV is missing. For the first time, we propose a methodology for test engineers to predict the long term TDV and yield and verify its prediction-capability. This methodology is based on dividing TDV into two components: a within-a-device charge fluctuation (WDF) and a non-discharging part under a given operation bias. We demonstrate that these two components originate from different types of defects and follows different aging kinetics. On one hand, the WDF originates from as-grown defects only and has a linear relation with the logarithmic measurement time window. On the other hand, the generated defects strongly contribute to the non-discharging component, which follows the same model as that for large devices: the 'As-grown-Generation (AG)' model.

Session 9 - TAPA II
Advanced CMOS Technology III-*Ge Devices*

Wednesday, June 11
Chairpersons: G. Yeap, Qualcomm Inc.
T. Tanaka, Fujitsu Semiconductor Ltd.

9.1 - 10:25 a.m.
Ge CMOS: Breakthroughs of nFETs (I_{max}=714 mA/mm, g_{max}=590 mS/mm) by Recessed Channel and S/D, H. Wu, M. Si, L. Dong, J. Zhang and P. Ye, Purdue University

We report a new approach to realize the Ge CMOS technology based on the recessed channel and source/drain (S/D). Both junctionless (JL) nFETs and pFETs are integrated on a common GeOI substrate. The recessed S/D process greatly improves the Ge n-contacts. A record high maximum drain current (Imax) of 714 mA/mm and trans-conductance (g_{max}) of 590 mS/mm, high I_{on}/I_{off} ratio of $1x10^5$ are archived at channel length (L_{ch}) of 60 nm on the nFETs. Scalability studies on Ge nFETs are conducted in sub-100 nm region down to 25 nm for the first time. Considering the Fermi level pining near the valence band edge of Ge, a novel hybrid CMOS structure with the inversion-mode (IM) Ge pFET and the JL accumulation-mode (JAM) Ge nFET is proposed.

9.2 - 10:50 a.m.
The Demonstration of Colossal Magneto-Capacitance and "Negative" Capacitance Effect with the Promising Characteristics of *Jg-EOT* and Transistor's Performance on Ge (100) n-FETs by the Novel Magnetic Gate Stack Scheme Design, M.H. Liao, S.C. Huang, C.Y. Liu, P.G. Chen, S.C. Kao, and C. Lien, National Taiwan University

In this work, tetragonal-phase $BaTiO_3$ dielectric HK layer + magnetic FePt MG film is proposed to be the gate scheme on the Ge n-FET. The ~175% κ-value improvement, ~100X *J*g reduction, and ~50% I_{on} enhancement are achieved due to the colossal magneto-capacitance effect. The magnetic field from the magnetic FePt MG film couples and triggers the more dipoles in the $BaTiO_3$ dielectric layer and then

results in the super Cgate and κ-value successfully. Moreover, the "negative" capacitance effect, which is important for the future steeper S.S device design, is also observed in this work. Super *Jg-EOT* characteristics, "negative" capacitance phenomenon, and the promising transistor's performance on the high mobility (Ge) material demonstrated in this work provides the useful solution for the future low power mobile device design.

9.3 - 11:15 a.m.

Undoped $Ge_{0.92}Sn_{0.08}$ Quantum Well PMOSFETs on (001), (011) and (111) Substrates with *In Situ* Si_2H_6 Passivation: High Hole Mobility and Dependence of Performance on Orientation, M. Liu, G. Han, Y. Liu*, C. Zhang*, H. Wang*, X. Li*, J. Zhang*, B. Cheng** and Y. Hao*, Xidian University, *Chongqing University, **Chinese Academy of Sciences

We demonstrate high performance undoped $Ge_{0.92}Sn_{0.08}$ quantum well (QW) pMOSFETs with in situ Si_2H_6 passivation on (001), (011) and (111) orientations. (011) and (111)-oriented $Ge_{0.92}Sn_{0.08}$ QW pFETs achieve higher on-state current and effective hole mobility compared to (001) devices. $Ge_{0.92}Sn_{0.08}$ (111) QW pFETs demonstrate a record high mobility of 845 $cm^2V^{-1}s^{-1}$ for GeSn p-channel devices. This is enabled by incorporating high biaxial compressive strain (1.43%) and eliminating dopant impurity scattering in the defect-free GeSn channel.

9.4 - 11:40 a.m.

Demonstration of Ge pMOSFETs with 6 Å EOT using TaN/ZrO_2/Zr-cap/n-Ge(100) Gate Stack Fabricated by Novel Vacuum Annealing and in-situ Metal Capping Method, Y. Shin, W. Chung, Y. Seo, C.-H. Lee*, D.K. Sohn* and B.J. Cho, KAIST, *Samsung Electronics

The superior gate stack was fabricated by employing novel high vacuum annealing followed by in-situ metal capping method to suppress GeO_x regrowth. Less GeO volatilization induces less Ta diffusion into gate oxide which reduces leakage current and enables further scaling. With ZrO_2/Zr-cap stack, highly scaled Ge (100) pMOSFETs have been demonstrated which shows extremely low EOT (6.06 Å), low gate leakage current of 250 nA/cm^2@$|V_g-V_{FB}|$=1V, superior SS of 70 mV/dec, and 110 cm^2/Vs of peak hole mobility.

Session 10 – TAPA III

Design Technology Co-Optimization I

Wednesday, June 11
Chairpersons: L. Baird, AMD
K. Miyashita, Toshiba Corporation

10.1 - 10:25 a.m.

Analog, RF, and ESD Device Challenges and Solutions for 14nm FinFET Technology and Beyond, J. Singh, C. Jerome, A. Wei, R. Miller, B. Arnaud, C. Lili, H. Zang, P. Kasun, P. Manjunatha, S. Biswanath, A. Kumar, S.M. Pandey, N. Iyer, A. Mittal, R. Carter, L. Zhao, E. Manfred, S. Samavedam, GLOBALFOUNDRIES

Fin-based analog, passive, RF and ESD devices have serious performance challenges, such as poor ideality, higher leakage, low breakdown voltage (BV) of diodes, BJTs with poor ideality, mismatch, weak re-surf action and low drain current(I_d/μm) of Laterally diffused MOS (LDMOS), degraded RF and 1/f noise of analog CMOS, etc. Innovative solutions which maintain process simplicity and low cost are

described in this paper. These new device designs demonstrate excellent performance, such as near perfect-ideality(n)≈1.01 diodes, low leakage, high BV, and BJTs with excellent analog behavior. Fin-based LDMOS and ESD devices outperform conventional planar devices in terms of Id/µm and ESD human body model (HBM) performance, respectively.

10.2 - 10:50 a.m.
Novel Critical Path Aware Transistor Optimization for Mobile SoC Device-Circuit Co-Design, N. Mojumder, S.C. Song, J. Wang, K. Lin, K. Rim, J. Xu and G. Yeap, Qualcomm Technologies Incorporated

We present, for the first time, a holistic system-circuit-transistor co-optimization method, named "Critical Path Aware (CPA) transistor optimization", through which we demonstrate power reduction of more than 20% in a state-of-the-art SoC design. In this method, we simplify and optimize all paths (critical and non-critical) to guide device design point for maximum power-performance benefit. We introduce novel 'Binning and Mapping of statistical Path delay (BMP)' method as a key enabler of this optimization platform, which deduces complex block level circuit data paths to a set of manageable ring oscillators, which are then used to link product level power-performance metric to transistor level optimization, taking intrinsic transistor performance, multiple Vt and multiple Lg into account simultaneously. This holistic optimization method has the potential as an important tool to extend Moore's law beyond 10nm node by maximizing performance and minimizing process complexity.

10.3 - 11:15 a.m.
Group IV Channels for 7nm FinFETs: Performance for SoCs Power and Speed Metrics, M. Garcia Bardon, P. Raghavan, G. Eneman, P. Schuddinck, M. Dehan, A. Mercha, A. Thean, D. Verkest and A. Steegen, imec

Smart Mobile SoCs combine the need for speed and for power efficiency. For the 7nm node, high-mobility materials (SiGe, Ge, and IIIV) are candidates in replacement of Si channels to continue speed improvement, but are more prone to leakage currents impacting active leakage power. Transport and voltages at scaled dimensions could also influence the gain due to mobility. We evaluate these aspects for group IV channels devices in the SoC context using an holistic approach over energy-delay metrics and in a node to node perspective. At the 7nm node, Ge devices are expected to reach 34% improvement in frequency at V_{dd} of 0.65V assuming a series resistance of 230 Ω-um can be reached. Low power complementary Si devices are needed to meet the active leakage budget of mobile SoCs.

10.4 - 11:40 a.m.
High Performance Mobile SoC Design and Technology Co-Optimization to Mitigate High-K Metal Gate Process Induced Variations, S. Yang, L. Ge, J. Lin, M. Han, D. Yang, J. Wang, K. Mahmood, T. Song, D. Yuan, D. Seo, M. Pedrali-Noy, D. Alladi, S. Wadhwa, X. Bai, L. Dai, S.S. Yoon, E. Terzioglu, S. Bazarjani and G. Yeap, Qualcomm Technologies Inc.

Despite improved device performance over traditional Poly-SiON technology, high-K metal gate flow introduces additional device variations not previously seen in Poly-SiON process, especially impacting large dimensional (WxL) devices for matching critical applications. For the first time, we report a comprehensive analysis of device variations introduced from metal gate process, GDIM and GGIM, and their sensitivity to circuit layout. Design optimization and verification mechanisms are developed to mitigate metal gate process induced variations in analog matching circuits. After co-optimization, DAC Vt mismatch is reduced by 2.1X and ADC comparator speed is improved by 23.5% in the analog blocks of an advanced mobile SoC currently in production.

Session 11 - TAPA I
3D Memory & Emerging Devices - 2

Wednesday, June 11
Chairpersons: J. Alsmeier, SanDisk
K. Tateiwa, Panasonic Corporation

11.1 - 1:30 p.m.
A Double-Density Dual-Mode Phase Change Memory Using a Novel Background Storage Scheme, J.-Y. Wu, M.-H. Lee, W.-S. Khwa, H.-C. Lu, H.-P. Li, Y.-Y. Chen, M.J. BrightSky*, T.-S. Chen, T.-Y. Wang, R.W. Cheek*, H.-Y. Cheng, E.-K. Lai, Y. Zhu*, H.-L. Lung and C.H. Lam*, Macronix International Co., Ltd., *IBM T.J. Watson Research Center

Conventional phase change memory (PCM) stores information in amorphous/crystalline states that can be read out as HRS/LRS. In this work we report a radically different mode of storage that can concurrently and independently work with the conventional storage mode. By stressing the memory cell with current we can shift the threshold for RESET switching, and the resulting R-I curve can be used to store logic states. These two modes of storage, HRS/LRS and R-I characteristics, are completely independent and do not interfere with each other, thus allow dual-mode storage. The background (R-I mode) and foreground (HRS/LRS) data can be independently written and read. Furthermore, the total number of bits stored is the multiplication of foreground and background storage. A 4-bit per cell storage scheme is illustrated.

11.2 - 1:55 p.m.
Towards the Integration of both ROM and RAM Functions Phase Change Memory Cells on a Single Die for System-On-Chip (SOC) Applications, H.L. Lung, M. BrightSky*, W.C. Chien, J.Y. Wu, S. Kim*, W. Kim*, H.Y. Cheng, Y. Zhu*, T.Y. Wang, R. Cheek*, R. Bruce* and C. Lam*, Macronix International Co., Ltd., *IBM T.J. Watson Research Center

We discovered that by changing the dielectric capping layer above the phase change memory element we can change the SET speed and data retention of the memory. This allows us, for the first time, to integrate memories of different functions on the same chip with simple processes. By using a low temperature silicon nitride capping material we can get fast SET speed down to 20ns. With a high temperature silicon nitride capping material, on the other hand, data retention is increased to > 400 years at 85°C. Based on these discoveries, we propose a unified embedded memory solution which provides both ROM and RAM functions in a single chip for SOC applications.

11.3 - 2:20 p.m.
23% Faster Program and 40% Energy Reduction of Carbon Nanotube Non-Volatile Memory with Over 10^{11} Endurance, S. Ning, T.O. Iwasaki, K. Shimomura, K. Johguchi, G. Rosendale*, M. Manning*, D. Viviani*, T. Rueckes* and K. Takeuchi, Chuo University, *Nantero

Carbon nanotube (CNT) non-volatile memory provides excellent cell characteristics of $>10^{11}$ endurance, low power, fast <5ns array program, and multi-level cell (MLC) potential. For the first time, optimal program methods are investigated considering speed, power and cell variability. Discrete cells are

measured and a multiple-pulse reset scheme is proposed to reduce verify-reset time and a gate pulse verify-reset scheme further reduces array program energy by 40%.

11.4 - 2:45 p.m.

Surface-Controlled Ultrathin (2 nm) Poly-Si Channel Junctionless FET Towards 3D NAND Flash Memory Applications, J.K. Park, S.-Y. Kim, K.-H. Lee*, S.H. Pyi*, S.-H. Lee and B.J. Cho, KAIST, *SK Hynix Semiconductor Inc.

An ultrathin junctionless (JL) charge trap flash (CTF) thin-film transistor (TFT) with a sub-2 nm thick poly-Si channel is demonstrated for 3D stacked flash memory. It provides the excellent memory performance of faster program/erase (P/E) speed, larger memory window (>12 V), and better endurance (>10^4 cycles) than inversion-mode (IM) devices; this device also has excellent 10-year data retention at 150 °C, as well as improved on/off current ratio (>10^8) and subthreshold swing (SS). The transfer characteristics and the memory performance as a function of the poly-Si channel thickness (TCh) are also systematically investigated.

Session 12 – TAPA III
Devices Physics & Reliability I

Wednesday, June 11

Chairpersons: M. Khare, IBM
B.H. Lee, Gwangju Institute of Science and Technology

12.1 - 1:30 p.m.

Spatial Mapping of Non-Uniform Time-to-Breakdown and Physical Evidence of Defect Clustering, E. Wu, B. Li, J. Stathis*, B. Linder* and T. Shaw*, IBM Semiconductor Research and Development Center, *IBM Research Division

For the first time, a spatial mapping methodology for time-dependent dielectric breakdown is successfully developed at the wafer scale. Using this technique, we can directly obtain the spatial BD distribution (wafer-maps) from TDDB data. Moreover, quantitative assessment of spatial distribution of BD defects and spatial correlation can be extracted at different stress times and various correlation spacings. This information provide much detailed assessment of BD defect clustering and fabrication process diagnosis. It is shown that BD defects are strongly clustered towards later times consistently with a recently developed time-dependent clustering model for non-uniform dielectric breakdown (E. Wu et al.p.401, IEDM 2013)

12.2 - 1:55 p.m.

Device-Level PBTI-Induced Timing Jitter Increase in Circuit-Speed Random Logic Operation, J. Lu, C. Vaz, J. Campbell, J. Ryan, K.C. Cheung, G. Jiao, G. Bersuker* and C. Young**, National Institute of Standard & Technology, *SEMATECH, **University of Texas at Dallas

We utilize eye-diagram measurements of timing jitter to investigate the impact of PBTI in devices subject to DC as well as ring oscillator (RO) and pseudo-random binary sequence (PRBS) stress waveforms. We observe that RO measurements miss the relevant random timing jitter increases which are well captured by using PRBS measurements. We also observe that DC, RO, and PRBS stresses all introduce similar increases in random timing jitter. This calls into question the widely assumed

degradation headroom between DC and AC measurements. This work collectively provides a snapshot of PBTI degradation in "real" circuit environments. It provides a path for more accurate and realistic circuit lifetime estimations and circuit timing budget criteria.

12.3 - 2:20 p.m.

Physics Based PBTI Model for Accelerated Estimation of 10 Year Lifetime, S. Zafar, A. Kerber* and R. Muralidhar, IBM T.J. Watson Research Center, *GLOBALFOUNDRIES

Threshold voltages (V_t) in high k nFETs are observed to shift under prolonged positive gate bias stressing. This bias induced V_t shift is referred as PBTI and is an important reliability issue. In this paper, we extend a previously proposed PBTI model to include de-trapping kinetics. The proposed model is verified by comparing calculated results with PBTI data measured over a wide range of stress conditions. Using the proposed model, an accelerated method for estimating 10 year lifetime is presented. This method does not require a-priori knowledge of parameters and uses a combination of voltage ramp and constant voltage measurements to estimate model parameters with the total measurement time < 1 hour. Using these extracted parameters and the model, 10 year lifetimes are estimated at different stress voltages. Since model parameters are associated with intrinsic trapping and de-trapping characteristics, the analysis provides correlation between PBTI and dielectric stack process details.

12.4 - 2:45 p.m.

The Experimental Demonstration of the BTI-Induced Breakdown Path in 28nm High-k Metal Gate Technology CMOS Devices, E.R. Hsieh, P.Y. Lu, S. Chung, K.Y. Chang*, C.H. Liu*, J.C. Ke*, C.W. Yang* and C.T. Tsai*, National Chiao Tung University, *United Microelectronics Corporation

For the first time, the breakdown path induced by BTI stress can be traced from the RTN measurement. It was demonstrated on advanced high-k metal gate CMOS devices. RTN traps in the dielectric layers can be labeled as a pointer to trace the breakdown path. It was found that breakdown path tends to grow from the interface of HK/IL or IL/Si which is the most defective region. Two types of breakdown paths are revealed. The soft-breakdown path is in a shape like spindle, while the hard breakdown is like a snake-walking path. These two breakdown paths are reflected in a two slopes TDDB lifetime plot. These new findings on the breakdown-path formation will be helpful to the understanding of the reliability in HK CMOS devices.

Session 13 – TAPA III
Advanced CMOS Technology II - FinFET

Wednesday, June 11

Chairpersons: C.-P. Chang, Applied Materials
C. Wann, TSMC

13.1 - 3:25 p.m.

Bottom Oxidation through STI (BOTS) - A Novel Approach to Fabricate Dielectric Isolated FinFETs on Bulk Substrates, K. Cheng, S. Seo, J. Faltermeier, D. Lu, T. Standaert, I. Ok, A. Khakifirooz, R. Vega, T. Levin, J. Li, J. Demarest, C. Surisetty, D. Song, H. Utomo, R. Chao,H. He, A. Madan, P. DeHaven, N. Klymko, Z. Zhu, S. Naczas, Y. Yin, J. Kuss, A. Jacob*, D. Bae**, K. Seo**, W. Kleemeier***, R. Sampson***, T. Hook, B. Haran, G. Gifford, D. Gupta, H. Shang, H. Bu, M. Na, P. Oldiges, T. Wu, B. Doris, K. Rim, E. Nowak, R. Divakaruni, M. Khare, IBM, *GLOBALFOUNDRIES, **Samsung, ***STMicroelectronics

We report a novel approach to enable dielectric isolated FinFET fabrication on bulk substrates by *bottom oxidation through STI (BOTS)*. BOTS FinFET transistors exhibit competitive performances with effective drive currents (NFET/PFET) of I_{eff} = 621/453 μA/μm at I_{off} = 10 nA/μm at V_{DD} = 0.8 V. The BOTS process results in a unique fin profile (fin tail). By extending gate vertically to the fin tail portion, the short-channel effect due to fin tail has been successfully suppressed. It is further demonstrated that the BOTS process can be extended to fabricate strained SiGe FinFETs and nanowires for future CMOS technologies.

13.2 - 3:50 p.m.

15nm-W_{FIN} High-Performance Low-Defectivity Strained-Germanium pFinFETs With Low Temperature STI-Last Process, J. Mitard, L. Witters, R. Loo, S.H. Lee*, J.W. Sun, J. Franco, L.-Å Ragnarsson, A. Brand**, X. Lu**, N. Yoshida**, G. Eneman, D.P. Brunco***, M. Vorderwestner^, P. Storck^, A.P. Milenin, A. Hikavyy, N. Waldron, P. Favia, D. Vanhaeren and A.V-Y. Thean, imec, assignee at imec from *Samsung, **Applied Materials, ***GLOBALFOUNDRIES, ^Siltronic

An STI-last integration scheme was successfully developed to fabricate low-defectivity and dopant-controlled SiGe SRB / sGe Fins. For the first time, 15 nm fin-width SiGe SRB/highly-strained Ge pFinFETs are demonstrated down to 35 nm gate length. With a CETINV-normalized GM,SAT,INT of 6.7 nm.mS/μm, the $Si_{0.3}Ge_{0.7}$ / sGe pFinFETs presented in this work improve the performance by ~90% as compared to the state-of-the-art relaxed-Ge FinFETs.

13.3 - 4:15 p.m.

Advanced RMG Module to Improve AC/DC Performance for 14nm FinFETs and Beyond, M. Togo, M. Joshi, H. van Meer, Y. Liu, C. Yong, B. Liu, X. He, X. Wu, S.Y. Mun, X. Zhang, D. Konduparthi, J. Lian, G. Bohra, W.H. Tong, C.Y. Xiao, D. Triyoso, E. Banghart, S.M. Pandey, A. Wei, R. Pal, R. Carter, M.H. Nam, M. Eller and S. Samavedam, GLOBALFOUNDRIES

An advanced Replacement Metal Gate (RMG) module was developed for 14nm node FinFETs and beyond. STI oxide extra recess increases on-current without any dedicated Source and Drain (SD) optimization. Tungsten (W) selective etch recesses work function metal (WFM), which reduces gate-contact capacitance, and improves AC performance and yields by increasing gate-contact space. Combination of work function (WF) adjust treatment and WFM optimization was applied to achieve wide range of threshold voltage (Vt) control for multiple Vt (multi-Vt) devices without any performance penalty.

13.4 - 4:40 p.m.

Lowest Variability SOI FinFETs Having Multiple V_t by Back-Biasing, T. Matsukawa, K. Fukuda, Y. Liu, K. Endo, J. Tsukada, H. Yamauchi, Y. Ishikawa, S. O'uchi, W. Mizubayashi, S. Migita, Y. Morita, H. Ota and M. Masahara, AIST

FinFETs with an amorphous metal gate (MG) are fab-ricated on silicon-on-thin-buried-oxide (SOTB) wafers for realizing both low variability and tunable threshold voltage (V_t) necessary for multiple V_t solution. The FinFETs with an amorphous TaSiN MG record the lowest on-state drain cur-rent (I_{on}) variability (0.37 %μm) in comparison to bulk and SOI planar MOSFETs thanks to the suppressed variability of V_t (A_{Vt}=1.32 mVμm), drain induced barrier lowering (DIBL) and trans-conductance (G_m). Back-biasing through the SOTB provides excellent V_t controllability keeping the low V_t vari-ability in contrast to V_t tuning by fin channel doping.

13.5 - 5:05 p.m.
Thermally Robust CMOS-Aware Ge MOSFETs with High Mobility at High-Carrier Densities on a Single Orientation Ge Substrate, C.H. Lee, C. Lu, T. Nishimura, K. Nagashio and A. Toriumi, The University of Tokyo

This paper presents the superior electron and hole mobility on a single orientation Ge substrate for compact and cost-effective CMOS applications. The different scattering mechanisms of electron and hole mobility are discussed for understanding carrier transport physics. On the basis of this understanding, the highest electron mobility of 437 cm^2/Vs and hole mobility of 213 cm^2/Vs at N_s=1e13 cm^{-2} in sub-nm EOT Ge(111) FETs are demonstrated.

13.6 – 5:30 p.m.
Demonstration of Ultimate CMOS based on 3D Stacked InGaAs-OI/SGOI Wire Channel MOSFETs with Independent Back Gate (Late News), T. Irisawa, K. Ikeda, Y. Moriyama, M. Oda, E. Mieda, T. Maeda, T. Tezuka, GNC-AIST

An ultimate CMOS structure composed of high mobility wire channel InGaAs-OI nMOSFETs and SGOI pMOSFETs has been successfully fabricated by means of sequential 3D integration. Well behaved CMOS inverters and first demonstration of InGaAs/SiGe (Ge) dual channel CMOS ring oscillators are reported. The 21-stage CMOS ring oscillator operation was achieved at Vdd as low as 0.37 V with the help of adaptive back gate bias, VBG control.

Session 14 - TAPA II
3D Systems & Packaging

Wednesday, June 11
Chairpersons: C. Mazure, Soitec Group
T. Tanaka, Tohoku University

14.1 - 3:25 p.m.
Applying a Redundancy Scheme to Address Post-assembly Yield Loss in 3D FPGAs (Invited), R.C Camarota, J. Wong, H. Liu, P. McGuire, Xilinx, Inc.

Advancement in 3D integration by die and wafer level stacking has enabled a wide variety of applications. There is an increasing demand for higher capacity and functionality in Field Programmable Gate Arrays (FPGAs) to improve performance, overall power consumption and form factor. FPGA capacity can be dramatically increased by stacking multiple smaller FPGA die on a passive interposer. The required interconnect between dies is achieved with densely packed inter-die drivers and minimum size µ-bumps. Aggressive sizing of interconnect structures poses a challenge to control post-assembly yield loss due to µ-bump or interposer defects. This paper proposes a redundancy scheme and repair technology to address this issue, significantly reducing 3D FPGA post-assembly yield loss.

14.2 - 3:50 p.m.
TSV Technology and Challenges for 3D Stacked DRAM (Invited), C.Y. Lee, S. Kim, H. Jun, K.W. Kim, S. J. Hong, SK hynix

A successful integration of Via-middle TSV process in DRAM technology with major process issues is introduced. Fast TSV open/short detection and how to trade-off in choice repair scheme is discussed. Process development for TSV volume shrink is required to reduce dynamic power for driving TSV. Fast Cu leak monitor method is essential to sustaining good quality and Fab process control.

14.3 - 4:15 p.m.
A High-Performance Low-Cost Chip-on-Wafer Package with Sub-µm Pitch Cu RDL, W.-S. Liao, C.C. Chiang, W.M. Wu, C.H. Fan, S.L. Chiu, C.C. Chiu, T.Y. Chen, C.C. Hsieh, H.Y. Chen, H.Y. Lo, L.C. Huang, T.J. Wu, W.C. Chiou, S.Y. Hou, S.P. Jeng, D. Yu, Taiwan Semiconductor Manufacturing Company

A simpler and thinner CoW structure with submicron Cu interconnect pitch of 0.8µm process has been characterized by mechanical and thermal simulations, electrical measurements, and preliminary reliability assessments. The possibility of fan-out exists to enable higher counts or lager pitch BGA connections. Board-level mechanical and thermal simulations have validated drastically increased TCoB endurance of 1250 cycles and reduced BGA and µBump straining after 1500G shock test. Moreover, relatively faster thermal conductivity than that of CoWoS structure has been clarified. Electrical continuity of 105 mm-long TSV daisy chains and leakage currents of neighboring RDL below 3µm distance have also assured 3D IC packaging system functioning. Finally, preliminary component-level reliability qualification of µHAST 168 hours, HTS 1000 hours and TC 1000 cycles have also revealed a promising potential for 12-inch WLP mass production with relatively cheap manufacturing cost, especially suitable for future high-volume mobile products that need thin packaging size.

14.4 - 4:40 p.m.
Low-Loss Silicon Interposer for Three-Dimensional System Integration with Embedded Microfluidic Cooling, P. Thadesar, L. Zheng and M. Bakir, Georgia Institute of Technology

Novel technology enablers for high-performance three-dimensional (3D) system integration are demonstrated in this paper: (a) A thick silicon interposer with 65 µm diameter and 370 µm tall low-loss polymer-embedded vias on a 150 µm pitch is fabricated and characterized demonstrating a 78% reduction in insertion loss compared to similar-sized conventional TSVs at 50 GHz; (b) Two dice with embedded microfluidic heatsinks and electrical and fluidic microbumps are assembled to an interposer demonstrating lower thermal resistance, chip-to-interposer average electrical microbump resistance of 12.06 mΩ and a robust fluidic microbump interconnection.

14.5 - 5:05 p.m.
A Novel Capacitive-Coupled Floating Gate Antenna Protection Design and Its Application to Prevent In-Process Charging Effects for 3D NAND Flash Memory, H.-T. Lue, T.-H. Yeh, K.-P. Chang, T.-H. Hsu, Y.-H. Shih and C.-Y. Lu, Macronix International Co., Ltd.

In-process charging effect is found to deteriorate the initial Vt distribution of 3D NAND Flash. In this work, we propose a novel antenna protection circuit using a capacitive coupled floating gate (CCFG) CMOS circuit that can be applied to the word line (WL), string select (SSL) and ground select transistor (GSL) decoders. Experimental results show a very low turn-on voltage (< +/-2V) for discharging, providing ideal protection for the memory devices. With this novel technique, our fully-integrated 3D NAND Flash device shows excellent initial Vt distribution free from the charging effect. Furthermore, the impact of SSL Vt distribution on the minimal Vdd bias is studied. With optimal SSL Vt distribution, it is

demonstrated that 3D VG NAND Flash can support Vdd as low as 1.6V with successful programming window.

Session 15 - TAPA II

Memory Technology - RRAM I

Thursday, June 12
Chairpersons: J. Zahurak, Micron Technology Inc.
H.-T. Lue, Macronix International Co., Ltd.

15.1 - 8:05 a.m.

Role of the Ta Scavenger Electrode in the Excellent Switching Control and Reliability of a Scalable Low-Current Operated TiN\\Ta_2O_5\\Ta RRAM Device, L. Goux, A. Fantini, A. Redolfi, C.Y. Chen, F.F. Shi*, R. Degraeve, Y.Y. Chen, T. Witters, G. Groeseneken and M. Jurczak, imec, *KU Leuven

We engineer a scalable and CMOS-friendly RRAM stack using down to 3nm ALD-based Ta_2O_5. The 20nm-sized TiN\\Ta_2O_5\\Ta device operated at 50µA exhibits ultra-fast write (~5ns) at moderate voltage (<2V) with >10^9 write endurance. We also demonstrate excellent disturb and retention characteristics, which we relate to the appropriate tuning of the oxygen chemical-potential profile along the filament by means of the Ta scavenger material and thickness.

15.2 - 8:30 a.m.

Utilizing Sub-5 nm Sidewall Electrode Technology for Atomic-Scale Resistive Memory Fabrication, K.-S. Li, C-H. Ho*, M.-T. Lee, M.-C. Chen, C.-L. Hsu, J.M. Lu, C.H. Lin, C.C. Chen, B.W. Wu, Y.F. Hou, C.Y. Lin, Y.J. Chen, T.Y. Lai, M.Y. Li, I. Yang, C.S. Wu, and F.-L. Yang**, National Nano Device Laboratories (NDL) / National Applied Research Laboratories (NARLabs), *Winbond Electronic Corporation, **Academica Sinica

A sidewall electrode technology was successfully developed for the first time in this study, improving the understanding of the working mechanism in an ultra small, functional HfO_2-based resistive random access memory (RRAM) device (< 1 × 3 nm^2). This technology exhibits potential for application in atomic-scale memories. The 1 × 3 nm^2 RRAM device exhibited an excellent performance, featuring a high endurance of more than 10^4 cycles, a large on/off verified window (>100), and reasonable reliability (stress time > 10^3s, 2 × 10^4h at 250℃). Furthermore, the 1 × 3 nm^2 RRAM device exhibited distinctive unipolar behavior when a high voltage and rapid switching operation (7 V, 50ns) were applied, and a switching mechanism model is proposed.

15.3 - 8:55 a.m.

Tailoring Switching and Endurance / Retention Reliability Characteristics of HfO_2 / Hf RRAM with Ti, Al, Si Dopants, Y. Chen, R. Roelofs*, A. Redolfi, R. Degraeve, D. Crotti, A. Fantini, S. Clima, B. Govoreanu, M. Komura**, L. Goux, L. Zhang***, A. Belmonte***, Q. Xie*, J. Maes*, G. Pourtois and M. Jurczak, imec, *ASM international, **Toshiba assignee in imec, ***also with KU Leuven

HfO_2 based RRAM offers high scalability and good reliability in 50µA operation current range. However, the dependencies between material properties and RRAM electrical characteristics which allow flexibility in device design and better matching with different selectors, are not well identified. Effect of different dopants in modifying Pt/HfO_2/TiN RRAM behaviors has been studied by ab-initio simulations. In this work, the impact of Ti, Al and Si doping of 40nm TiN/HfO2/Hf/TiN 1T1R cells is experimentally

investigated. It is shown that the dopants not only modifies the HK material properties but also influences the formation of the OEL (oxygen exchange layer) that determines RRAM switching performance and endurance/retention reliability. A general trend of dopant selection is identified in tailoring the HfO_2 based RRAM cells into different operation ranges. This offers flexibility in adjusting RRAM to be compatible with different selectors for stand-alone applications and targeting different voltage operation range for 1T1R embedded applications.

15.4 - 9:20 a.m.
A 1TnR Array Architecture using a One-Dimensional Selection Device, C. Ahn, Z. Jiang, C.-S. Lee, H.-Y. Chen, J. Liang, L. Liyanage and H.-S.P. Wong, Stanford University

A novel 1TnR array architecture using a 1D selector is demonstrated using a carbon nanotube transistor (CNFET) that is tightly integrated with the phase-change memory (PCM) cell. The 1TnR architecture enables array sizes that approach that for a 1T1R structure while achieving device density similar to a 1R array. The fabricated CNFET device has good electrical characteristics of ultra-low leakage (< 1 pA) and large ON/OFF ratio (> 1M) at high current densities to serve as a 1D selector, and 1TnR PCM cells show endurance of over 100 cycles with uniform resistance values and high ON/OFF ratios. Owing to the small contact area (~ several nm x nm), ultra-low SET and RESET currents of < 1 μA are also achieved. The same 1TnR concept is also applicable to metal oxide RRAM and CBRAM and may offer a practical trade-off between device density and performance.

15.5 - 9:45 a.m.
NbO_2-Based Low Power and Cost Effective 1S1R Switching for High Density Cross Point ReRAM Application, W.G. Kim, H.M. Lee, B.Y. Kim, K.H. Jung, T.G. Seong, S. Kim, H.C. Jung, H.J. Kim, J.H. Yoo, H.D. Lee, S.G. Kim, S. Chung, K.J. Lee, J.H. Lee, H.S. Kim, S.H. Lee, J. Yang, Y. Jeon and R.S. Williams*, SK Hynix Inc. and *Hewlett-Packard Laboratories

In this paper, 54nm cross point cell array for the low power ReRAM operation was developed with 1S1R cell structure. Through the optimization of both TiOx/TaOx based-1R and NbO_2 based-1S stacks with TiN based-electrode, the world's first and best bipolar switching characteristics with the lowest operation current (20~50uA) and sneak current (~1uA) level were acquired.

Session 16 – TAPA III
Focus Session - Interconnect

Thursday, June 12
Chairpersons: R. Arghavani, LAM Research
M. Tada, LEAP

16.1 - 8:05 a.m.
Impact of Contact and Local Interconnect Scaling on Logic Performance (Invited), S. Datta, R. Pandey, A. Agrawal, S. K. Gupta and R. Arghavani*, The Pennsylvania State University, *Lam Research

We perform a comparative analysis of metal-Si and metal-insulator-Si (MIS) contacts and quantify the impact of the contact/via resistances on logic performance. Our results show that silicide contacts account for 32% degradation in the ON current of an nFinFET (*ION*) compared to ideal contact. MIS contacts which lead to lowering of Schottky barrier height provide 12% performance gain at iso-energy.

Technology scaling to 5 nm will make MIS contact contribute 35% to the overall extrinsic resistance, with metal resistance contribution rising to 20%.

16.2 - 8:30 a.m.
Process Technology Scaling in an Increasingly Interconnect Dominated World (Invited), J.S. Clarke, C. George, C. Jezewski, A. Maestre Caro, D. Michalak, J. Torres, Intel Corporation

The RC delay and power restrictions imposed by the interconnect system can contribute to poor circuit performance in an increasingly severe manner as dimensions shrink. Resistances are increasing faster than the scale factor of the technology and capacitance improvements are constrained by mechanical requirements of the assembled stack. Collectively, these cause a bottleneck in both local and global information transfer on a chip. Novel deposition methods and novel conductor materials are being explored as means to increase conductive cross sectional area. Molecular ordering is an opportunity to simultaneously deliver capacitance and mechanical strength. Despite these improvement paths, a more holistic approach to interconnect design is needed, where the application and micro architecture are more tolerant of RC scaling constraints.

16.3 - 8:55 a.m.
What Can We Do About Barrier Layer Scaling to 5 nm Node Technology? (Invited), J. Koike, Tohoku University

Interconnect-related problems in the advanced technology node are identified and possible solutions are proposed. A PVD process of a double-layer Ta/TaN barrier is to be replaced with a CVD process of a single-layer barrier. Cu filling process can be changed from PVD seed deposition and electroplating to dynamic PVD reflow of Cu. Manganese and its oxide are shown as a possible choice of new barrier materials.

16.4 - 9:20 a.m.
***In-situ* Contact Formation for Ultra-Low Contact Resistance NiGe Using Carrier Activation Enhancement (CAE) Techniques for Ge CMOS,** H. Miyoshi, T. Ueno, K. Akiyama, Y. Hirota and T. Kaitsuka, Tokyo Electron Ltd.

We first achieved ultra-low NiGe specific contact resistivities of $2.3x10^{-9}$ Ωcm^2 and $1.9x10^{-8}\Omega cm^2$, which were both reduced from the best values ever reported by one order of magnitude, for Ge P- and N-MOS, respectively. The keys to the excellent performance were carrier activation enhancement (CAE) techniques using Ge pre-amorphization implant (PAI) or laser anneal (LA)followed by an *in-situ* contact process. Impact of ultra-low contact resistances on saturation drive current (Idsat) was also simulated for ITRS 2015 HP nFinFET.

16.5 - 9:45 a.m.
3D CMOS-MEMS Stacking with TSV-Less and Face-to-Face Direct Metal Bonding, S.L. Chua, A. Razzaq, K.H. Wee*, K.H. Li, H. Yu and C.S. Tan, Nanyang Technological University, *DSO National Laboratories

CMOS readout circuit is stacked on MEMS accelerometer using face-to-face (F2F) direct metal bonding. F2F bonding provides smaller form factor, latency, and power consumption. The CMOS chip acts as an active cap that encapsulates and provides interconnect routing to the MEMS chip. Metal bonding (Al-Au) was achieved at $300^{o}C$/10min/50N. The bond quality meets the requirements during shear and helium leak tests. The stacked CMOS/MEMS chip is verified to be functional and sustains shock test of 500g.

Session 17 - TAPA II

Technology / Circuits Joint Focus Session - Design Technology Co-Opt. II

Thursday, June 12
Chairpersons: G. Yeric, ARM
M. Masahara, AIST

17.1 - 10:25 a.m.

IoT Design Space Challenges: Circuits and Systems (Invited), D. Blaauw, D. Sylvester, P. Dutta, Y. Lee, I. Lee, S. Bang, Y. Kim, G. Kim, P. Pannuto, Y.-S. Kuo, D. Yoon, W. Jung, Z. Foo, Y.-P. Chen, S. Oh, S. Jeong, M. Choi, University of Michigan

The Internet of Things (IoT) is a rapidly emerging application space, poised to become the largest electronics market for the semiconductor industry. IoT devices are focused on sensing and actuating of our physical environment and have a nearly unlimited breadth of uses. In this paper, we explore the IoT application space and then identify two common challenges that exist across this space: ultra-low power operation and system design using modular, composable components. We survey recent low power techniques and discuss a low power bus that enables modular design. Finally, we conclude with three example ultra-low power, millimeter-scale IoT systems.

17.2 – 10:50 a.m.

Chip Package Interaction with Fine Pitch Cu Pillar Bump Using Mass Reflow and Thermal Compression Bonding Assembly Process for 20nm/16nm and Beyond, L. Zhao, A. Bao, Y. Sun, C.-J. Chen*, S. Tsai*, K. Lee, X. Zhang, D. Perry, T. Kalleberg, M. Han, S. Bezuk and G. Yeap, Qualcomm Technologies, Inc., *TSMC

This paper summarizes key learnings on 20/16nm CPI (Chip-Package-Interaction) challenges at 100um pitch and below to support ever increasing performance/cost/form factor demands for high performance mobile SoCs. CPI solutions for two types of Cu pillar interconnects using mass reflow and thermal compression type assembly process respectively are studied in technology development/ production, and separate bump cell structures are proposed.

17.3 – 11:15 a.m.

Ultralow-Voltage Design and Technology of Silicon-on-Thin-Buried-Oxide (SOTB) CMOS for Highly Energy Efficient Electronics in IoT Era (Invited), S. Kamohara, N. Sugii, Y. Yamamoto, H. Makiyama, T. Yamashita, T. Hasegawa, S. Okanishi, H. Yanagita, M. Kadoshima, K. Maekawa, H. Mitani, Y. Yamagata, H. Oda, Y. Yamaguchi, K. Ishibashi*, H. Amano**, K. Usami+, K. Kobayashi++, T. Mizutani#, T. Hiramoto#, Low-power Electronics Association & Project, *The University of Electro-Communications, **Keio University, +Shibaura Institute of Technology, ++Kyoto Institute of Technology, #Institute of Industrial Science, The University of Tokyo

Ultralow-voltage (ULV) operation of CMOS circuits is effective for significantly reducing the power consumption of the circuits. Although operation at the minimum energy point (MEP) is effective, its slow operating speed has been an obstacle. The silicon-on-thin-buried-oxide (SOTB) CMOS is a strong candidate for ultralow-power (ULP) electronics because of its small variability and back-bias control. These advantages of SOTB CMOS enable power and performance optimization with adaptive *V*th control at ULV and can achieve ULP operation with acceptably high speed and low leakage. In this paper, we describe our recent results on the ULV operation of the CPU, SRAM, ring oscillator, and, other logic

circuits. Our 32-bit RISC CPU chip, named “Perpetuum Mobile,” has a record low energy consumption of 13.4 pJ when operating at 0.35 V and 14 MHz. Perpetuum-Mobile micro-controllers are expected to be a core building block in a huge number of electronic devices in the internet-of-things (IoT) era.

17.4 - 11:40 a.m.
Cost and Power/Performance Optimized 20nm SoC Technology for Advanced Mobile Devices, G. Nallapati, J. Zhu, J. Wang, J.Y. Sheu*, K.L. Cheng*, C. Gan, D. Yang, M. Cai, J. Cheng, L. Ge, Y. Chen, R. Bucki, B. Bowers, F. Vang, X. Chen, O. Kwon, S. Yoon, C.C Wu*, P.R. Chidambaram, M. Cao*, J. Fischer, E. Terzioglu, Y.J. Mii*, and G. Yeap, Qualcomm Technologies, Inc., *TSMC

A cost competitive 20nm technology node is described that enabled industry-first 20nm cellular modem chip with 2x peak data rates vs 28nm, and 2x carrier aggregation. Process and design enhancements for layout context optimization, and continuous process improvements resulted in 18% boost in circuit performance while simultaneously achieving >30% power reduction. 3 mask local interconnect and i64nm double patterning lower level metals – with yield-friendly single color pitch of 95nm 90nm (=gate pitch) single color pitch construstfor cell abutment - were used for achieving ~2x gate density. Single patterning 80nm pitch metal for routing levels was optimized for both density and performance. Active/passive device and double pattern metal mask count was optimized to reach process should-cost goals. Resulting technology provides cost reduction vs 28 HKMG per close to historical trend, and also cost-competitiveness vs 28 PolySiON. Leveraging of yield learning of this common back-end metallization results in up to 6 month pull-in of 16nm Finfet node yield ramp.

Session 18 – TAPA III
Device Physics and Reliability - II

Thursday, June 12
Chairpersons: B.-K. Liew, nVidia
H. Morimura, NTT Microsystem Integration Labs

18.1 - 10:25 a.m.
Direct Measurement of the Dynamic Variability of 0.120µm^2 SRAM Cells in 28nm FD-SOI Technology, J. El Husseini, X. Garros, A. Subirats, A. Makosiej, O. Weber, O. Thomas, V. Huard*, X. Federspiel* and G. Reimbold, CEA-LETI, *STMicroelectronics

A new characterization technique is successfully used to measure the dynamic variability of SRAMs at the bitcell level. This effective method easily replaces heavy simulations based on measures at transistors level. Moreover, an analytical model is proposed to explain the SRAM cell variability results. Using this model, the read failure probability after 10 years of working at operating conditions is estimated and is shown to be barely impacted by this BTI-induced variability in this FDSOI technology.

18.2 - 10:50 a.m.
Ultra-Low Voltage (0.1V) Operation of V_{th} Self-Adjusting MOSFET and SRAM Cell, A. Ueda, S.-M. Jung, T. Mizutani, A. Kumar, T. Saraya and T. Hiramoto, University of Tokyo

A V_{th} self-adjusting MOSFET consisting of floating gate is proposed and the ultra-low voltage operation of the V_{th} self-adjustment and SRAM cell at as low as 0.1V is successfully demonstrated. In this device, V_{th} automatically decreases at on-state and increases at off-state, resulting in high I_{on}/I_{off} ratio as well as

stable SRAM operation at low V_{dd}. The minimum operation voltage at 0.1V is experimentally demonstrated in 6T SRAM cell with V_{th} self-adjusting nFETs and pFETs.

18.3 - 11:15 a.m.

Systematic Study of RTN in Nanowire Transistor and Enhanced RTN by Hot Carrier Injection and Negative Bias Temperature Instability, K. Ota, M. Saitoh, C. Tanaka, D. Matsushita and T. Numata, Toshiba Corporation

We experimentally study the random telegraph noise (RTN) in nanowire transistor (NW Tr.) with various NW widths (*W*), lengths (*L*), and heights (*H*). Time components of RTN such as time to capture and emission are independent of NW size, while threshold voltage fluctuation by RTN was inversely proportional to the one-half power of circumference corresponding to the conventional carrier number fluctuations regardless of the side surface orientation. Hot carrier injection (HCI) and negative bias temperature instability (NBTI) induced additional carrier traps leading to the increase in the number of observed RTN. Moreover, threshold voltage fluctuation is enhanced by HCI and NBTI and increase of threshold voltage fluctuation becomes severer in narrower W.

18.4 - 11:40 a.m.

Further Understandings on Random Telegraph Signal Noise through Comprehensive Studies on Large Time Constant Variation and its Strong Correlations to Thermal Activation Energies, J. Chen, Y. Higashi, K. Kato and Y. Mitani, Toshiba Corporation

Comprehensive studies on random telegraph signal (RTS) noise have been done to understand carrier trapping processes, with a main focus on the large variations of time constants. It is observed that time constant distributions, as well as thermal activation energy distributions, weakly depend on the substrate doping concentrations or surface orientations. For individual traps, time constants are quite stable under strong negative bias stressing with serious interface degradation. More importantly, correlations of time constants and thermal activation energies with a narrow distribution window are experimentally observed for the first time. With further discussions, it is concluded that the activation energy variation is the main reason for large time constant distributions, and carrier trapping process is thought to be most likely from multiphonon-assisted tunneling process.

Luncheon & Executive Panel Discussion

Thursday 6/12, 12:15 pm

Emerging Semiconductor Industry Trends and Implications

Moderator: Dan Hutcheson, CEO and Chairman of VLSI Research Inc and author of The Chip Insider

Looking past traditional scaling that has driven semiconductor industry over the last few decades, we see a new paradigm unfolding around us. Emerging trends and applications information technology are fueling unprecedented demands on information ubiquity – user-friendly, mobile anywhere, any time. This has opened up the need for a new class of systems – both mobile and fixed – which are in turn driving the need for a new class of device technologies, circuits and designs. The impact of this paradigm shift on semiconductor industry professionals and researchers in the academic community is profound. For example, if wearable computing or IoT become increasingly larger segments of application space - what technology/system/ manufacturing/economic implications does this have? Will we need to push harder on new materials and low power technologies? Will we need to think of new ways to integrate dissimilar components (wireless, NVM, RF/Analog/digital, MEMS, batteries etc) or traditional SOC/SIP suffice? The panel will deliberate on this topic and discuss trends, applications that are shaping around us, industry needs, infrastructural/manufacturing gaps and economic challenges.

Panelists:

Scott DeBoer, Micron
Venu Menon, Texas Instruments
Om Nalamasu, AMAT
Yoshifumi Okamoto, Panasonic
Gary Patton, IBM
Jack Sun, TSMC

Session 19 - TAPA II
Emerging Device Technology II

Thursday, June 12
Chairpersons: T. Ernst, CEA-LETI, MINATEC
K. Uchida, Keio University

19.1 - 1:30 p.m.
$In_{0.53}Ga_{0.47}As$ Quantum-Well MOSFET with Source/Drain Regrowth for Low Power Logic Applications,
X. Zhou, A. Alian, Y. Mols, R. Rooyackers, G. Eneman, D. Lin, T. Ivanov, M.A. Pourghaderi, N. Collaert and A. Thean, Imec

This paper reports $In_{0.53}Ga_{0.47}As$ quantum-well MOSFET with source/drain regrowth for logic applications. For a device with L_g=100nm and EOT of 1.1nm, Ion=550µA/µm at 0.5V and fixed I_{off}=100nA/µm, peak $g_{m,ext}$=2.21mS/µm, and SS=82mV/dec at V_{ds}=0.5V are obtained. Minimum SS at V_{ds}=0.5V remains 80-87mV/dec for all gate lengths from 500nm to 75nm. To our knowledge, these are the best planar InGaAs-channel MOSFETs in literature. We attribute these advances to the improvement in epitaxy especially the InAlAs buffer, III-V/oxide interface engineering, and source/drain regrowth. A

process has been developed to improve dielectric/III-V interface. The effects of EOT scaling on device performance are studied.

19.2 - 1:55 p.m.

Electrostatics and Performance Benchmarking using all Types of III-V Multi-Gate FinFETs for sub 7nm Technology Node Logic Application, R.-H. Baek, T.-W. Kim, T. Michalak*, C. Borst*, C. Shin**, W. Park**, S.-C. Song***, G. Yeap***, R. Hill, C. Hobbs, W. Maszara^, D.-H. Kim and P. Kirsch, SEMATECH, *CNSE, **KANC, ***QUALCOMM, ^GLOBALFOUNDRIES

In this paper, we conducted the sub 7nm technology benchmarking for logic application using performance comparison between III-V multi-gate(double, tri, gate-all-around) nMOSFET and Si nFinFET. The benchmarking was executed based on the physical parameters extracted from Virtual-Source(VS) modeling and well-calibrated TCAD simulation. Especially by quantitatively investigating fin width(W_{fin}) and interface trap(D_{it}) effects on electrostatic of III-V multi-gate(MG) nMOSFET which is critical to device scaling, we proposed a device design strategy for sub 7nm technology node.

19.3 - 2:20 p.m.

Scaling to 50-nm C-Axis Aligned Crystalline In-Ga-Zn Oxide FET with Surrounded Channel Structure and Its Application for Less-Than-5-nsec Writing Speed Memory, Y. Kobayashi, D. Matsubayashi, S. Nagatsuka, Y. Yakubo, T. Atsumi, Y. Shionoiri, S. Hondo, T. Yamamoto, Y. Okazaki, M. Nagai, S. Sasagawa, D. Ito, Y. Hata, T. Hamada, R. Arasawa, K. Hanaoka, M. Sakakura, H. Suzawa, Y. Yamamoto and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd.

We report novel FETs with a structure in which not only the top surface but also the side surfaces of island-shaped c-axis aligned crystalline indium-gallium-zinc oxide (CAAC-IGZO) serving as a channel are surrounded by a gate electrode, that is, surrounded channel CAAC-IGZO FETs. The FETs maintained their favorable subthreshold characteristics even if the channel length was scaled down to approximately 50 nm, i.e., normally-off, DIBL of 67 mV/V, SS of 92 mV/dec, and an off-state current lower than the measurement limit (0.1 pA) for a gate insulating film EOT of 11 nm. Moreover, we applied an FET with such a structure to a memory and discussed the writing time and the retention time, which were expected to be less than 5 ns and greater than 1,000 sec, respectively, for storage capacitance of 1 fF from circuit simulation.

19.4 - 2:45 p.m.

Monolithic Three-Dimensional Integration of Carbon Nanotube FETs with Silicon CMOS, M. Shulaker, K. Saraswat, H.-S.P. Wong and S. Mitra, Stanford University

We demonstrate the first VLSI-compatible approach for monolithic three-dimensional (3D) integration of carbon nanotube field effect transistors (CNFETs) with silicon CMOS for high-performance digital logic applications. Fine-grained monolithic 3D integration is demonstrated at the logic gate level, whereby individual logic gates are composed of both CNFETs and silicon FETs. Monolithic 3D integration is additionally achieved at the circuit-level, with CNFET logic gates cascaded with silicon CMOS logic gates, creating hybrid CNFET−silicon CMOS logic circuits. All the CNFET fabrication steps are VLSI-scalable and silicon CMOS compatible. CNFET fabrication is performed after the silicon CMOS processing is completed and the CNFETs directly overlap on top of the silicon FETs. This work demonstrates both the compatibility of CNFETs with silicon CMOS and the ability to achieve monolithic 3D ICs simultaneously using silicon CMOS and CNFETs.

Session 20 – TAPA III
Process Technology II

Thursday, June 12
Chairpersons: C.-P. Chang, Applied Materials
Y. Akasaka, Tokyo Electron Ltd.

20.1 - 1:30 p.m.
Statistical Demonstration of Silicide-Like Uniform and Ultra-Low Specific Contact Resistivity using a Metal/High-k/Si Stack in a Sidewall Contact Test Structure, K. Majumdar, R. Clark*, T. Ngai, K. Tapily*, S. Consiglio*, E. Bersch, K. Matthews, E. Stinzianni, Y. Trickett*, G. Nakamura*, C. Wajda*, G. Leusink*, H. Chong**, V. Kaushik**, J. Woicik***, C. Hobbs and P. Kirsch, SEMATECH, *TEL Technology Center, **CNSE, ***NIST

We demonstrate a 300mm wafer scale conformal contact process to achieve uniform ultra-low specific contact resistivity for metal/high-k/n^+Si (MIS) contacts. To achieve conformal contacts, we use a sidewall TLM (STLM) test structure that helps to minimize current crowding effect and variability. A systematic study is provided by varying doping density, high-k material (LaO_x, ZrO_x and TiO_x) and high-k thickness to optimize specific contact resistivity. The obtained specific contact resistivity and its uniformity are found to be comparable with standard nickel silicide technology, with a possibility of further improvement by use of lower work-function metal.

20.2 - 1:55 p.m.
The Demonstration of *D-SMT* Stressor on Si and Ge n-FinFETs, M.H. Liao, P.G. Chen, S.C. Huang, S.C. Kao, C.X. Hung, K.H. Liu, C. Lien, C.Y. Liu, National Taiwan University

The ~20% *Id,sat* improvement is demonstrated successfully on the Si and Ge n-FinFETs with the implement of D-SMT stressor for the first time, based on the optimization of dislocation angle and the understanding of crystal re-growth velocities along different surface planes and directions in Si and Ge. The mobility enhancement ratio with D-SMT stressor in Ge n-FinFET (37%) is found to be larger than it in the Si n-FinFET (30%). Ultra-high capping stress film (>3 GPa)is the must to modify the crystal re-growth velocities along the [100] and [110] directions for the dislocation angle optimization and the implement of D-SMT on the FinFET structure. The larger stress and mobility enhancement ratio are observed in the narrower gate width device, due to the effect of triple crystal re-growth directions. Finally, the mobility enhancement ratio with the stress on the Si (100)/[110], Si (110)/[110], Ge (100)/[110] and Ge (110)/[110] is calculated theoretically.

20.3 - 2:20 p.m.
Design Methodology of Tri-Gate Poly-Si MOSFETs with 10nm Nanowire Channel to Enhance Short-Channel Performance and Reduce V_{th} & I_d Variability, M. Saitoh, K. Ota, C. Tanaka and T. Numata, Toshiba Corporation

We present the optimum design of tri-gate poly-Si nanowire transistors (NW Tr.) based on the systematic performance and variability analysis for various NW width (W_{NW}) and thickness (T_{Si}) down to 10nm. I_{on} difference between poly-Si and crystalline-Si Tr. at short L (down to 25nm) is much smaller than long L due to poly-Si defect-barrier lowering by high lateral field. Ion of poly-Si pFETs is close to nFETs due to smaller interface defects. Both W_{NW} and T_{Si} scaling reduces S factor, SCE and A_{vt} (V_{th} & I_d variations) caused by random grain placement. Avt of thin poly-Si Tr. falls even below doped bulk Tr.

Since short-NW Tr. suffers from high R_{SD} and low μ, narrow and tall poly-Si NW Tr. is the best for 3D CMOS.

20.4 - 2:45 p.m.
Enhanced Drivability of High-V_{bd} Dual-Oxide-Based Complementary BEOL-FETs for Compact On-Chip Pre-Driver Applications, H. Sunamura, N. Inoue, N. Furutake, S. Saito, M. Narihiro, M. Hane and Y. Hayashi, Renesas Electronics Corporation

Enhanced current drivability of BEOL-process-compatible dual-oxide complementary BEOL-FETs on LSI-interconnects with just two additional masks to the state-of-the-art BEOL process is demonstrated, aiming at high-V_{bd} pre-driver operation. We have developed processes so that IGZO-based NFETs have lower AR_{on} as compared to currently available Si power devices. We also developed new SnO processes, realizing a 30x I_{on} boost for PFETs. Dual oxide semiconductor channels are integrated to form BEOL-CMOS inverters with stable and sharp cut-off characteristics for lower power operation, leading to a successful operation of an integrated 6T-SRAM cell. Pre-driver capability of NFET inverters is demonstrated with MCU-controlled operation of brushless DC (BLDC) motors. This technology is a strong candidate to realize high-V_{bd} pre-drivers and low-power logic on BEOL, which gives standard LSIs a special add-on function for smart society applications.

Session 21 - TAPA II
Emerging Device Technology I

Thursday, June 12
Chairpersons: A. Ionescu, Swiss Federal Institute of Technology
N. Sugii, LEAP

21.1 - 3:25 p.m.
Integration of Silicon Photonics in Bulk CMOS, R. Meade, J. Orcutt*, K. Mehta*, O. Tehar-Zahav***, D. Miller***, M. Georgas*, B. Moss*, C. Sun*, Y.-H. Chen*, J. Shainline**, M. Wade**, R. Bafrali, Z. Sternberg***, G. Machavariani***, G. Sandhu, M. Popovic**, R. Ram* and V. Stojanovic*, Micron Technology, Inc., *Massachusetts Institute of Technology, **University of Colorado, Boulder, ***Micron Semiconductor Israel

This paper presents the first functional monolithic integration of a silicon photonic link on bulk CMOS. Other research groups have published on SOI devices or "stand alone" silicon photonics (i.e. not monolithically integrated). This paper is different in that, for the first time, a working optical link has been demonstrated on an economically feasible (specifically for memory) CMOS platform. Today, 3D integration is a major industry focus in part due to the power and performance requirements of chip-to-chip I/O. While 3D integration is important, this research shows a clear alternative path that has significant benefits.

21.2 - 3:50 p.m.
Germanium-Tin on Silicon Avalanche Photodiode for Short-Wave Infrared Imaging, Y. Dong, W.Wang, X. Xu, X. Gong, D. Lei, Q. Zhou, Z. Xu*, S.-F. Yoon*, G. Liang and Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

The first demonstration of Germanium-Tin on Silicon ($Ge_{1-x}Sn_x/Si$) avalanche photodiode (APD) for short-wave infrared (SWIR) imaging is reported. The temperature dependence of breakdown voltage was

characterized. An extracted thermal coefficient of 0.05% K^{-1} indicates that the $Ge_{1-x}Sn_x$/Si APD achieved a lower thermal sensitivity than conventional III-V-based APDs. At the wavelength of 1600 to 1630 nm, a responsivity of ~ 1 A/W (bias voltage V_{bias} = -9.7 V) was achieved due to the internal avalanche gain of $Ge_{1-x}Sn_x$/Si APD. The monolithic and CMOS-compatible $Ge_{1-x}Sn_x$/Si APD presented here shows promise in SWIR imaging applications where low-cost and high sensitivity sensing arrays are needed.

21.3 - 4:15 p.m.

Advanced 1.1um Pixel CMOS Image Sensor with 3D Stacked Architecture, J.C. Liu, D.N. Yaung, J.J. Sze, C.C. Wang, G. Hung, C.J. Wang, T.H. Hsu, R.J. Lin, T.J. Wang, W.D. Wang, H.Y. Cheng, J.S. Lin, S.J. Tsai, C.C. Chuang, W.I. Hsu, S.Y. Chen, K.C. Huang, W.H. Wu, S. Takahashi, Y.L. Tu, C.S. Tsai, R.L. Lee, W.P. Mo, F.J. Shiu, Y.P. Chao, and S.G. Wuu, Taiwan Semiconductor Manufacturing Company

This paper demonstrates an advanced 1.1um pixel backside illuminated CMOS image sensor with a 3D stacked architecture. The carrier wafer in conventional BSI is replaced by ASIC wafer, which contains a part of periphery circuit and is connected to the sensor wafer through bonding technology. With proper layout design and process improvement, the impact of 3D connection (Through Via, TV) on the sensor performance can be significantly minimized. In addition, for the first time, the degradation of stacked pixel performance during the folded circuit operation under sensor array is found and improved. The final stacked sensor exhibits the comparable pixel performances to conventional BSI. Furthermore, stacked architecture provides the opportunity to enhance sensor performance by the separate process tuning for sensor wafers (without any effect on ASIC wafers), leading to a further improvement of dark performance.

21.4 - 4:40 p.m.

High-Q Inductors on Locally Semi-Insulated Si Substrate by Helium-3 Bombardment for RF CMOS Integrated Circuits, N. Li, K. Okada, T. Inoue*, T. Hirano, Q. Bu, A.T. Narayanan, T. Siriburanon, H. Sakane* and A. Matsuzawa, Tokyo Institute of Technology, *S.H.I. Examination & Inspection, Ltd.

A novel helium-3 ion bombardment technique is proposed for creating locally semi-insulating substrate areas. A helium-3 dose of only $1.5x10^{13}$ cm^{-2} increases a Si substrate resistivity from 6 Ω-cm to 1.5 kilo Ω-cm, which improves the quality factor of a 2-nH inductor with a 140-um diameter by 38% (Q=16.3). An aluminum mask is used for covering active areas, and at most 15-µm distance from the mask edge is required to avoid the p-n junction leakage. The proposed technique is applied to an 8-GHz oscillator, and an 8.5-dB improvement in the measured phase noise has been achieved.

21.5 - 5:05 p.m.

Electrical and Reliability Characteristics of a Scaled (~30nm) Tunnel Barrier Selector (W/Ta_2O_5/TaO_x/TiO_2/TiN) with Excellent Performance (J_{MAX} > 10^7A/cm^2), J. Woo, J. Song, K. Moon, J.H. Lee, E. Cha, A. Prakash, D. Lee, S. Lee, J. Park, Y. Koo, C.G. Park and H. Hwang, Pohang University of Science and Technology

We demonstrate a selector device with excellent performances (J_{MAX} > 10^7A/cm^2, switching speed < 20ns) at the 30nm cell size. Furthermore, these promising device characteristics were achieved in a fully CMOS compatible stack (W/Ta_2O_5/TaO_x/TiO_2/TiN) with extremely thin oxide layer (< 10nm). Through the comprehensive understanding on the exponential I-V curve, the effect of intrinsic/extrinsic factors such as scaling (area and thickness), and parasitic components were systemically investigated.

21.6 – 5:30 p.m.

High-Performance MoS_2 Field-Effect Transistors Enabled by Chloride Doping: Record Low Contact Resistance (0.5 kΩ•µm) and Record High Drain Current (460 µA/µm) (Late News), L. M. Yang, Y. C. Du, H. Liu, H. Wu, P. D. Ye, K. Majumdar*,P. Y. Hung*, R. Tieckelmann*, C. Hobbs*, M. Hatzistergos**, W. Tsai***, Purdue University, *SEMATECH, **SUNY CNSE, ***Intel

In this paper, we report a novel chemical doping technique to reduce the contact resistance (Rc) of transition metal dichalcogenides (TMDs) – eliminating two major roadblocks (namely, doping and high Rc) towards demonstration of high-performance TMDs field-effect transistors (FETs). By using 1,2 dichloroethane (DCE) as the doping reagent, we demonstrate an active n-type doping density > 2E19 cm-3 in a few-layer MoS_2 film. This enabled us to reduce the Rc value to a record low number of 0.5 kΩ•µm, which is ~10x lower than the control sample without doping. The corresponding specific contact resistivity (ρc) is found to decrease by two orders of magnitude. With such low Rc, we demonstrate 100 nm channel length (Lch) MoS_2 FET with a drain current (Ids) of 460 µA/µm at Vds = 1.6 V, which is twice the best value reported so far on MoS_2 FETs.

Session 22 – TAPA III

Memory Technology: RRAM II

Thursday, June 12

Chairpersons: K. Attenborough, NXP Central R&D
T.-R. Yew, UMC

22.1 - 3:25 p.m.

Lateral and Vertical Scaling Impact on Statistical Performances and Reliability of 10nm TiN/Hf(Al)O/Hf/TiN RRAM Devices, A. Fantini, L. Goux, A. Redolfi, R. Degraeve, G. Kar, Y. Chen and M. Jurczak, imec

We present a systematic investigation of the impact of aggressive lateral and vertical TiN/Hf(Al)O/Hf/TiN RRAM cells stack scaling down to 10nmx10nm cell size and 5nm thickness on performance and reliability. We demonstrate that median values and 1-sigma dispersion of programming voltages, resistances and disturb are not affected by lateral and vertical scaling in agreement with QPC/hour glass conduction model. We also demonstrate that endurance robustness is instead adversely affected by both a reduction of total stack thickness and lateral cell size, the latter probably due to a reduction of the available ion supply in the oxygen exchange layer (OEL) as consequence of scaling.

22.2 - 3:50 p.m.

Towards High-Speed, Write-Disturb Tolerant 3D Vertical RRAM Arrays, H.-Y. Chen, B. Gao*, H. Li*, R. Liu*, P. Huang*, Z. Chen*, B. Chen*, F. Zhang*, L. Zhao*, Z. Jiang*, L. Liu, X. Liu, J. Kang, S. Yu**, Y. Nishi* and H.-S.P. Wong*, Peking University, *Stanford University, **Arizona State University

3D RRAM array suffers more serious reliability issues than 2D array due to the additional dimension involved. This paper systematically assesses the cell-location-dependent write-access (selected cells) and disturbance issues (unselected cells) for a 3D vertical RRAM array. Using a combination of experiments and simulations, a methodology is developed to enable array-level evaluation by conducting single device measurements and without the need to fabricate a full 3D array. Based on this evaluation method, it is found that a double-sided bias (DSB) scheme improves write-disturb tolerance by a factor of 1800 and reduces write latency by 19 % under worst-case analyses.

22.3 - 4:15 p.m.
Fast Step-Down Set Algorithm of Resistive Switching Memory with Low Programming Energy and Significant Reliability Improvement, Y. Meng, X. Xue, Y. Song, J. Yang, B.A. Chen, Y. Lin, Q. Zou*, R. Huang* and J. Wu*, Fudan University, *Semiconductor Manufacturing International Corp.

We propose an asymmetric write algorithm of step-down set/step-up reset without verify for the first time. The demonstration is carried out on a 128Kb test macro of AlO_x/WO_x bi-layer ReRAM fabricated based on 0.18μm logic process. The set and reset energy per bit are reduced by 34% and 20% respectively. The set and reset access time decrease by 54% and 32% respectively. The mean value of endurance distribution is improved by 2 orders of magnitude from 10^7 to 10^9. R_{on} and R_{off} retention failure rate is reduced by 88% and 71% respectively. R_{off}/R_{on} window enlarges from 25x to 180x. The reliability improvements are attributed to refinement of CF shape and size by the step-down set algorithm.

22.4 - 4:40 p.m.
1T-1R Pillar-Type Topological-Switching Random Access Memory (TRAM) and Data Retention of $GeTe/Sb_2Te_3$ Super-Lattice Films, M. Tai, T. Ohyanagi, M. Kinoshita, T. Morikawa, K. Akita, S. Kato*, H. Shirakawa*, M. Araidai*, K. Shiraishi* and N. Takaura, Low-power Electronics Association & Project, *University of Tsukuba

A 1T-1R pillar-type “topological-switching RAM” (TRAM) and the data retention of $GeTe/Sb_2Te_3$ super-lattice were investigated. Reset voltage of TRAM, 2 V, was 40 % of that of the conventional PCM with Ge2Sb2Te5. From data retention evaluation, the TRAM was found to endure the retention at 260˚C for 18 hours.

22.5 - 5:05 p.m.
A Fast and Low-Voltage Cu Complementary-Atom-Switch 1Mb Array with High-Temperature Retention, N. Banno, M. Tada, T. Sakamoto, M. Miyamura, K. Okamoto, N. Iguchi, T. Nohisa and H. Hada, Low-power Electronics Association & Project (LEAP)

Fast (10ns) and low voltage (2V) programming of a Cu complementary-atom-switch (CAS) has been demonstrated in a 1Mb switch array for the first time. A newly developed redox-control buffer of $Al_{0.5}Ti_{0.5}O_x$ leads to extreme-steep slope switching of 56mV/dec., voltage dependent time-to-ON-state, by eliminating metallic Al residues at the Cu surface. The programmed ON-state shows long lifetimes both under data-retention test at 260 degrees Celsius and DC stress test (I_{max}=140μA) at 125 degrees Celsius. A redox-control technology is indispensable for conducting bridges used in a low-power, nonvolatile programmable logic (NPL).