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Media Contacts:

Secretariat for VLSI Symposia (Japan and Asia)
c/o ICS Convention Design, Inc.
Chiyoda Bldg. 1-5-18 Sarugaku-cho, Chiyoda-ku,
Tokyo 101-8449 Japan
Tel: +81-3-3219-3541
E-mail: vlsisymp@ics-inc.co.jp

BtB Marketing (NorthAmerica and EU)
Chris Burke
BtB Marketing
co-Media Relations Director
Tel: +1-919-872-8172
E-mail: chris.burke@btbmarketing.com

For Immediate Release

Tip Sheet for
2015 Symposia on VLSI Technology and Circuits

KYOTO, JAPAN -- This Tip Sheet is an advance look at some of the most newsworthy papers to be presented at the 2015 Symposia on VLSI Technology & Circuits, which will be held at the Rihga Royal Hotel Kyoto here June 15-18, 2015 (Technology Symposium) and June 16-19, 2015 (Circuits Symposium).

See the "Media" tab of the Symposia website for higher-resolution versions of these images. (www.vlsisymposium.org/press.html)
A glossary of technical terms is at the end of this tip sheet.

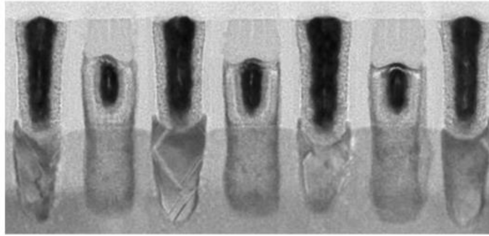
I) Technical Highlights from 2015 Symposium on VLSI Technology

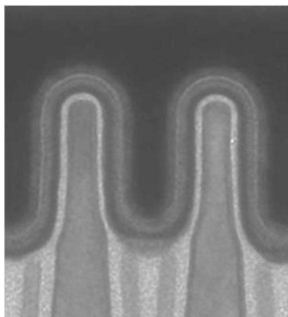
A) Platform Technology for CMOS Manufacturing

14 nm SoC Platform Technology for Low Power, High Performance and High Density SoC Products:
Intel discusses their 14 nm SoC platform based on the 2nd generation Tri-Gate transistor technology that has been optimized for density, low power and wide dynamic range. 70 nm gate pitch, 52 nm metal pitch and 0.0499 um^2 HDC SRAM cells are the most aggressive design rules reported for 14/16 nm node SoC process to achieve Moore's Law 2x density scaling over 22 nm node. High performance NMOS/PMOS drive currents of 1.3/1.2 mA/μm, respectively, have been achieved at 0.7 V and 100 nA/μm off-state leakage, 37%/50% improvement over 22 nm node. Ultra-low power NMOS/PMOS drives are 0.50/0.32 mA/um at 0.7 V and 15pA/μm Ioff. This SoC technology deploys high voltage I/O transistors supporting up to 3.3 V I/O, and supports a full range of analog, mixed-signal and RF features. The Symposia features other papers from Intel with the same 14nm platform: paper number C23-1 in circuits: refer to technology tip sheet. ***(Paper T2-1, "A 14 nm SoC Platform Technology Featuring 2nd***

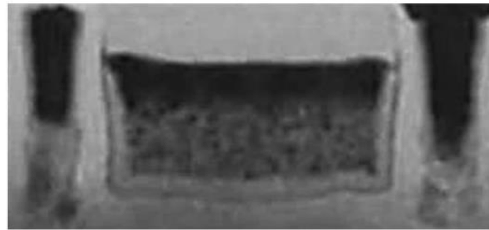
Generation Tri-Gate Transistors, 70 nm Gate Pitch, 52 nm Metal Pitch, and 0.0499 um² SRAM cells, Optimized for Low Power, High Performance and High Density SoC Products," C.-H. Jan et al., Intel. See also Paper C23-1, "Broadwell : A family of IA 14nm processors," A. Nalamalpu et al. Intel)

High Speed Logic Transistor





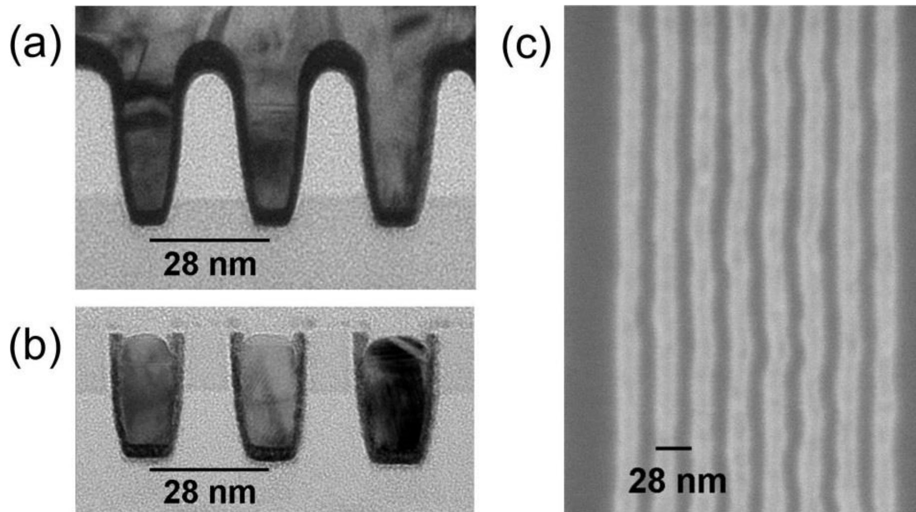
High Voltage I/O Transistor



Fin/Gate cross-sectional TEMs of logic (top) and HV I/O transistors (bottom).

Resistivity of Copper Interconnects beyond the 7 nm Node:

Interconnect wiring delay due to copper resistance increase is one of major challenges for 7nm node CMOS. IBM and GLOBALFOUNDRIES intensively studied scattering mechanisms contributing to the resistivity of copper. The resistivity of damascene copper is measured at pitch ranging down to 40 nm and copper cross-sectional area as low as 140 nm^2. Metallization by copper reflow is demonstrated at 28 nm pitch with patterning by directed self-assembly (DSA). Extremely low line-edge-roughness (LER) is obtained by surface reconstruction of a single crystal silicon mask. LER variation is found to have no impact on resistivity. Wires with nearly bamboo grain structure appears to have a resistivity benefit, offering the potential of improved performance beyond the 7 nm node if the grain size can be controlled. ***(Paper T8-3, "Resistivity of copper interconnects beyond the 7 nm node," A. Pyzyna et al., IBM & GLOBALFOUNDRIES)***

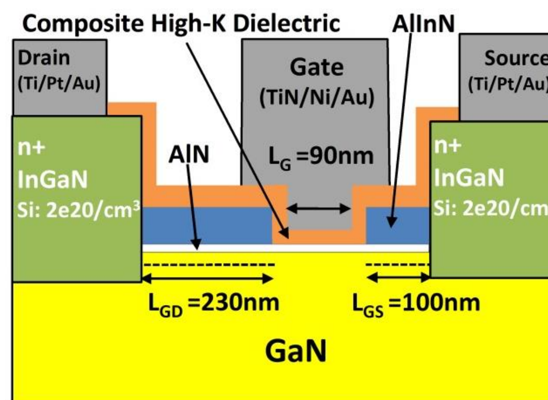


Cross-sectional TEM of trenches (a) as filled and (b) after CMP.
(c) SEM shows DSA patterned lines at 28nm pitch after CMP.

B) Emerging Device Technology

High-performance Low-Leakage Enhancement-Mode High-K Dielectric GaN MOS-HEMTs:

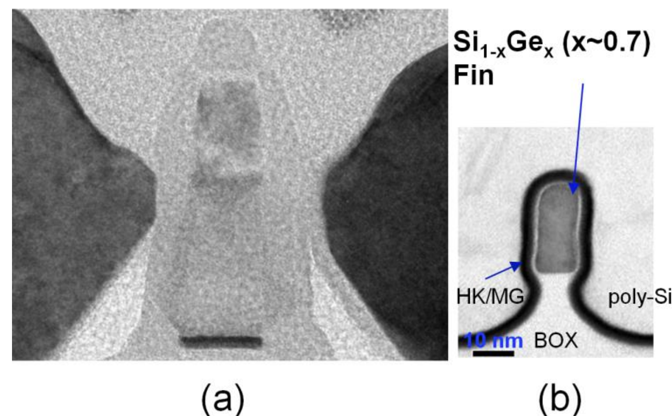
GaN devices have advantages on high power and high frequency applications. Those devices are mostly depletion-mode (normally-on) HEMTs, which are not suitable for low-power SoCs. In this paper, Intel demonstrated 90nm gate length high-K dielectric enhancement-mode (e-mode) GaN MOS-HEMT which shows low I_{OFF}=70nA/µm (V_D=3.5V, V_G=0V), low R_{ON}=490Ω-µm, high $I_{D,max}$=1.4mA/µm, and excellent power-added efficiency (PAE) of 80% at RF output power density (RF Pout) of 0.55W/mm (V_D=3.5V, f=2.0GHz). These results represent (i) >3.6X lower R_{ON} at equivalent breakdown voltage (BV_D) than industry-standard Si voltage regulator (VR) transistors, and (ii) >10% better PAE at matched RF Pout or >50% higher RF Pout at matched PAE than industry-standard GaAs RF power amplifier (PA) transistors, all at mobile SoC-compatible voltages. This work shows, for the first time, hat the application space of GaN electronics can be expanded beyond the existing high-voltage power and RF electronics (e.g. automobile, power conversion, base-station, radar) to include low-power mobile SoC applications. ***(Paper T15-1, "High-Performance Low-Leakage Enhancement-Mode High-K Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF Power Amplifiers for Low-Power Mobile SoCs," H.W. Then et al., Intel)***



Schematic of the e-mode high-k GaN MOS-HEMT of this work.

High-Mobility High-Ge-Content $Si_{1-x}Ge_x$-on-Insulator PMOS FinFETs:

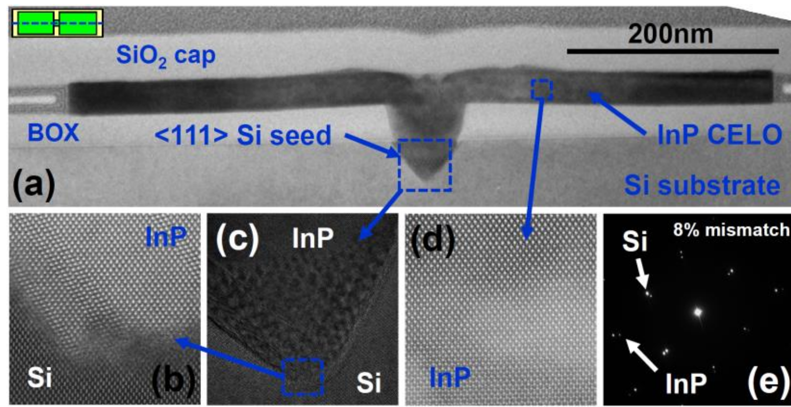
Higher strain in the channel (higher Ge content for pMOS) and thinner channel are preferable for the extremely scaled CMOS. IBM demonstrates scaled high-Ge-content (HGC) SiGe-OI FinFETs with Ge fraction up to 71%, using a CMOS-compatible approach. Aggressively scaled HGC relatively-tall fins with vertical sidewalls and sub-10 nm widths have been demonstrated using an enhanced 3D-Ge-condensation technique. An improved Si-cap-free high-k/metal-gate process featuring optimized interfacial layer has enabled scaled EOT (equivalent oxide thickness) of 0.85 nm, impressive long channel subthreshold swing (SS=69 mV/dec.) and enhancement-mode devices for Ge content ~0.6. Moreover, long-channel mobility characteristics (~300 cm^2/Vs at $N_{inv}=1x10^{13}cm^{-2}$) at the scaled EOT as well as short-channel pMOS FinFETs with good cut-off behavior are shown. ***(Paper T2-3, "High-Mobility High-Ge-Content $Si_{1-x}Ge_x$-OI PMOS FinFETs with Fins Formed Using 3D Germanium Condensation with Ge Fraction up to x~ 0.7, Scaled EOT~8.5A and ~10nm Fin Width," P. Hashemi et al., IBM)***



Typical cross-section TEM of $Si_{1-x}Ge_x$-OI (x~0.7) pMOS FinFETs (a) along and (b) across the fin direction.

CMOS-compatible Confined Epitaxial Lateral Overgrowth (CELO) to Integrate InGaAs-on-Insulator MOFETs on Large-Area Si Substrates:

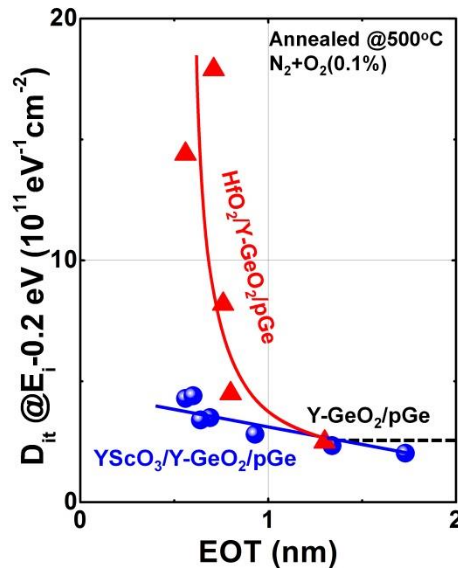
Cost effective integration of high-mobility III-V (InGaAs or others) semiconductor material on large-area silicon substrates is one of the most challenging issues. IBM and EMPA report the CMOS compatible integration of high-quality InGaAs on insulator (InGaAs-OI) on Si substrates by a novel concept named Confined Epitaxial Lateral Overgrowth (CELO). This method, based on the selective epitaxy, only requires the use of standard large-area silicon substrates and typical CMOS processes. It enables the fabrication of InGaAs-OI starting from both bulk and SOI Si wafers. The InGaAs epitaxial structures are characterized to be a very low defectivity, and can fulfill the requirements of both ultra-thin-body and fins-based transistor structures used in the advanced CMOS nodes. Gate-first self-aligned FinFETs (100-nm-long gate, 50-nm-wide fins and 250-nm-wide plug contacts) with excellent electrical characteristics, comparable to the state-of-the-art InGaAs MOSFETs on Si, are demonstrated. This new concept has a significant potential to introduce high-mobility channel materials into the high-volume manufacturing in the coming advanced CMOS nodes. ***(Paper T13-3, "Confined Epitaxial Lateral Overgrowth (CELO): A Novel Concept for Scalable Integration of CMOS-Compatible InGaAs-on-insulator MOSFETs on Large-Area Si Substrates," L. Czornomaz et al., IBM & EMPA)***



Material quality analysis with InP on Si by CELO. (a) Cross-sectional TEM. High number of defects is observed at the seed region by HR-STEM (b) / TEM (c) (mostly stacking faults). Away from the seed, a perfect lattice structure is observed with 8% mismatch to Si corresponding to fully relaxed InP (d and e).

Reliability-aware Ge Gate Stacks with 0.5nm EOT:

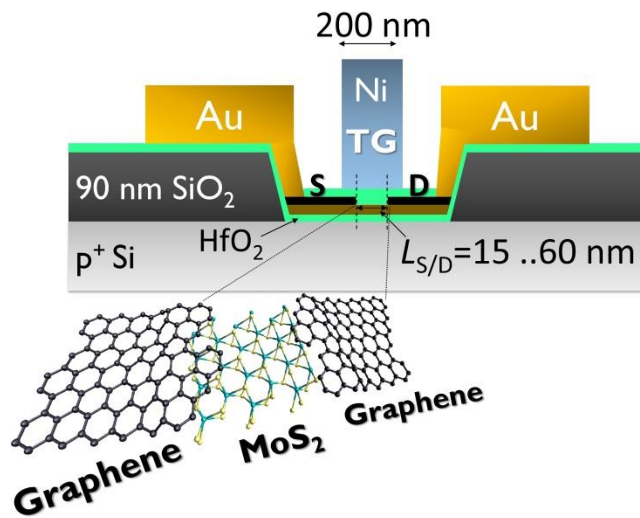
Low interface-state density, high carrier mobility in the channel and high reliability are significant issues of the gate-stack technology for the Ge MOSFETs. The University of Tokyo reports a novel material/process-based design for reliability-aware Ge gate stack. Initially good characteristics of the Ge gate stacks do not necessarily guarantee the long-term device reliability. To overcome this issue, the stability of GeO_2 network as well as the formation of new high-k has been investigated. A robust Ge gate stack with both 0.5 nm equivalent oxide thickness (EOT) and sufficiently low interface-state density (D_{it}) have been demonstrated. ***(Paper T2-4, "Design and Demonstration of Reliability-aware Ge Gate Stacks with 0.5 nm EOT," C. Lu et al., The University of Tokyo)***



D_{it} at E_i - 0.2 eV in $YScO_3$ and HfO_2 / Y-GeO_2 / Ge (111) stacks with various Y-GeO_2 interfacial-layer (IL) thicknesses. HfO_2 needs over 1 nm IL to block its destructive influence on Ge interface, while $YScO_3$ is free from this concern.

Record short channel length (15nm) MoS_2 FETs:

Atomically thin-films of layered semiconductors such as MoS_2 have great potential in device applications because of their ultra-thin body nature, large bandgap, thermal stability and compatibility with CMOS processes. MoS_2 FETs have an extremely low I_{off}, making them promising for low power applications. Massachusetts Institute of Technology (MIT) and others demonstrate single- and double-gated (SG & DG) field effect transistors (FETs) with a record source-drain length ($L_{S/D}$) of 15 nm built on monolayer (t_{ch}~0.7 nm) and 4-layer (t_{ch}~3 nm) MoS_2 channels using monolayer graphene as the Source/Drain contacts. The best devices, corresponding to DG 4-layer MoS_2-FETs with $L_{S/D}$=15 nm, had an I_{on}/I_{off} in excess of 10^6 and a minimum subthreshold swing ($SS_{min.}$) of 90 mV/dec. at V_{DS}=0.5 V. At $L_{S/D}$=1 μm and V_{DS}=0.5 V, $SS_{min.}$=66 mV/dec., which is the best SS reported in MoS_2 FETs, indicating the high quality of the interface and the enhanced channel electrostatics. ***(Paper T3-4, "15-nm Channel Length MoS_2 FETs with Single- and Double-Gate structures," A. Nourbakhsh et al., Massachusetts Institute of Technology, imec & KULeuven)***

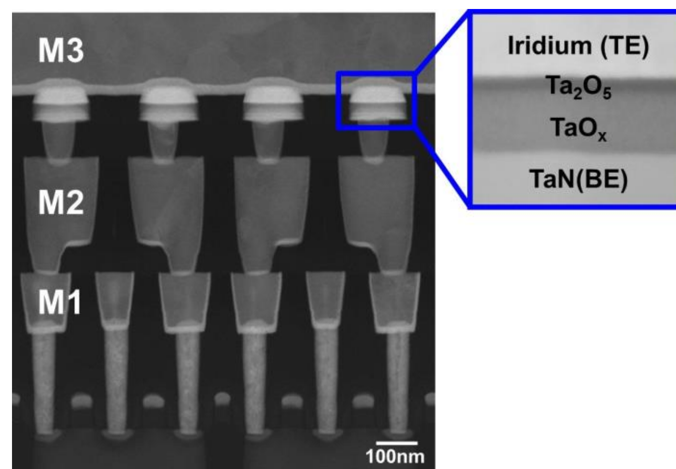


Device schematic cross-section of the short channel SG & DG-MoS_2 FETs with graphene S/D contacts.

C) Emerging Nonvolatile Memory Technology

Highly Reliable TaO_x ReRAM with Centralized Filament for 28-nm Embedded Application:

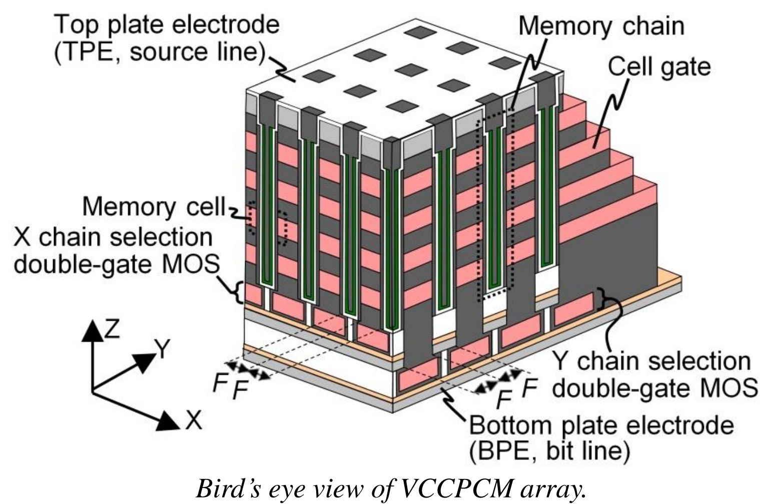
Oxide-based ReRAM has major potential as non-volatile memory. The concern is that the filament of the cell becomes highly susceptible to the influence of the cell edge and the environment around the cell during formation process. For 28-nm embedded application, Panasonic and imec have proposed a TaO_x-based ReRAM with precise filament positioning and high thermal stability. The cell was realized using several newly-developed process technologies and cell structures: low-damage etching, cell side oxidation and encapsulated cell structure. As a result, they succeeded for the first time in forming a filament at the cell center. In addition, they confirmed the feasibility of 20-nm cell size. Using the proposed filament control and thermal stability technologies, very good reliability was achieved in 2-Mbit ReRAM: 100k cycles and 10 years' retention at 85 °C was demonstrated. ***(Paper T2-2, "Highly reliable TaO_x ReRAM with centralized filament for 28-nm embedded application," Y. Hayakawa et al., Panasonic & imec)***



Cross-sectional TEM of Ir (top electrode)/TaO_x/TaN (bottom electrode) ReRAM.

3D Vertical Chain-cell-type Phase-Change-Memory Array for Low Bit Cost and High Programming Throughput:

SSD storage system requires nonvolatile storage memories with both low bit cost and high programming throughput. Hitachi reveals a high-programming-throughput three-dimensional (3D) vertical chain-cell-type phase-change memory (VCCPCM) array for a next-generation storage device. To increase the number of write cells at one time by reducing resistance of bit and source lines, the VCCPCM array includes plate electrodes and double-gate vertical-chain-selection MOSs with 5-nm-thick poly-Si channels. In addition, CO_2 laser annealing enhances the drivability of a poly-Si cell MOS to 680 μA/μm to suppress energy loss in the cell MOS. Erase throughput is improved by "bundle erase" operation, which erases memory cells in a bundle by channel heating. ***(Paper T7-1, "2.8-GB/s-write and 670-MB/s-erase operations of a 3D vertical chain-cell-type phase-change-memory array," K. Kurotsuchi et al., Hitachi)***

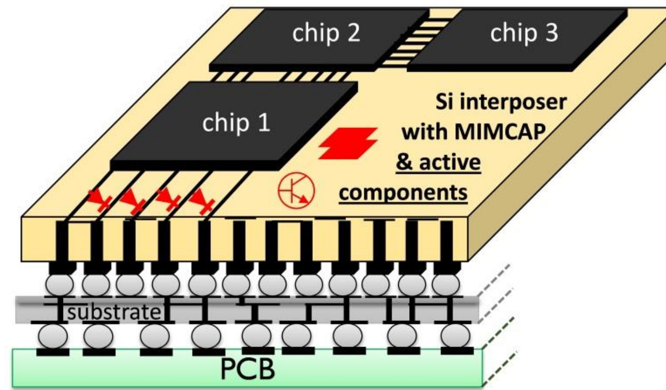


Bird's eye view of VCCPCM array.

D) Design/Technology Co-Optimization & 3D integration

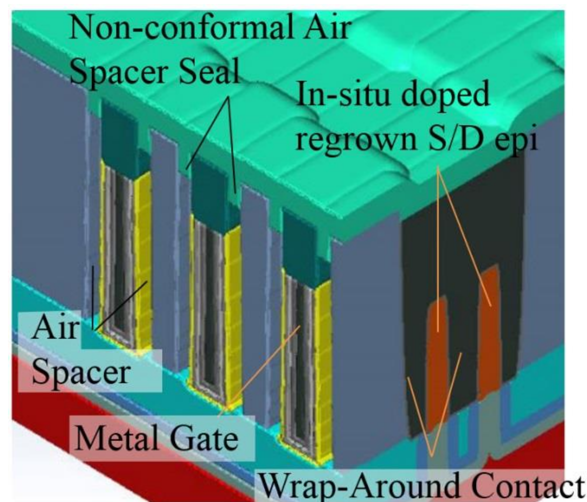
Active-Lite Interposer for 2.5 & 3D Integration:

Adding functionality to a passive Si interposer used in 2.5/3D integration, can result in system cost reductions. Imec integrated active components (diodes, BJTs, SCR (silicon-controlled rectifier), etc.) on Si interposer using a new low-mask process flow. This low-cost process enables: (1) to move part of the area hungry ESD protection from the stacked dies to the interposer; (2) the realization of pre-bond testable interposers (DFT); and (3) components for analog circuits. These features result in large system cost savings, especially on large interposers with many I/O. ***(Paper JFS4-1, "Active-Lite Interposer for 2.5 & 3D Integration," G. Hellings et al., imec)***



Schematic view of an active-lite interposer with TSV, MIMCAP and active components.

Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC:
Qualcomm systematically investigated the impact of R and C scaling to 7nm node by accounting for FEOL and BEOL holistically. Speed-power performance of plainly scaled 7 nm node CMOS turns out to be degraded compared to previous node. BEOL wire resistance (Rwire) multiplied by logic gate input pin cap (Cpin), Rwire×Cpin, is identified as a major limiter of performance and power at 7 nm node. Reducing Cpin is crucial to mitigate abruptly rising BEOL Rwire effect. Depopulation of fin is one of most effective methods to reduce Cpin, and scale the logic gate area. Air Spacer (AS) on transistor sidewall further reduces Cpin. Careful choice of routing metal stack ameliorates adverse effect of Rwire. Wrap-Around-Contact (WAC) over Source and Drain of scaled fin pitch (Pfin) is needed to reduce transistor resistance (Rtr). Fin depopulation with other cost effective process innovations significantly improve Power-Performance-Area-Cost (PPAC) of 7nm node, enabling continued scaling of mobile SoC. ***(Paper JFS3-4, "Holistic Technology Optimization and Key Enablers for 7nm Mobile SoC," S. C. Song et al., Qualcomm)***

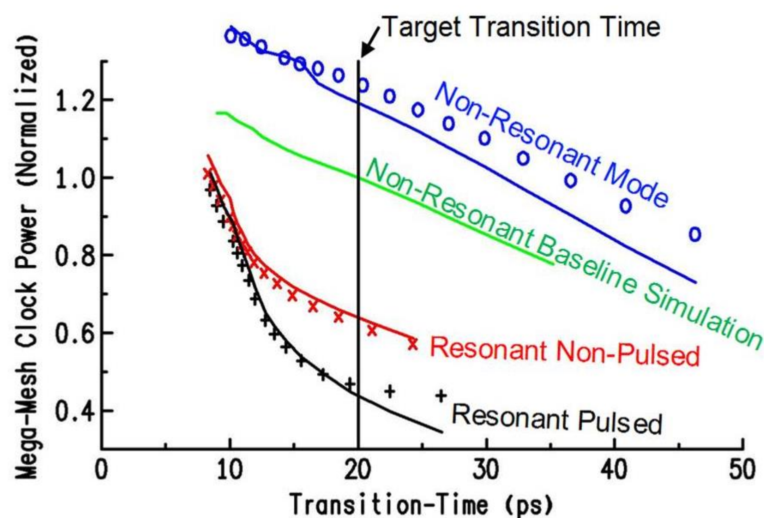


3D Cross-sectional image of proposed 7nm transistors incorporating WAC and AS.

II) Technical Highlights from 2015 Symposium on VLSI Circuits

A) High-performance processors

Low-Power and High-Speed Clock Distribution for Microprocessors:
A large resonant “mega-mesh” global clock distribution is proposed for the IBM z13 microprocessor. Improved two-layer inductors, one resonant mode, new pulsed-mode sector buffers, and higher resonant frequency contribute to saving 50% of the final-stage clock mesh power and 8% of the total chip power in the desired frequency range of 4.5 to 5.5 GHz, as compared to a simulated, non-resonant baseline. Resonant clock power savings allows the implementation of a mega-mesh, resulting in significant advantages in bus bandwidth and chip timing with little power impact. The design is implemented in IBM’s high-performance 22nm high-k CMOS SOI technology with 17 metal layers. (***Paper C23-5, ”Resonant Clock Mega-Mesh for the IBM z13,” David Shan et al., IBM***)



Comparison of mega-mesh power across operational modes

Highly Energy-Efficient Processor for Mobile Devices:
Intel Core™ M and 5th generation of Core™ processors (code named Broadwell) are fabricated on a 14 nm process technology node resulting in a 49% reduction in feature-neutral die area. Techniques and optimizations were implemented to deliver 2.5x total die power (TDP) reduction coupled with up-to 60% higher graphics performance. Broadwell introduces the second generation of Fully Integrated Voltage Regulator with better droop control and parallel boot linear voltage regulator (LVR) along with other power-reduction features resulting in 35% reduction in active and standby power over first generation. 3DL inductor technology introduced for the first time in Broadwell, enables 30 % reduction in package thickness and improved low-load efficiency. IO re-partitioning of the SOC and a major re-design of DDR system resulted in 30% reduction in I/O power. Shutting down various parts of the SOC die in various idle states (C* states) resulted in 60% reduction in the idle power. New software controlled co-optimization methods were implemented such as duty-cycle control and dynamic display support to improve the energy efficiency of the graphics and the display subsystem. The Symposia features other papers from Intel with the same 14nm platform: paper number C19-1 in circuits and T2-1 in technology: refer to technology tip sheet. (***Paper C23-1, ”Broadwell : A family of IA 14nm processors,” A. Nalamalpu et al., Intel Corporation. See also Papers T2-1, “A 14 nm SoC Platform Technology Featuring 2nd Generation Tri-Gate Transistors, 70 nm Gate Pitch, 52 nm Metal Pitch,” C.-H. Jan et al., Intel, and 19-1,***

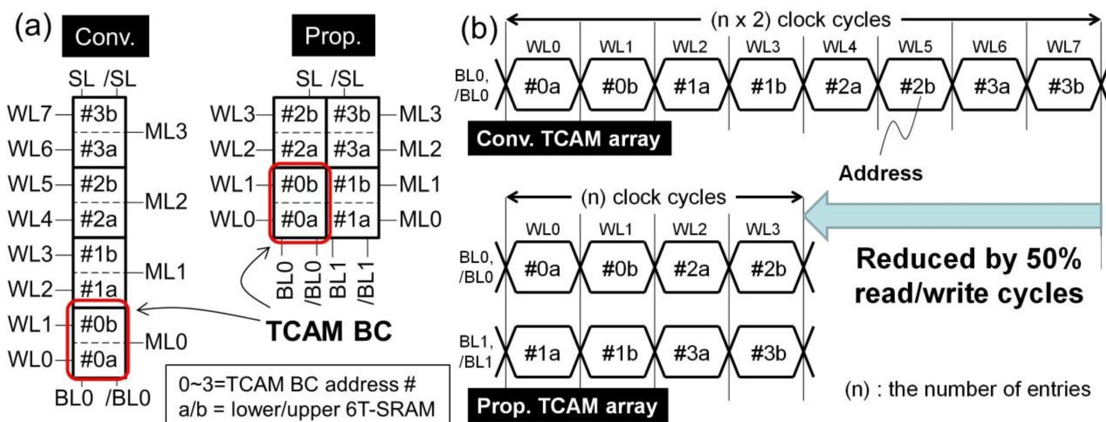
“A 0.0499 um2 High Density and Aging Resilient 8T SRAM with 14nm FinFET Technology Featuring 560mV VMIN with Read and Write Assist,” Y-H. Koo, et al., Intel.)

Broadwell die map

B) High-performance memory systems

16nm Highest Bit Density and Fastest Search Speed TCAM:

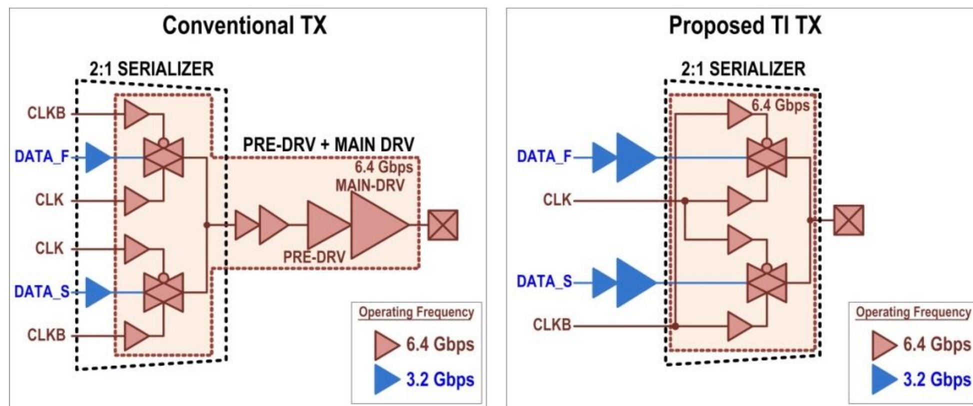
A new 16 nm Fin-FET bit-cell (BC) for ternary content-addressable memory (TCAM) is proposed. The proposed BC is 15.8% smaller than the conventional BC. A 10kb TCAM macro achieves the highest density of 1.8 Mbit/mm^2. Measurement shows that total active power in the proposed macro is 8% less than that in the conventional one. A 484 ps of search access time is observed at 0.8 V, which marks the world’s fastest operation cycle of 1.25 G search per second.. ***(Paper C19-5 , “1.8 Mbit/mm2 Ternary-CAM macro with 484 ps Search Access Time in 16 nm Fin-FET Bulk CMOS Technology “, Y. Tsukamoto, et al., Renesas Electronics Corporation)***



Bit-cell schematic, array, and cycle time reduction

High speed DRAM interfaces:

A paper by Chang-Kyo Lee, et al., from Samsung Electronics will describe a 6.4 Gb/s TX-interleaving technique at sub-1V supply voltage. It is implemented with 25nm DRAM process for the future mobile DRAM interface which requires 51.2 GB/s which is 2X bandwidth of LPDDR4. A proposed 2-channel TX interleaving technique with a bootstrapping switch can save power consumption drastically by eliminating repeaters, while operating at 6.4 Gb/s with 40% enhancement of I/O power efficiency compared to LPDDR4. ***(Paper C12-2 “A 6.4Gb/s/pin at Sub-1V Supply Voltage TX-interleaving Technique for Mobile DRAM Interface”, C-K. Kee, et al., Samsung Electronics)***

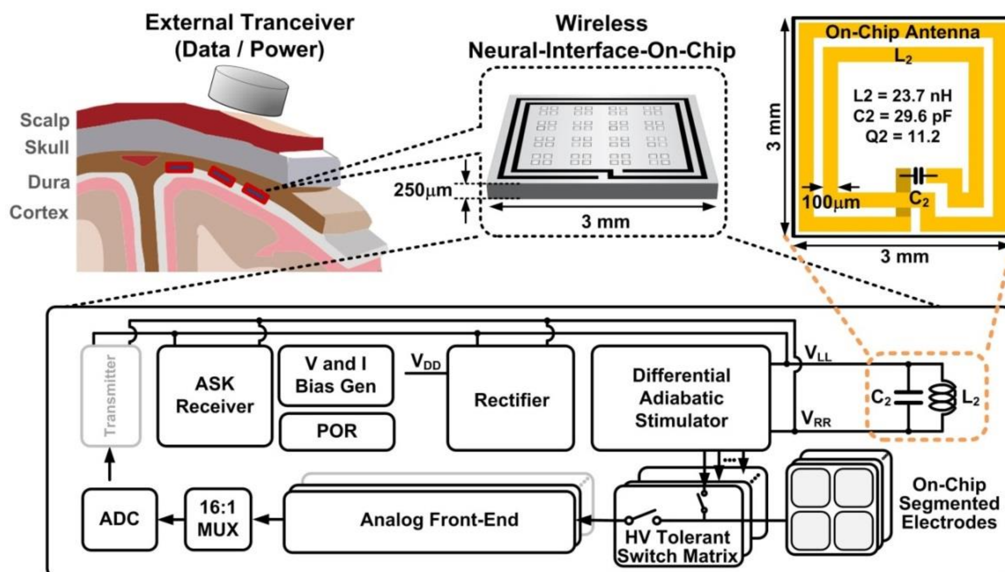


Comparison of the conventional to the proposed interleaved TX

C) Biomedical and sensors

A 16-Channel Wireless Neural Interfacing SoC:

The paper by S. Ha, et al., from University of California, San Diego, USA presents a fully-integrated 16-channel wireless neural interfacing SoC that employs an adiabatic stimulator powered directly from a 190-MHz on-chip antenna to eliminate bulky external components while simultaneously avoiding rectifier and regulator losses. Using a charge replenishing architecture, the stimulator outputs up to 145-uA, while achieving a 63.1% replenishing ratio and a stimulation efficiency factor of 6.0. Fabricated in a 0.18um CMOS-SOI process, this chip was validated for stimulation and recording under *in vivo* physiological conditions. ***(Paper C6-1: "A 16-Channel Wireless Neural Interfacing SoC with RF-Powered Energy-Replenishing Adiabatic Stimulation, S. Ha et al., UCSD)***

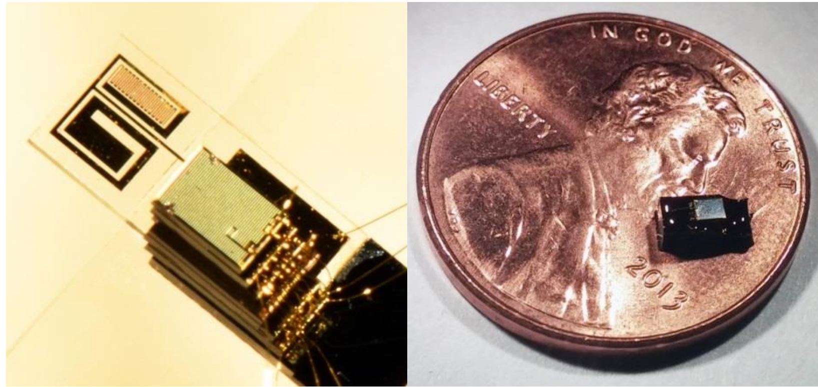


Concept and block diagram of wireless neural interface

A Self-Powered Wireless Sensor Node with 8GHz UWB Transmitter:

The paper by Hyeongseok Kim, et al., from the University of Michigan presents a complete, autonomous, wireless temperature sensor, fully encapsulated in a 10.6mm3 volume. This sensor module includes solar energy harvesting with an integrated 2uAh battery, optical receiver for

programming, microcontroller and memory, 8GHz UWB transmitter, and miniaturized custom antennas with a wireless range of 7 meters. It is the first time to demonstrate full and stand-alone wireless sensing functionality with such a tiny integrated system. ***(C13-2: "A 10.6mm3 Full-Integrated, Wireless Sensor Node with 8GHz UWB Transmitter", Hyeongseok Kim et al., University of Michigan)***

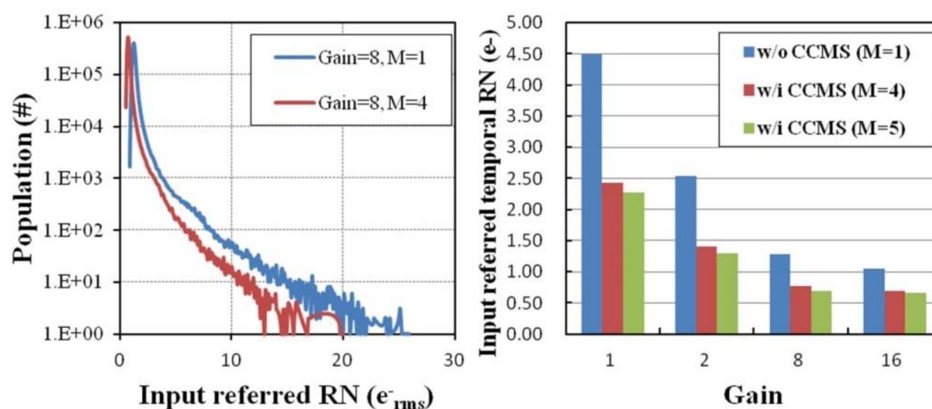


Proposed encapsulated stack system

D) 3D stacked image sensors

A 3D stacked CMOS Image Sensor with a low noise technique:

The paper by Shang-Fu Yeh, et al., of TSMC will describe an 8Mpixel 3D-stacked low noise CMOS image sensor with Conditional Correlated Multiple Sampling (CCMS) technique. This technique is proposed to solve the low frame rate issue by using multiple small-range voltage ramps. A 0.66e-rms input referred temporal readout noise is obtained with a 5-times CCMS technique, and also both thermal noise and the random telegraph signal (RTS) noise can be reduced by using CCMS technique. ***(Paper C4-2,"A 0.66e-rms Temporal-Readout-Noise 3D-Stacked CMOS Image Sensor with Conditional Correlated Multiple Sampling (CCMS) Technique," Shang-Fu Yeh et al., TSMC)***



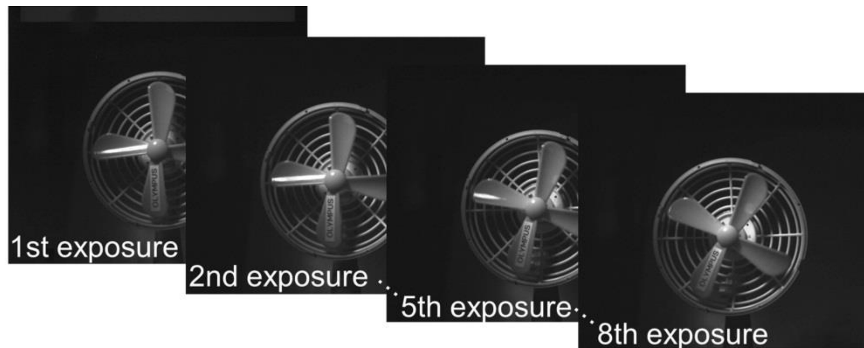
Improvement of noise with CCMS technique

A 3D stacked CMOS Image Sensor with Global-shutter mode and high speed capturing mode:

The paper by Toru Kondo et al. from Olympus Corp. will describe a 16Mpixel 3D stacked CMOS image sensor with pixel level interconnections using 4 million micro bumps.

The two semiconductor substrates are bonded by a 7.6um pitch micro-bump array, and the

storage node array is comprised on the bottom substrate to improve parasitic light sensitivity (PLS). Both a 16Mpixel global-shutter mode with a -180dB PLS and 2Mpixel 10000fps high speed image capturing are achieved. ***(Paper C4-5, "A 3D stacked CMOS image sensor with 16Mpixel global-shutter mode and 2Mpixel 10000fps mode using 4 million interconnections," Toru Kondo et al., Olympus Corp.)***

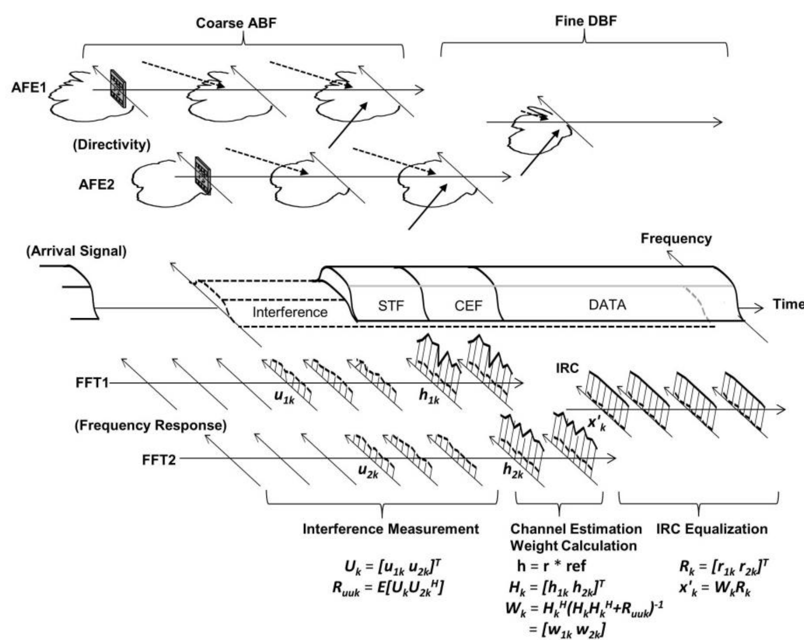


Sample images at 10000fps high speed image capturing mode

E) Interference Suppressing mm-Wave Transceiver

WiGig Transceiver:

The paper by Takinami, et al., from Panasonic describes a 60GHz radio that is targeting WiGig/IEEE 802.11ad standard. For the use in dense small cell networks for mobile data offloading, a hybrid analog/digital beamforming with packet-by-packet adaptive interference suppression is introduced. The transceiver consists of two-stream analog front-ends (AFEs) with four–element phased array antenna. The proposed interference suppression scheme demonstrates 3.1dB EVM advantage compared with conventional method. ***(Paper C22-3,"A 60GHz Wireless Transceiver Employing Hybrid Analog/Digital Beamforming with Interference Suppression for Multiuser Gigabit/s Radio Access," K. Takinami et al., Panasonic)***

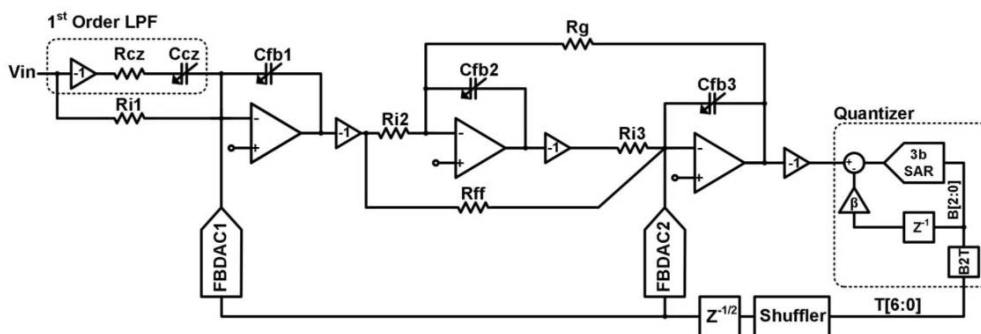


Operation of the RX across frequency and time domains

F) High-performance ADC

Continuous-time delta-sigma ADC:

A paper by G. Wei, et al., from Broadcom will describe a multi-bit continuous-time delta-sigma modulator with a novel SAR (successive approximation register) quantizer. The SAR quantizer realizes an embedded excess-loop-delay compensation with negligible power and area overhead.. Implemented in 28nm CMOS technology, the modulator features 13-ENOB over 5MHz bandwidth with FoMs (figure-of-merits) of 36.4fJ/conv.-step and 175.9dB. A notable SFDR of 94dB, achieved by digital correction of digital-to-analog converter (DAC) non-linearity, is also demonstrated. ***(Paper C21-2,"A 13-ENOB, 5 MHz BW, 3.16 mW Multi-Bit Continuous-Time Delta-Sigma ADC in 28 nm CMOS with Excess-Loop-Delay Compensation Embedded in SAR Quantizer," G. Wei et al., Broadcom)***

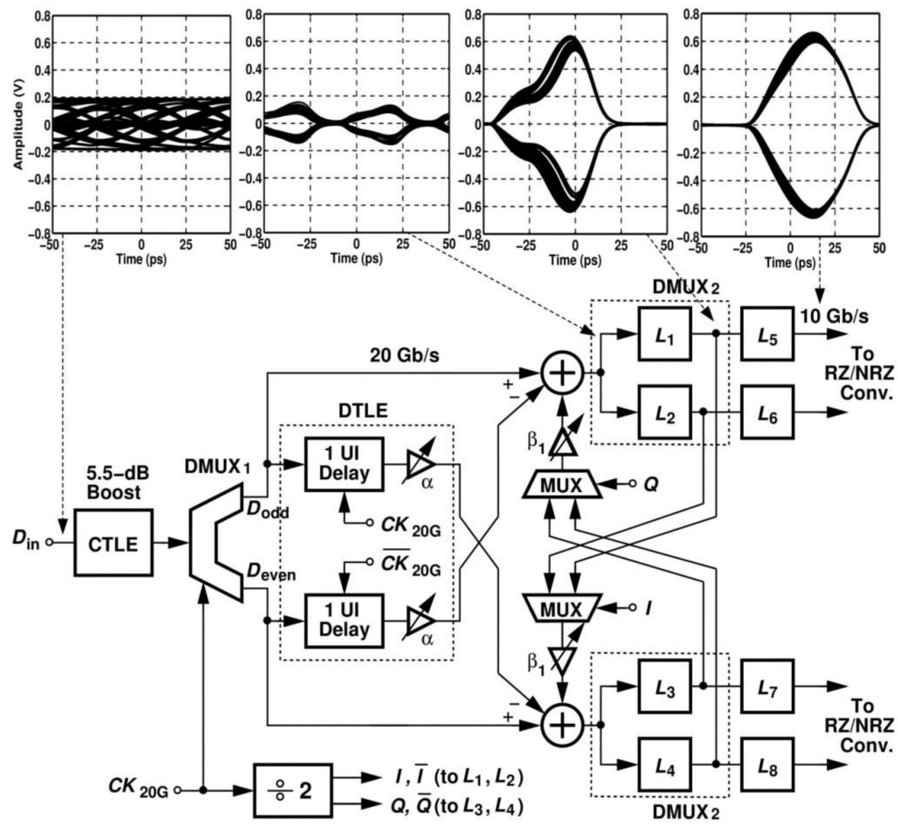


ADC architecture

G) High-speed wireline receiver

40Gb/s equalizer with a power consumption of 9.2mW in 45nm CMOS process:

In the Ultra-High-Speed Receiver session, A. Manian and Prof. B. Razavi of UCLA will present a 40Gb/s CMOS equalizer with outstanding power consumption of 9.2mW designed for highly integrated I/O's in wavelength division multiplexing (WDM) systems. The equalizer employs a 1-stage CTLE with a 2-tap half-rate/quarter-rate DFE and a novel 1-tap discrete-time linear equalizer (DTLE) to relax the CTLE boost gain requirement, significantly reducing power consumption. Charge-steering logics are utilized to meet the ultra-high-speed requirement with good energy efficiency. Implemented in 45nm CMOS, the equalizer can compensate a channel loss of 20dB at Nyquist for error free operation. ***(Paper C15-2," A 40-Gb/s 9.2-mW CMOS Equalizer," A. Manian et al., UCLA)***



Equalizer architecture

Here are definitions of some important technical terms:

- **ADC, or Analog-to-Digital Converter** – A device that converts a continuous physical quantity (usually voltage) to a digital number.
- **Back-End/BEOL** and **Front-End/FEOL** -- In integrated circuit manufacturing, transistors and other active devices are built first (at the front end of the manufacturing line or FEOL), while the interconnect, or the wiring, is built afterward, at the "back end" of the manufacturing line (BEOL).
- **CMOS/MOS/MOSFET/FET**-- Most transistors today are FETs, or field-effect transistors. Most FETs are built with CMOS manufacturing technology (complementary metal oxide semiconductor). Generically they are called MOSFETs, or sometimes MOS transistors.
- **Compound/III-V Semiconductors** -- Most semiconductors are silicon-based, but researchers continue to investigate other semiconducting materials with higher electron mobilities because they can be used to make faster devices. The tradeoff is that the materials are harder to work with than silicon. Compound semiconductors are made of two or more elements (e.g. GaAs, InP, GaN, etc.) which are generally found in groups III and V of the periodic table of the elements.
- **DAC or Digital-to Analog Converter –** A device that converts digital data into an analog signal (current, voltage, or electric charge).
- **Droop Control –** Droop is a reduction in the power supply voltage drop usually due to a change in the operating state of the system (e.g., going from a low activity to a high activity mode). Droop control is a mechanism to compensate for this voltage drop, increasing timing margins and potentially reducing the number of decoupling capacitors.
- **DRAM** – Dynamic random access memory stores information as charge on a capacitor that must be periodically refreshed. Dedicated DRAM chips form the bulk of the main memory for typical computers, tablets, and smartphones.
- **EOT or equivalent oxide thickness** – A distance to compare performance of high-k dielectrics with that of SiO_2 film. A SiO2 film with the thickness of EOT has the same gate capacitance with the high-k material that is used. The higher k dielectrics can reduce EOT, which enhances the MOSFET performance.
- **Equalizer (CTLE/DTLE/DFE)** – Equalizers are used in wireline communication to compensate for the variable attenuation across frequency for typical copper interconnects. Continuous time linear equalizers (CTLE) and discrete-time linear equalizers (DTLE) use a linear filter that generally increases the high frequency content of the signal. A decision feedback equalizer (DFE) is a nonlinear process that corrects the level of a received signal based off of previously decided bits.
- **ESD** – Electrostatic discharge. A sudden release of static electricity between two object caused by contact. If the ESD hits the integrated circuit, it may cause the device to fail or reduce the lifetime.
- **FD-SOI** -- Fully depleted silicon on insulator is a process technology option that can offer speed and power advantages over conventional bulk silicon transistors.
- **FinFET** -- A transistor whose 3-D shape resembles a fin, usually with multiple gates surrounding it for better on/off switching control.
- **Front-End/FEOL and Back-End/BEOL** -- In integrated circuit manufacturing, transistors and other active devices are built first (at the front end of the manufacturing line or FEOL), while the interconnect, or the wiring, is built afterward, at the "back end" of the manufacturing line (BEOL).
- **HEMT** – High Electron Mobility Transistor, also known as heterostructure FET (HFET) or modulation-doped FET (MODFET). A HEMT is based on a heterojunction which consists of two semiconductors with different band gaps (see also Compound/III-V Semiconductors). By choosing proper materials, the band discontinuity forms high-mobility two-dimensional electron gas at the hetero interface.
- **HKMG, or High-k Dielectrics/Metal Gates** -- A dielectric is an electrical insulator. "k" is the relative permittivity and is a measure of how well a material will prevent current flow between the gate electrode and the channel region of a field-effect transistor, while capacitively coupling the two to control on/off switching. In future CMOS integrated circuits (chips) the gate dielectric will need to provide capacitive coupling equivalent to that of a silicon-dioxide layer that is just a few atoms thick, to allow the length of the channel region to be scaled down to 10 nm and below. Metal gate materials are more compatible with high-k gate dielectrics than are traditional doped polycrystalline silicon material. Much progress has been made in recent years to integrate metal gates into the CMOS process flow for the manufacture of high-performance chips.

- **III-V** -- see Compound/III-V Semiconductors
- **Integrated Circuit** -- An electrical circuit comprising many interconnected elements (e.g. transistors, diodes, capacitors, resistors, inductors) built on a semiconducting substrate.
- **Interconnect** -- The metal lines, or wiring, connecting transistors and other circuit elements. See **Back-End/BEOL**.
- **Interposer** – An electrical interface between chips or between socket and chips. The purpose of an interposer is to connect chips and sockets with different I/O terminals.
- **Linear Voltage Regulator** – Maintain a steady voltage by changing output resistance according to load current. It requires a higher input voltage than output voltage and normally results in lower efficiency than a switching regulator.
- **Low-k Dielectrics/Interconnect** -- Interconnect refers to the metal wires that connect elements together in an integrated circuit (chip). The close proximity of adjacent wires can result in capacitance that can limit chip performance. A low-k dielectric electrically insulates the copper lines while minimizing their mutual capacitance; however, these materials are generally more fragile and thus pose challenges for manufacturing.
- **MEMS** -- A micro-electro-mechanical system, containing micrometer-scale moving parts.
- **N-FET/P-FET or NMOS/PMOS** -- MOSFETs come in two varieties (n-channel or p-channel) which operate in a complementary fashion.
- **Non-volatile memory (NVM)** – A type of computer memory that retains its stored information even when the power is off.
- **Phase-Change Memory/PCM** -- Phase-change materials have crystalline and non-crystalline states which are used to represent the digits “0” or “1” in computer non-volatile memory. Electrical current is used to toggle between the two states – heat from the current causes the material to change its state.
- **ReRAM or RRAM** – Resistive random-access memory. A non-volatile random access memory that stores the binary digit by changing the resistivity of material between electrodes.
- **Scaling/Density/Integration** -- Scaling is making transistors and other circuit elements smaller so that more of them will fit on a chip. A denser chip contains more transistors in a given area. Integration is combining circuit elements on a chip to add more functions to achieve lower cost per function.
- **Semiconductor** -- A material that can be made to conduct or to block the passage of electrical current, giving the ability to store and process information.
- **SoC** -- A system-on-a-chip. An integrated circuit which integrates all necessary components of a computer or other electronic system on a single chip.
- **SOI** -- A silicon-on-insulator substrate, used to reduce parasitic capacitance and thereby improve integrated circuit performance
- **Strained silicon & SiGe stressors** -- Silicon is said to be “strained” when its atoms are pulled farther apart or closer together than normal. Doing so alters the ease with which electrons flow through the silicon, enabling transistors built with it to operate faster and /or at lower voltage. The external stressors which impart strain are materials with slightly different atomic spacing than silicon. For example, a common way to compressively strain the channel region of a p-channel silicon field-effect transistor is to embed silicon-germanium (SiGe), which has larger atomic spacing than does Si, in its source and drain regions.
- **SRAM** -- A type of computer memory (static random access memory) that uses six or more transistors to store each bit of information. It can be written to and read from very quickly.
- **STT-MRAM** – Spin torque transfer magnetic random access memory is an emerging type of non-volatile memory that operates according to the “spin” state of electrons, not their electric charge. STT-MRAMs can be made extremely small.
- **TDC, or Time-to-Digital Converter** – A device for recognizing events and providing a digital representation of the time they occurred.
- **Ternary content-addressable memory (TCAM) –** Content-addressable memory is a specialized memory capable of searching a word in the entire contents. “Ternary” refers to capability of storing and querying “X” don’t care, in addition to 0 and 1.
- **UWB** – Ultra-wideband radio is wireless communication that operates in the 3.1-10.6 GHz band using a minimum of 500MHz of bandwidth, typically with very low average radiated power density.
- **Global shutter –** Method of capturing entire scene at single instant in time, rather than by scanning across the scene, like rolling shutter.

- **Effective Number of Bits (ENOB) –** Measure of the dynamic performance of ADCs, including noise and distortion effect, normalized to the performance of an otherwise ideal ADC with finite resolution.
- **Transistor** -- A tiny electrical switch that serves as the building block for integrated circuits. It has no moving parts and is made with a semiconductor material, usually silicon. Transistors can be ganged together by the billions on chips and programmed to receive, process and store information, and to output information and/or control signals.

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