2016 VLSI Circuits Short Course Program
Honolulu I

Advanced Wireline Techniques

Tuesday, June 14, 10:30 a.m.

Organizers: Afshin Momtaz, Broadcom Corporation
Patrick Yue, Hong Kong University of Science and Technology

10:30 a.m. **Introduction**

10:40 a.m. **28-56Gb/s Standards and Design Implications,** Frank O'Mahony, Intel

11:30 a.m. **Low Power CMOS Transceivers for 28Gb/s Serial Links and Future Prospects,** Mounir Meghelli, IBM

12:20 p.m. **Lunch**

1:30 p.m. **ADCs for PAM-X / QAM-X Backplane and Optical Data Links,** Aaron Buchwald, Inphi

2:20 p.m. **56Gb/s Analog Based NRZ Electrical Transceiver,** Hisakatsu Yamaguchi, Fujitsu Labs

3:10 p.m. **Break**

3:25 p.m. **Silicon Photonic Transceivers for Short-Reach Optical Interconnects,** Joris Van Campenhout, IMEC

4:15 p.m. **Integrated Electronic-Photonic Communication Circuits,** Vladimir Stojanovic, University of California, Berkeley

5:05 p.m. **Closing Remarks**

2016 VLSI Circuits Short Course Program
Honolulu II

Circuit Design in FinFET, FDSOI, and Advanced Memory Technologies

Tuesday, June 14, 10:30 a.m.

Organizers: Steve Dillen, Qualcomm Technologies, Inc.
Jonathan Chang, TSMC

10:30 a.m. **Introduction**

10:40 a.m. **How the FinFET is Changing Processor Design,** Jim Dodrill, ARM

11:30 a.m. **Embedded Memory Design in CMOS FinFET Technology,** Yih Wang, Intel

12:20 p.m. **Lunch**

1:30 p.m. **Migrating Analog/Mixed-Signal Designs to FinFET,** Alvin Loke, Qualcomm

2:20 p.m. **High Performance and High Reliability 3D Vertical NAND Flash,** Woopyo Jeong, Samsung

3:10 p.m. **Break**

3:25 p.m. **SRAM and Digital Logic in UTBB FDSOI,** Bora Nikolic, University of California, Berkeley

4:15 p.m. **FD-SOI Technology, Advantages for Analog/RF and Mixed-Signal Designs,** Andreia Cathelin, STMicroelectronics

5:05 p.m. **Closing Remarks**

Session 1 – TAPA II
Plenary Session

Wednesday, June 15, 8:05 a.m.
Chairs: G. Lehmann, Infineon Technologies
M. Ikeda, The University of Tokyo

8:05 a.m. **Welcome and Opening Remarks**
J. Gealow, Analog Devices
M. Motomura, Hokkaido University

1.1 – 8:35 a.m.
"Enabling Future Progress in Machine-Learning" (Invited), Olivier Temam, Google Inc.

1.2 – 9:20 a.m.
Accelerating the Sensing World through Imaging Evolution (Invited), Tetsuo Nomoto, Vice President and Senior General Manager, SONY

Session 2 – Tapa I
Memory Design

Wednesday, June 15
Chairpersons: J. Wuu, AMD
H. Yamauchi, Fukuoka Institute of Technology

2.1 - 10:15 a.m.
A 16nm Dual-Port SRAM with Partial Suppressed Word-line, Dummy Read Recovery and Negative Bit-line Circuitries for Low V_{MIN} Applications, Y.-H. Chen, K.-C. Lin, C.-W. Wu, W.-M. Chan, J.-J. Liaw, H.-J. Liao, J. Chang, TSMC

2.2 - 10:40 a.m.
A 6.05-Mb/mm^2 16-nm FinFET Double Pumping 1W1R 2-port SRAM with 313 ps Read Access Time, M. Yabuuchi, Y. Sawada, T. Sano*, Y. Ishii, S. Tanaka, M. Tanaka*, K. Nii, Renesas Electronics Corp., *Renesas System Design Corp.

2.3 - 11:05 a.m.
A 2x Logic Density Programmable Logic Array using Atom Switch Fully Implemented with Logic Transistors at 40nm-node and beyond, Y. Tsuji, X. Bai, A. Morioka, M. Miyamura, R. Nebashi, T. Sakamoto, M. Tada, N. Banno, K. Okamoto, N. Iguchi, H. Hada, T. Sugibayashi, NEC Corporation

2.4 - 11:30 a.m.
80Kb 10ns Read Cycle Logic Embedded High-K Charge Trap Multi-Time-Programmable Memory Scalable to 14nm FIN with no Added Process Complexity, J. Viraraghavan, D. Leu, B. Jayaraman, A. Cestero, R. Kilker*, M. Yin, J. Golz, R. R. Tummuru, R. Raghavan, D. Moy, T. Kempanna, F. Khan, T. Kirihata, S. Iyer** GLOBALFOUNDRIES, *IBM , **UCLA

Session 3 – Honolulu Suite

Oversampling Data Converters

Wednesday, June 15
Chairpersons: Y. Chiu, University of Texas at Dallas
Y.-S. Shu, Mediatek, Inc.

3.1 - 10:15 a.m.
A 97.99 dB SNDR, 2 kHz BW, 37.1 µW Noise-Shaping SAR ADC with Dynamic Element Matching and Modulation Dither Effect, K. Obata, K. Matsukawa, T. Miki, Y. Tsukamoto, K. Sushihara, Panasonic Corporation

3.2 - 10:40 a.m.
A 35µW 96.8dB SNDR 1 kHz BW Multi-Step Incremental ADC Using Multi-Slope Extended Counting with a Single Integrator, Y. Zhang, C. -H. Chen, T. He, G. Temes, Oregon State University

3.3 - 11:05 a.m.
A 18.5-fJ/step VCO-Based 0-1 MASH ΔΣ ADC with Digital Background Calibration, A. Sanyal, N. Sun, The University of Texas at Austin

3.4 - 11:30 a.m.
A 13.3mW 60MHz Bandwidth, 76dB DR 6GS/s CTΔΣ M with Time Interleaved FIR Feedback, A.Jain, S.Pavan, IIT

Session 4 – Tapa I
Biomedical SOCs

Wednesday, June 15
Chairpersons: N. Verma, Princeton University
J. Ohta, Nara Institute of Science and Technology

4.1 - 1:15 p.m.
A 128-Channel Spike Sorting Processor Featuring 0.175 µW and 0.0033 mm^2 per Channel in 65-nm CMOS, S. Mohammad Ali Zeinolabedin, A. T. Do*, D. Jeon**, D. Sylvester***, T.-H. Kim, Nanyang Technological University, *Institute of Microelectronics, **Seoul National University, ***University of Michigan, Ann Arbor

4.2 - 1:40 p.m.
1.74-µW/ch, 95.3%-Accurate Spike-Sorting Hardware based on Bayesian Decision, Z. Jiang, J. Cerqueira, S. Kim, Q. Wang, M. Seok, Columbia University

4.3 - 2:05 p.m.
An High-Density CMOS Multi-Modality Joint Sensor/Stimulator Array with 1024 Pixels for Holistic Real-Time Cellular Characterization, J. S. Park, T. Chi, A. Su, C. Zhu, J. H. Sung*, H. C. Cho*, M. Styczynski, and H. Wang, Georgia Institute of Technology, *Emory University

4.4 - 2:30 p.m.

A Front-end ASIC with Receive Sub-Array Beamforming Integrated with a 32 × 32 PZT Matrix Transducer for 3-D Transesophageal Echocardiography, C. Chen, Z. Chen, D. Bera*, S. B. Raghunathan, M. Shabanimotlagh, E. Noothout, Z.-Y. Chang, J. Ponte**, C. Prins, H. J. Vos, J. G. Bosch*, M. D. Verweij, N. de Jong, M. A.P. Pertijs, Delft University of Technology, *Thoraxcenter, Erasmus MD, **Oldelft Ultrasound

Session 5 – Honolulu Suite
Ultra High Speed Wireline Transceivers

Wednesday, June 15
Chairpersons: A. Momtaz, Broadcom Corporation
J. Lee, National Taiwan University

5.1 - 1:15 p.m.
A Fully-Adaptive Wideband 0.5-32.75Gb/s FPGA Transceiver in 16nm FinFET CMOS Technology, P. Upadhyaya, A. Bekele, D. Turkur Melek, H. Zhao, J. Im, J. Cho, K. H. Tan, S. McLeod, S. Chen, W. Zhang, Y. Frans, K. Chang, Xilinx

5.2 - 1:40 p.m.
A 28.3 Gb/s 7.3 pJ/bit 35 dB Backplane Transceiver with Eye Sampling Phase Adaptation in 28 nm CMOS, H. Miyaoka, F. Terasawa, M .Kudo, H. Kano, A. Matsuda, N. Shirai, S. Kawai, T. Shibasaki*, T. Danjo*, Y. Ogata*, Y. Sakai*, H. Yamaguchi*, T. Mori*, Y. Koyanagi*, H. Tamura*, Y. Ide, K. Terashima, H. Higashi, T. Higuchi, N. Naka, Socionext, *Fujitsu Laboratories Ltd.

5.3 - 2:05 p.m.
A 32 Gb/s Rx Only Equalization Transceiver with 1-tap Speculative FIR and 2-tap Direct IIR DFE, S. Hwang, S. Moon, J. Song, and C. Kim, Korea University

5.4 - 2:30 p.m.
A 56Gb/s PAM4 Wireline Transceiver using a 32-way Time-Interleaved SAR ADC in 16nm FinFET, Y. Frans, M. Elzeftawi, H. Hedayati, J. Im, V. Kireev, T. Pham, J. Shin, P. Upadhyaya, L. Zhou, S. Asuncion, C. Borrelli, G. Zhang, H. Zhang, K. Chang, Xilinx, Inc.

Session 6 – Tapa I
Voltage Regulation

Wednesday, June 15
Chairpersons: N. Van Helleputte, imec
N. Miura, Kobe University

6.1 - 2:55 p.m.
A 50MHz 5V 3W 90% Efficiency 3-Level Buck Converter with Real-Time Calibration and Wide Output Range for Fast-DVS in 65nm CMOS, X. Liu, C. Huang*, P. K. T. Mok, Hong Kong University of Science and Technology, *also with Keio University

6.2 - 3:20 p.m.
95% Light-load Efficiency Single-Inductor Dual-Output DC-DC Buck Converter with Synthesized Waveform Control Technique for USB Type-C, W-H Yang, C-H Lin, K-H Chen, C-L Wey, Y-H Lin*, J-R Lin*,

T-Y Tsai*, J-L Chen**, National Chiao Tung University, *Realtek Semiconductor Corp., **Vanguard Semiconductor Corp.

6.3 - 3:45 p.m.
A Reconfigurable SIMO System with 10-Output Dual-Bus DC-DC Converter using the Load Balancing Function in Group Allocator for Diversified Load Condition, S-U Shin, M-Y Jung, K-D Kim, S-H Park, Y. Huh, C. Shin, S-H Park, J-S Bang, J-B Baek, S-W Choi, Y-M Ju, H-H Cho, KAIST

6.4 - 4:10 p.m.
A Microcontroller with 96% Power-Conversion Efficiency using Stacked Voltage Domains, K. Blutman, A. Kapoor, A. Majumdar, J. Garcia Martinez, J. Echeverri, L. Sevat, A. van der Wel, H. Fatemi, J. Pineda de Gyvez, K. Makinwa*, NXP Semiconductors, *Delft University of Technology

6.5 - 4:35 p.m.
A Fast, Flexible, Positive and Negative Adaptive Body-Bias Generator in 28nm FDSOI, M. Blagojević, M. Cochet, B. Keller*, P. Flatresse, A. Vladimirescu**, B. Nikolić*, STMicroelectronics, *University of California, Berkeley, **ISEP

Session 7 – Honolulu Suite
Low Power RF-Transceivers

Wednesday, June 15
Chairpersons: A. Cathelin, STMicroelectronics
H. Shin, Kwangwoon University

7.1 - 2:55 p.m.
A Bluetooth Low-Energy (BLE) Transceiver with TX/RX Switchable On-Chip Matching Network, 2.75mW High-IF Discrete-Time Receiver, and 3.6mW All-Digital Transmitter, F-W Kuo, S. Binsfeld Ferreira*, M. Babaie**, R. Chen, L-C Cho, C-P Jou, F-L Hsueh, G. Huang***, I. Madadi***, M. Tohidian**, R. Bogdan Staszewski**, TSMC, *Federal University of Rio Grande do Sul, **Delft University of Technology, ***University College Dublin

7.2 - 3:20 p.m.
A 380pW Dual Mode Optical Wake-up Receiver with Ambient Noise Cancellation, W. Lim, T. Jang, I. Lee, H-S Kim, D. Sylvester and D. Blaauw, University of Michigan

7.3 – 3:45 p.m.
SleepTalker: a 28nm FDSOI ULV 802.15.4a IR-UWB Transmitter SoC Achieving 14pJ/bit at 27Mb/s with Adaptive-FBB-based Channel Selection and Programmable Pulse Shape, G. de Streel, F. Stas, T. Gurné, F. Durant, C. Frenkel and D. Bol, Université catholique de Louvain

7.4 - 4:10 p.m.
A 2.4GHz Ternary Sequence Spread Spectrum OOK Transceiver with Harmonic Spur Suppression and Dual-Mode Detection Architecture for ULP Wearable Devices, S.J. Kim, C.S.Park*,Y.Kim*, S.-J.Yun*, Y.-J.Hong*, S.-G.Lee, KAIST, *Samsung Electronics

7.5 - 4:35 p.m.

An 18 µW Spur Canceled Clock Generator for Recovering Receiver Sensitivity in Wireless SoCs, Y. Ogasawara, H. Sakurai, R. Fujimoto, K. Sami, Toshiba Corporation

Technology Executive Panel Discussion

Wednesday, June 15, 6:00 p.m. – 7:00 p.m.

Chairs: Raj Jammy, Carl Zeiss
Satoshi Inaba, Toshiba Electronics Korea Corporation

Semiconductor Business: Inflections Beyond Scaling

Moderator: Dan Hutcheson, CEO and Chairman of VLSI Research Inc and author of The Chip Insider

As semiconductor industry approaches seemingly finite limits of physical scaling, a number of inflections are unfolding around us that may require us to rethink how we design, develop and manufacture semiconductor devices. Sensing, positioning, energy-aware and predictive systems are becoming the norm, opening up wider applications and enormous growth potential for semiconductor industry. Yet, implementation of such technologies from research to reality also poses technical and business challenges. Such systems require ultra-low power, always-on sensing, connectivity, vast embedded and discrete memory, smart energy sources and management - all wrapped in to ever smaller form factors. IoT, self-driving automobiles, next generation 5G networks, machine learning, brain-inspired computing, virtual/immersive reality and many other emerging trends will also need large investments for successful deployment and business models for ROI. The cost of developing such technologies, acceptable standards, security protocols, inter-platform operability, etc., will need unprecedented collaboration in the industry. The panel will deliberate on these topics and discuss trends, applications that are shaping around us, industry needs, infrastructural/manufacturing gaps and economic challenges.

Panelists:

Mike Cadigan, Senior Vice President, Global Sales and Business Development, GLOBALFOUNDRIES
Tze-Chiang Chen, IBM Fellow, IBM TJ Watson Research Center, IBM
SungJoo Hong, EVP and Head of R&D, SK Hynix
Steve Lloyd, Vice President, Engineering and New Product Development, InvenSense
Marie-Noelle Semaria, CEO, CEA LETI

Session 8 – Tapa I

Innovative Systems for a Smart Society

Thursday, June 16
Chairpersons: R. Aitken, ARM

Y. Oike, SONY Corp.

8.1 - 8:05 a.m.
An Energy Harvesting Wireless Sensor Node for IoT Systems Featuring a Near-Threshold Voltage IA-32 Microcontroller in 14nm Tri-Gate CMOS, S. Paul, V. Honkote, R. Kim, T. Majumder, P. Aseron, V. Grossnickle, R. Sankman, D. Mallik, S. Jain, S. Vangal, J. Tschanz, V. De, Intel Corporation

8.2 - 8:30 a.m.
Lensless Smart Sensors: Optical and Thermal Sensing for the Internet of Things (Invited Paper), P. Gill, T. Vogelsang, Rambus Inc.

8.3 - 8:55 a.m.
Features of retinal prosthesis using suprachoroidal transretinal stimulation from an electrical circuit perspective (Invited Paper), Y. Terasawa, K. Shodo, K. Osawa, J. Ohta*, NIDEK Co Ltd, *Nara Institute of Science & Technology

8.4 - 9:20 a.m.
Multi-modal Smart Bio-sensing SoC Platform with >80dB SNR 35µA PPG RX Chain, A. Sharma, S. Lee, A. Polley, S. Narayanan, W. Li, T. Sculley, S. Ramaswamy, Texas Instruments Inc.

8.5 - 9:45 a.m.
An FPGA-accelerated Partial Image Matching Engine for Massive Media Data Searching Systems (Invited Paper), T. Shimizu, Y. Tomita, H. Matsumura, M. Sugimura, H. Yamasaki, D. Thach, T. Miyoshi, T. Baba, Y. Watanabe and A. Ike, Fujitsu Laboratories LTD

Session 9 – Honolulu Suite
Power Management

Thursday, June 16
Chairpersons: J. Nilles, Texas Instruments
K. Kanda, Fujitsu Laboratories, Ltd.

9.1 - 8:05 a.m.
A 66pW Discontinuous Switch-Capacitor Energy Harvester for Self-Sustaining Sensor Applications, X. Wu, Y. Shi, S. Jeloka, K. Yang, I. Lee, D. Sylvester, D. Blaauw, University of Michigan

9.2 - 8:30 a.m.
A Wireless Power Transfer System with Enhanced Response and Efficiency by Fully-Integrated Fast-Tracking Wireless Constant-Idle-Time Control for Implants, C. Huang, T. Kawajiri, H. Ishikuro, Keio University

9.3 - 8:55 a.m.
A Fully Integrated 144 MHz Wireless-Power-Receiver-on-Chip with an Adaptive Buck-Boost Regulating Rectifier and Low-Loss H-Tree Signal Distribution, C.. Kim, J. Park, A. Akinin, S. Ha, R. Kubendran, H. Wang, P. P. Mercier, G. Cauwenberghs, University of California, San Diego

9.4 - 9:20 a.m.

A ±36A Integrated Current-Sensing System with 0.3% Gain Error and 400µA Offset from −55°C to +85°C, S. H. Shalmany, K. A. A. Makinwa, D. Draxelmayr*, Delft University of Technology, *Infineon Technologies

9.5 - 9:45 a.m.
A 114-pW PMOS-Only, Trim-Free Voltage Reference with 0.26% within-Wafer Inaccuracy for nW Systems, Q. Dong, K. Yang, D. Blaauw, D. Sylvester, University of Michigan

Session 10 – Tapa I
Industrial and Power Circuit Directions for a Smart Society

Thursday, June 16
Chairpersons: E. Alon, University of California, Berkeley
M. Takamiya, The University of Tokyo

10.1 - 10:25 a.m.
Motor Control Used to Be Boring (Invited Paper), A. Tessarolo, Texas Instruments Pty Ltd.

10.2 - 10:50 a.m.
A Fully Integrated GaN-based Power IC Including Gate Drivers for High-Efficiency DC-DC Converters (Invited Paper), S. Ujita, Y. Kinoshita, H. Umeda, T. Morita, K. Kaibara, S. Tamura, M. Ishida, T. Ueda, Panasonic Corporation

10.3 - 11:15 a.m.
A Transformer-based Digital Isolator With 20kVPK Surge Capability and > 200kV/µS Common Mode Transient Immunity, R. Yun, J. Sun, E. Gaalaa, B. Chen, Analog Devices Inc.

10.4 - 11:40 a.m.
Innovative System on Chip Platform for Smart Grids and Internet of Energy Applications (Invited Paper), A. Moscatelli, STMicroelectronics

Session 11 – Honolulu Suite
RF Transceiver Techniques

Thursday, June 16
Chairpersons: E. Fogelman, MaxLinear
K. Agawa, Toshiba Corp.

11.1 - 10:25 a.m.
A 65nm CMOS Transceiver with Integrated Active Cancellation Supporting FDD from 1GHz to 1.8GHz at +12.6dBm TX Power Leakage, S. Ramakrishnan, L. Calderin, A. Puglielli, E. Alon, A. Niknejad, B. Nikolić, University of California, Berkeley

11.2 - 10:50 a.m.
Digital PLL for Phase Noise Cancellation in Ring Oscillator-Based I/Q Receivers, Z-Z Chen*, Y Li*, Y-C Kuan*, B Hu*, C-H Wong*, M-C Frank Chang* **, *University of California, Los Angeles, **National Chiao Tung University

11.3 - 11:15 a.m.

A Chopping Switched-Capacitor RF Receiver with Integrated Blocker Detection, +31dBm OB-IIP3, and +15dBm OB-B1dB, Y. Xu, P. Kinget, Columbia University

11.4 - 11:40 a.m.
A 180 mW Multistandard TV Tuner in 28 nm CMOS, J. Xiao, W. Gao, X. Xu, D. Chang, J. Cao, R. Sun, V. Periasamy, N-Y Wang, X. Chen, G. Unruh, T. Hayashi, T-H Chih, L. Krishnan, K-K Huang, S. Dommaraju, G. Wei, B. Shen, A. Venes, D. Koh, J. Y.C. Chang, Broadcom Corporation

Luncheon Talk

Thursday, June 16, 12:15 p.m. – 1:30 p.m.

Cyborg Insects and Other Things: Building Interfaces Between the Synthetic and the Multicellular
Speaker: Michel Maharbiz, University of California, Berkeley

As the computation and communication circuits we build radically miniaturize (i.e. become so low power that 1 pJ is sufficient to bang out a bit of information over a wireless transceiver; become so small that 500 µm^2 of thinned CMOS can hold a reasonable sensor front-end and digital engine), the barrier to introducing these types of interfaces into organisms will get pretty low. Put another way, the rapid pace of computation and communication miniaturization is swiftly blurring the line between the technological base that created us and the technological based we've created. In this talk, I'll give an overview of recent work in my lab that touches on this concern. Most of the talk will cover our ongoing exploration of the remote control of insects in free flight via implantable radio-equipped miniature neural stimulating systems.; recent results with pupally-implanted neural interfaces and extreme miniaturization directions will be discussed. If time permits, I will show recent results building extremely small neural interfaces we call "neural dust," work done in collaboration with the Carmena, Alon and Rabaey labs.

Biography: Michel M. Maharbiz is an Associate Professor with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley.

He received his Ph.D. from the University of California at Berkeley under Professor Roger T. Howe (EECS) and Professor Jay D. Keasling (ChemE); his work led to the foundation of Microreactor Technologies, Inc. which was acquired in 2009 by Pall Corporation. From 2003 to 2007, Michel Maharbiz was an Assistant Professor at the University of Michigan, Ann Arbor. He is the co-founder of Tweedle Technologies, Cortera Neurotech and served as vice-president for product development at Quswami, Inc. from July 2010 to June 2011.

Prof. Maharbiz is a Bakar Fellow and was the recipient of a 2009 NSF Career Award for research into developing microfabricated interfaces for synthetic biology. His group is also known for developing the world's first remotely radio-controlled cyborg beetles. This was named one of the top ten emerging technologies of 2009 by MIT's Technology Review (TR10) and was in Time Magazine's Top 50 Inventions of 2009. Dr. Maharbiz has been a GE Scholar and an Intel IMAP Fellow. Professor Maharbiz's current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods. Michel's long term goal is understanding developmental mechanisms as a way to engineer and fabricate machines."

Session 12 – Tapa I

Circuit/Technology Joint Focus Session:
Embedded Memories

Thursday, June 16

Chairpersons: B. Calhoun, University of Virginia
K. Sohn, Samsung Electronics Co., Ltd.

12.1 - 1:30 p.m.

Full Chip Integration of 3-D Cross-Point ReRAM with Leakage-Compensating Write Driver and Disturbance-Aware Sense Amplifier, S. Lee, J. Song, C. Seong, J. Woo, J.-M. Choi*, C Kwon*, H-J Kim*, H-S Kang*, S. G. Kim**, H. G. Jung**, K-W Kwon*, H Hwang, POSTECH, *SKKU, **SK Hynix Semiconductor Inc.

12.2 - 1:55 p.m.

Embedded Memory and ARM Cortex-M0 Core Using 60 nm C-Axis Aligned Crystalline Indium–Gallium–Zinc Oxide FET Integrated with 65 nm Si CMOS, T. Onuki, W. Uesugi, H. Tamura, A. Isobe, Y. Ando, S. Okamoto, K. Kato, T R Yew*, C. Bin Lin*, J Y Wu*, C. C. Shuai*, S. H. Wu*, J. Myers**, K. Doppler***, M. Fujita^, and S. Yamazaki, Semiconductor Energy Laboratory Co., Ltd., *United Microelectronics Corporation (UMC), *ARM Ltd., **Nokia Technologies, ^VLSI Design and Education Center (VDEC), The University of Tokyo

12.3 - 2:20 p.m.

Versatile TLC NAND Flash Memory Control to Reduce Read Disturb Errors by 85% and Extend Read Cycles by 6.7-times of Read-Hot and Cold Data for Cloud Data Centers, A. Kobayashi, T. Tokutomi and K. Takeuchi, Chuo University

12.4 - 2:45 p.m.

A 0.9µm^2 1T1R Bit Cell in 14nm SoC Process for Metal-Fuse OTP Array with Hierarchical Bitline, Bit Level Redundancy, and Power Gating, Z. Chen, S. Kulkarni, V. Dorgan, U. Bhattacharya, K. Zhang, Intel Corporation.

Session 13 – Honolulu Suite

Analog Techniques

Thursday, June 16

Chairpersons: R. Navid, Rambus, Inc.
M. Ito, Renesas System Design Co., Ltd.

13.1 - 1:30 p.m.

A 0.6mW 31MHz 4th-Order Low-Pass Filter with +29dBm IIP3 Using Self-Coupled Source Follower Based Biquads in 0.18µm CMOS, Y. Xu, S. Leuenberger, P. Venkatachala, U. Moon, Oregon State University

13.2 - 1:55 p.m.

3.5mW 1MHz AM Detector and Digitally-Controlled Tuner in a-IGZO TFT for Wireless Communications in a Fully Integrated Flexible System for Audio Bag, T. Meister*, K. Ishida*, C. Carta*, R. Shabanpour*, B. K.-Boroujeni*, N. Münzenrieder**, L. Petti**, G.A. Salvatore**, G. Schmidt***, P. Ghesquiere****, S. Kiefl****, G. De Toma*****, T. Faetti*****, A.C. Hübler***, G. Tröster**, F. Ellinger*, *Technische

Universität Dresden, **Swiss Federal Institute of Technology Zurich, ***Technische Universität Chemnitz, ****Siemens AG, *****Smartex S.r.l.

13.3 - 2:20 p.m.
A 16-channel Noise-Shaping Machine Learning Analog-Digital Interface, F. N. Buhler*, A. E. Mendrela*, Y. Lim**, J. A. Fredenburg*** and M. P. Flynn*, *University of Michigan, Ann Arbor, MI, **Samsung Electronics, Yongin, Korea, ***Movellus Circuits, Ann Arbor, MI

13.4 - 2:45 p.m.
A Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Blocks, Y. Choi, Y. Lee, S-H Baek, S-J Lee, J. Kim, Seoul National University

Session 14 – Tapa I
Circuits/Technology Joint Focus Session:
Design in Scaled Technologies

Thursday, June 16
Chairpersons: G. Gammie, MediaTek USA
H. Noda, Micron Memory Japan

14.1 - 3:25 p.m.
A 5.8 pJ/Op 115 Billion Ops/sec, to 1.78 Trillion Ops/sec 32nm 1000-Processor Array, B. Bohnenstiehl, A. Stillmaker, J. Pimentel, T. Andreas, B. Liu, A. Tran, E. Adeagbo, B. Baas, University of California, Davis

14.2 - 3:50 p.m.
28nm FDSOI Technology Sub-0.6V SRAM Vmin Assessment for Ultra Low Voltage Applications, R. Ranica, N. Planes, V. Huard, O. Weber*, D. Noblet, D. Croain, F. Giner, S. Naudet, P. Mergault, S. Ibars, A. Villaret, M. Parra, S. Haendler, M. Quoirin, F. Cacho, C. Julien, F. Terrier, L. Ciampolini, D. Turgis, C. Lecocq and F. Arnaud, STMicroelectronics, *CEA-LETI

14.3 - 4:15 p.m.
A 400mV Active VMIN, 200mV Retention VMIN, 2.8 GHz 64Kb SRAM with a 0.09 um2 6T bitcell in a 16nm FinFET CMOS Process, A. Bhavnagarwala, I. Iqbal, A. Nguyen, D. Ondricek, V. Chandra, R. Aitken, ARM Research

14.4 - 4:40 p.m.
A 350mV-900mV 2.1GHz 0.011mm2 Regular Expression Matching Accelerator with Aging-Tolerant Low-VMIN Circuits in 14nm Tri-Gate CMOS, A. Agarwal, S. Hsu, M. Anders, S. Mathew, G. Chen, H. Kaul, S. Satpathy, R. Krishnamurthy, Intel Corporation

14.5 - 5:05 p.m.
Unified Technology Optimization Platform using Integrated Analysis (UTOPIA) for holistic technology, design and system co-optimization at <= 7nm nodes, S. C. Song, J. Xu, D. Yang, K. Rim, P. Feng, J. Bao, J. Zhu, J. Wang, G. Nallapati, M. Badaroglu, P. Narayanasetti, B. Bucki, J. Fischer, and G. Yeap, Qualcomm Technologies Inc.

Session 15 – Honolulu Suite
Successive Approximation ADCs

Thursday, June 16
Chairpersons: R. Kapusta, Analog Devices
K. Okada, Tokyo Institute of Technology

15.1 - 3:25 p.m.
A 12-bit 1.6 GS/s Interleaved SAR ADC with Dual Reference Shifting and Interpolation Achieving 17.8 fJ/conv-step in 65nm CMOS, J.-W. Nam, M. Hassanpourghadi, A. Zhang, M.S. Chen, University of Southern California

15.2 - 3:50 p.m.
A 14.6mW 12b 800MS/s 4×Time-Interleaved Pipelined SAR ADC achieving 60.8dB SNDR with Nyquist input and sampling timing skew of 60fsrms without calibration, Y-C Lien, MediaTek Inc. and University of Twente

15.3 - 4:15 p.m.
An Oscillator Collapse-Based Comparator with Application in a 74.1dB SNDR, 20kS/s 15b SAR ADC, M. Shim, S. Jeong*, P. Myers*, S. Bang*, C. Kim, D. Sylvester*, D. Blaauw*, W. Jung*, Korea University, *University of Michigan

15.4 - 4:40 p.m.
A 0.44fJ/conversion-step 11b 600KS/s SAR ADC with Semi-Resting DAC, S.-E. Hsieh, C.-C. Hsieh, National Tsing Hua University

IEEE Solid-States Circuits Society Young Professionals and Grad Students Mentoring and Career coaching event
Thursday, June 16, 6:30 p.m. – 7:30 p.m.

IEEE Solid-States Circuits Society Executives and AdCom members will have a mentoring session on career coaching, entrepreneurship, publications and answer your questions.

Circuits Panel Sessions

Thursday, June 16, 8:00 p.m. – 10:00 p.m.

P1 Top circuit techniques: Life with and without them

Organizers: Dejan Markovic, University of California, Los Angeles
Kenichi Okada, Tokyo Institute of Technology

Moderator: Un-Ku Moon, Oregon State University

Panel consisting of experts from different areas will provide a review of the highest-impact circuit techniques, and give examples of how these techniques brought significant system advances. After the

opening statement from each of panelists, limited to one technique, audience can debate to gauge the impact of those techniques. At the end of the panel discussion, everyone can join to vote the top three circuit techniques in 2016.

Panelists:

Asad Abidi, University of California, Los Angeles
Cyrus Afghahi, Broadcom
Ippei Akita, Toyohashi University
Andreas Burg, EPFL
Meng-Fan (Marvin) Chang, Nat'l Tsing Hua University
Muhammad Khellah, Intel
Takahiro Miki, Renesas
Adrian Tang, Jet Propulsion Lab

P2 It's all a common platform – how do I build a differentiated product?

Organizers: Fatih Hamzaoglu. Intel
Masanori Hashimoto, Osaka, University

Moderator: Ajith Amerasekera, Texas Instruments

Chip industry has been very competitive in recent years as semiconductor Foundry, Memory suppliers, IP developers, and EDA tools have diminished to few players. With very tight TTM (Time to Market) and cost requirements, vendors have limited value options to add to their products to differentiate from competition. The panelists will discuss how innovation, software hardware co-design, cost vs. performance optimization, user interface and other factors can differentiate their products even with common infrastructure.

Panelists:

Robert Aitken, ARM
Mark Doran, Intel
Takashi Kono, Renesas
Suk Lee, TSMC
Hugh Mair, MediaTek
Hoi Jun Yoo, KAIST
Steve Young, Xilinx

Session 16 – Tapa I

Advanced Wireline Techniques

Friday, June 17

Chairpersons: J. T. Pawlowski, Micron Technologies, Inc.
Y. Tomita, Fujitsu Laboratories, Ltd.

16.1 - 8:05 a.m.

A 35 mW 10 Gb/s ADC-DSP less Direct Digital Sequence Detector and Equalizer in 65nm CMOS, AKM D. Hossain, Aurangozeb, M. Mohammad*, M. Hossain, University of Alberta, *Qualcomm Atheros

16.2 - 8:30 a.m.

A 125 mW 8.5-11.5 Gb/s Serial Link Transceiver with a Dual Path 6-bit ADC/5-tap DFE Receiver and a 4-tap FFE Transmitter in 28 nm CMOS, B. Raghavan, A. Varzaghani, L. Rao, H. Park, X. Yang, Z. Huang, Y. Chen, R. Kattamuri, C. Wu, B. Zhang, J. Cao, A. Momtaz, N. Kocaman, Broadcom Corp.

16.3 - 8:55 a.m.

A 0.003 mm² 5.2 mW/tap 20 GBd Inductor-less 5-Tap Analog RX-FFE, R. Boesch, K. Zheng, B. Murmann, Stanford University

16.4 - 9:20 a.m.

A 16Gb/s 14.7mW Tri-Band Cognitive Serial Link Transmitter with Forwarded Clock to Enable PAM-16/256-QAM and Channel Response Detection in 28 nm CMOS, Y. Du, W-H Cho, Y. Li, C-H Wong, J. Du, P-T Huang*, Y. Kim, Z-Z Chen, S. J. Lee, M-C Frank Chang, University of California, Los Angeles, *National Chiao Tung University, Taiwan

16.5 - 9:45 a.m.

A Low-EMI Four-Bit Four-Wire Single-Ended DRAM Interface by Using a Three-Level Balanced Coding Scheme, I-M Yi, S-J Bae*, M-K Chae, S-M Lee, Y-J Jang, Y-C Cho*, Y-S Sohn*, J-H Choi*, S-J Jang*, B. Kim, J-Y Sim, H-J Park, POSTECH, *Samsung Electronics Co.

Session 17 – Tapa II

Digital Architectures and Processors

Friday, June 17

Chairpersons: E. Beigne,CEA-LETI
M. Natsui, Tohoku University

17.1 - 8:05 a.m.

A 0.3-2.6 TOPS/W Precision-Scalable Processor for Real-Time Large-Scale ConvNets, B. Moons, M. Verhelst, KU Leuven

17.2 - 8:30 a.m.

A 1.40mm2 141mW 898GOPS Sparse Neuromorphic Processor in 40nm CMOS, P. Knag, C. Liu, Z. Zhang, University of Michigan

17.3 - 8:55 a.m.

A 190GFLOPS/W DSP for Energy-Efficient Sparse-BLAS in Embedded IoT, R. Dorrance, D. Marković, University of California, Los Angeles

17.4 - 9:20 a.m.
A 58.6mW Real-Time Programmable Object Detector with Multi-Scale Multi-Object Support Using Deformable Parts Model on 1920x1080 Video at 30fps, A. Suleiman, Z. Zhang, V. Sze, MIT

17.5 - 9:45 a.m.
Adaptive Clocking with Dynamic Power Gating for Energy Efficiency Improvement in a 22nm Graphics Execution Core under Fast Voltage Droop, M. Cho, C. Tokunaga, S. Kim, J. Tschanz, M. Khellah, V. De, Intel Corporation

Session 18 – Tapa III
Advanced Sensor Circuits

Friday, June 17
Chairpersons: D. Sylvester, University of Michigan
S.H. Cho, KAIST

18.1 - 8:05 a.m.
A 0.23 micro-g Bias Instability and 1.6 micro-g/rt(Hz) Resolution Silicon Oscillating Accelerometer with Build-in Sigma-Delta Frequency-to-Digital Converter, J. Zhao, X. Wang*, Y. Zhao, G. M. Xia, A. P. Qiu, Y. Su, Y. P. Xu*, Nanjing University of S&T, *National University of Singapore

18.2 - 8:30 a.m.
A BJT-based Temperature-to-Digital Converter with ±60mK (3σ) Inaccuracy from -70°C to 125°C in 160nm CMOS, B. Yousefzadeh, S. H. Shalmany, K. Makinwa, Delft University of Technology

18.3 - 8:55 a.m.
A 28nm CMOS Ultra-Compact Thermal Sensor in Current-Mode Technique, M. Eberlein, I. Yahav, Intel Corporation

18.4 - 9:20 a.m.
A 35fJ/Step Differential Successive Approximation Capacitive Sensor Readout Circuit with Quasi-Dynamic Operation, H. Omran, A. Alhoshany, H. Alahmadi, K. N. Salama, King Abdullah University of Science and Technology (KAUST)

18.5 - 9:45 a.m.
A 9.84–73.2 nJ, 0.048 mm2 Time-Domain Impedance Sensor that Provides Values of Resistance and Capacitance, Y. Hong*, Y. Wang*, W. L. Goh*, Y. Gao**, L. Yao**, *Nanyang Technological University, **Institute of Microelectronics

Session 19 – Tapa I
High Speed Data Converters

Friday, June 17
Chairpersons: K. Makinwa, Delft University of Technology
T. Okumoto, Socionext

19.1 - 10:25 a.m.
A 23mW 24GS/s 6b Time-Interleaved Hybrid Two-Step ADC in 28nm CMOS, B. Xu, Y. Zhou, Y. Chiu, University of Texas at Dallas

19.2 - 10:50 a.m.
A 8.2-mW 10-b 1.6-GS/s 4× TI SAR ADC with Fast Reference Charge Neutralization and Background Timing-Skew Calibration in 16-nm CMOS, Y.-Z. Lin, C.-H. Tsai, S.-C. Tsou, C.-H. Lu, MediaTek Inc.

19.3 - 11:15 a.m.
A 14-bit 2.5GS/s and 5GS/s RF Sampling ADC with Background Calibration and Dither, A.M.A. Ali, H. Dinc, P. Bhoraskar, S. Puckett, A. Morgan, N. Zhu, Q. Yu, C. Dillon, B. Gray, J. Lanford, M. McShea, U. Mehta, S. Bardsley, P. Derounian, R. Bunch, R. Moore, G. Taylor, Analog Devices

19.4 - 11:40 a.m.
A 14-bit 8.9GS/s RF DAC in 40nm CMOS achieving >71dBc LTE ACPR at 2.9GHz, V. Ravinuthula, W. Bright, M. Weaver, K. Maclean, S. Kaylor, S. Balasubramanian, J. Coulon, R. Keller, B. Nguyen, E. Dwobeng, Texas Instruments Incorporated

Session 20 – Tapa II
VCOs and Optical Building Blocks

Friday, June 17
Chairpersons: E. Janssen, NXP Semiconductors
K. Sunaga, NEC Corporation

20.1 - 10:25 a.m.
A 7-to-18.3GHz Compact Transformer based VCO in 16nm FinFET, M. Raj, P. Upadhyaya, Y. Frans, K. Chang, Xilinx Inc.

20.2 - 10:50 a.m.
-197dBc/Hz FOM 4.3-GHz VCO Using an Addressable Array of Minimum-Sized NMOS Cross-Coupled Transistor Pairs in 65-nm CMOS, A. Jha, A. Ahmadi, S. Kshattry, T. Cao* K. Liao**, G. Yeap**, Y. Makris and K. K. O, The University of Texas at Dallas, *Cornell University, **Qualcomm Technologies

20.3 - 11:15 a.m.
A 10Gb/s, 342fJ/bit Micro-Ring Modulator Transmitter with Switched-Capacitor Pre-Emphasis and Monolithic Temperature Sensor in 65nm CMOS, S. Saeedi, and A. Emami*, Oracle Labs, *California Institute of Technology

20.4 - 11:40 a.m.
A 50.6-Gb/s 7.8-mW/Gb/s –7.4-dBm Sensitivity Optical Receiver based on 0.18-um SiGe BiCMOS Technology, T. Takemoto, Y. Matsuoka, H. Yamashita, Y. Lee, K. Akita, H. Arimoto, M. Kokubo, and T. Ido, Hitachi Ltd.

Session 21 – Tapa III
Advanced Imagers

Friday, June 17
Chairpersons: A. Molnar, Cornell University
Y. Hirose, Panasonic Corporation

21.1 - 10:25 a.m.
An 8.3M-pixel 480fps Global-Shutter CMOS Image Sensor with Gain-Adaptive Column ADCs and 2-on-1 Stacked Device Structure, Y. Oike, K. Akiyama, L. D. Hung, W. Niitsuma, A. Kato, M. Sato, Y. Kato, W. Nakamura, H. Shiroshita, Y. Sakano, Y. Kitano*, T.. Nakamura*, T. Toyama, H. Iwamoto, T. Ezaki, Sony, *Sony Semiconductor

21.2 - 10:50 a.m.
A Dead-time Free Global Shutter CMOS Image Sensor with in-pixel LOFIC and ADC using Pixel-wise Direct Connections, H. Sugo, S. Wakashima, R. Kuroda, Y. Yamashita*, H. Sumi*, T.-J. Wang*, P.-S. Chou*, M.-C. Hsu*, S. Sugawa, Tohoku Univ., *TSMC

21.3 - 11:15 a.m.
A 220pJ/Pixel/Frame CMOS Image Sensor with Partial Settling Readout Architecture, S. Ji, J. Pu, B. Lim, M. Horowitz, Stanford University

21.4 - 11:40 a.m.
A 260µW Infrared Gesture Recognition System-on-Chip for Smart Devices, S. Oh, N. Le Ba*, S. Bang, J. Jeong**, D. Blaauw, T. Kim*, D. Sylvester, University of Michigan, *Nanyang Technological University, **Korea University

"30th Symposium on VLSI Circuits"
SSCS sponsored Lunch

Friday, June 17, 12:15 p.m. – 1:30 p.m.

Session 22 – Tapa I
Clock and Frequency Synthesis

Friday, June 17
Chairpersons: V. Agrawal, Cypress Semiconductor
J.-Y. Sim, Pohang University of Science and Technology

22.1 - 1:30 p.m.
An Inductor-less Fractional-N Injection-Locked PLL with a Spur-and-Phase-Noise Filtering Technique, A. Li, Y. Chao, X. Chen, L. Wu, H. Luong, The Hong Kong University of Science and Technology

22.2 - 1:55 p.m.
An 8.865-GHz -244dB-FOM High-Frequency Piezoelectric Resonator-Based Cascaded Fractional-N PLL with Sub-ppb-Order Channel Adjusting Technique, S. Ikeda, H. Ito, A. Kasamatsu*, Y. Ishikawa, T. Obara, N. Noguchi, K. Kamisuki, Y. Jiyang, S. Hara*, D. Ruibing*, S. Dosho, N. Ishihara, K. Masu, Tokyo Tech, *NICT

22.3 - 2:20 p.m.
A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer, L. Kong, B. Razavi, University of California, Los Angeles

22.4 - 2:45 p.m.
A PVT-Robust −59-dBc Reference Spur and 450-fsRMS Jitter Injection-Locked Clock Multiplier Using a Voltage-Domain Period-Calibrating Loop, Y. Lee, H. Yoon, M. Kim, J. Choi, Ulsan National Institute of Science and Technology

22.5 - 3:10 p.m.
A 0.034mm^2 , 725fs RMS Jitter, 1.8%/V Frequency-Pushing, 10.8-19.3GHz Transformer-Based Fractional-N All-Digital PLL in 10nm FinFET CMOS, C-C Li, T-H Tsai, M-S Yuan, C-C Liao, C-H Chang, T-C. Huang, H-Y Liao, C-T Lu, H-Y Kuo, K. Hsieh, M. Chen, A., XimeneS*, R. Bogdan Staszewski*, TSMC, *Delft University of Technology, **University College Dublin

Session 23 – Tapa II
Hardware Security and Application Specific Digital Design

Friday, June 17
Chairpersons: V. Sze, Massachusetts Institute of Technology
K. Fujii, NTT Device Innovation Center

23.1 - 1:30 p.m.
250mV-950mV 1.1Tbps/W Double Affine Mapped Sbox based Composite-Field SMS4 Encrypt/Decrypt Accelerator in 14nm Tri-gate CMOS, S. Satpathy, S. Mathew, V. Suresh, M. Anders, G. Chen, H. Kaul, A. Agarwal, S. Hsu, R. Krishnamurthy, Intel Corporation

23.2 - 1:55 p.m.
A Compact 446 Gbps/W AES accelerator for Mobile SoC and IoT in 40nm, Y. Zhang, K. Yang, M. Saligane, D. Blaauw, D. Sylvester, University of Michigan

23.3 - 2:20 p.m.
A 4fJ/bit Delay-Hardened Physically Unclonable Function Circuit with Selective Bit Destabilization in 14nm Tri-gate CMOS, S. Mathew, S. Satpathy, V. Suresh, M. Anders, H. Kaul, A. Agarwal, S. Hsu, G. Chen, R. Krishnamurthy, VivV.ek De, Intel Corporation

23.4 - 2:45 p.m.
A 0.58mm2 2.76Gb/s 79.8pJ/b 256-QAM Massive MIMO Message-Passing Detector, W. Tang, C.-H. Chen*, Z. Zhang, University of Michigan, *Intel Labs

23.5 - 3:10 p.m.
A Machine-learning Classifier Implemented in a Standard 6T SRAM Array, J. Zhang, Z. Wang, and N. Verma Princeton University

Session 24 – Tapa III
Neural Interfaces and Processing

Friday, June 17

Chairpersons: D. Markovic, University of California, Los Angeles
J. Ohta, Nara Institute of Science and Technology

24.1 - 1:30 p.m.

A 16-Channel 1.1mm2 Implantable Seizure Control SoC with Sub-µW/Channel Consumption and Closed-Loop Stimulation in 0.18µm CMOS, M. Shoaran, M. Shahshahani*, M. Farivar, J. Almajano**, A. Shahshahani*, A. Schmid*, A. Bragin**, Y. Leblebici*, A. Emami, Caltech, *EPFL, **UCLA

24.2 - 1:55 p.m.

A Microelectrode Array with 8,640 Electrodes Enabling Simultaneous Full-frame Readout at 6.5 kfps and 112-Channel Switch-Matrix Readout at 20 kS/s, X. Yuan, S. Kim, J. Juyon, M. D'Urbino, T. Bullmann, Y. Chen*, A. Stettler*, A. Hierlemann*, U. Frey, RIKEN Japan, *ETH Zurich, TU Delft

24.3 - 2:20 p.m.

A Wearable Ear-EEG Recording System Based on Dry-Contact Active Electrodes, X. Zhou*,**, Q. Li**, S. Kilsgaard***, F. Moradi*, S. L. Kappel*, P. Kidmose*, *Aarhus University, **UESTC, ***Widex A/S

24.4 - 2:45 p.m.

A 2.048 Mb/s Full-Duplex Free-Space Optical Transceiver IC for a Real-Time In Vivo Neurofeedback Mouse Experiment Under Social Interaction, G. Hwang, J.-K. Choi, J. Yang, S. Lim, J.-M. Kim, M.-G. Choi, D.-S. Kim, K. Gwak, J. Jeon, H. S. Shin*, I.-H. Choi*, S. Park*, H.-M. Bae, KAIST, *Institute for Basic Science

24.5 - 3:10 p.m.

A 450mV Timing-Margin-Free Waveform Sorter based on Body Swapping Error Correction, S. Kim, J. Pedro Cerqueira, M. Seok, Columbia University