**VLSI Technology Short Course 2016**

Monday, June 13, 8:30 a.m. – 5:10 p.m.

**Inflections in VLSI Technologies – Cloud and Beyond**

Organizers: Chorng-Ping Chang, Applied Materials
Shinya Yamakawa, Sony Corporation

**8:30 a.m. - Brief outline** - Chorng-Ping Chang

**Cloud Computing**

**8:35 a.m.** **The Future of HP Computing – Technology Scaling and Hardware Accelerators:** Terence Hook, IBM

**9:10 a.m.** **Silicon Photonics Technology Enabling Both Low Power Consumption and High Aggregated Bandwidth:** Ken Morito, PETRA

**9:45 a.m.** **Confluence of Memory and Storage Technologies:** Craig Hampel, Rambus

**10:20 a.m.** **Break**

**10:35 a.m.** **5G: From Data Center to Mobile Phone, System Architecture Influences on Semiconductor Technology Requirements:** Ted Letavic, GlobalFoundries

**11:10 a.m.** **Cloud Computing: Everything Close with 3D System Integration:** Denis Dutoit, CEA-LETI

**11:45 a.m.** **Performances and Application of Power Devices in Si, SiC and GaN:** Salvo Coffa, STMicroelectronics

**12:20 p.m. -** **Lunch**

**The Beyond: Edge Computing and Emerging Horizons**

**1:30 p.m.** **The Road to Ultra-Low Energy Computation:** Jan Rabaey, UC Berkeley

**2:10 p.m.** **Challenge of MOS/MTJ-Hybrid Nonvolatile VLSI Processor for IoE Applications:** Takahiro Hanyu, Tohoku U.

**2:50 p.m.** **Recent Progress in Neuromorphic Computing:** Geoffrey Burr, IBM

**3:30 p.m.** **Break**

**3:45 p.m.** **Flexible Sensors for Health-Monitoring Applications:** Takao Someya, U. Tokyo

**4:25 p.m.** **Battery Life Considerations for Mobile PCs:** Kamal Shah, Intel

**5:05 p.m.** **Adjourn**

Session 1 – TAPA I & II

**Plenary Session**

Tuesday, June 14, 8:05 a.m.

Chairpersons: M. Khare, IBM Research
M. Masahara, AIST

**8:05 a.m.** **Welcome and Opening Remarks**
R. Jammy, Carl Zeiss
S. Inaba, Toshiba Corporation Storage & Electronic Devices Solutions Company

**1.1 – 8:35 a.m.**

**The Age of Sensors – How MEMS sensors will enable the next wave of new products (Invited),** Stephen Lloyd, VP of Engineering and New Product Development, InvenSense, Inc.

**1.2 – 9:20 a.m.**

**Intelligent Mobility realized through VLSI (Invited),** Takao Asami, Senior Vice President, Nissan

Session 2 - TAPA I & II

**Technology Highlights Session**

Tuesday, June 14

Chairpersons: G. Yeap, Qualcomm
K. Endo, AIST

**2.1 - 10:25 a.m.**

**Si FinFET based 10nm Technology with Multi Vt Gate Stack for Low Power and High Performance Applications,** H.-J. Cho, H. S. Oh, K. J. Nam, Y. H. Kim, K. H. Yeo, W. D. Kim, Y. S. Chung, Y. S. Nam, S. M. Kim, W. H. Kwon, M. J. Kang, I. R. Kim, H. Fukutome, C. W. Jeong, H. J. Shin, Y. S. Kim, D. W. Kim, S. H. Park, H. S. Oh, J. H. Jeong, S. B. Kim, D. W. Ha, J. H. Park, H. S. Rhee, S. J. Hyun, D. S. Shin, D. H. Kim, H. Y. Kim, S. Maeda, K. H. Lee, Y. H. Kim, M. C. Kim, Y. S. Koh, B. Yoon, K. Shin, N. I. Lee, S. B. Kangh, K. H. Hwang, J. H. Lee, J.-H. Ku, S. W. Nam, S. M. Jung, H. K. Kang, J. S. Yoon, E. S. Jung, Samsung Electronics

**2.2 - 10:50 a.m.**

**FINFET Technology Featuring High Mobility SiGe Channel for 10nm and Beyond,** D. Guo, G. Karve, G. Tsutsui, K.-Y. Lim*, R. Robison, T. Hook, R. Vega, D. Liu, S. Bedell, S. Mochizuki, F. Lie, K. Akarvardar*, M. Wang, R. Bao, S. Burns, V. Chan, K. Cheng, J. Demarest, J. Fronheiser*, P. Hashemi, J. Kelly, J. Li, N. Loubet, P. Montanini, B. Sahu*, M. Sankarapandian, S. Sieg, J. Sporre, J. Strane, R. Southwick, N. Tripathi*, R. Venigalla, J. Wang, K. Watanabe, C. W. Yeung, D. Gupta, B. Doris, N. Felix, A. Jacob*, H. Jagannathan, S. Kanakasabapathy, R. Mo, V. Narayanan, D. Sadana, P. Oldiges, J. Stathis, T. Yamashita, V. Paruchuri, M. Colburn, A. Knorr*, R. Divakaruni, H. Bu, M. Khare, IBM, *GLOBALFOUNDRIES Inc.

**2.3 - 11:15 a.m.**

**High performance $In_{0.53}Ga_{0.47}As$ FinFETs Fabricated on 300 mm Si Substrate,** M. L. Huang, S. W. Chang, M. K. Chen, Y. Oniki, H. C. Chen, C. H. Lin, W. C. Lee, C. H. Lin, M. A. Khaderbad, K. Y. Lee, Z. C. Chen, P. Y. Tsai, L. T. Lin, M. H. Tsai, C. L. Hung, T. C. Huang, Y. C. Lin, Y.-C. Yeo, S. M. Jang, H. Y. Hwang, H. C.-H. Wang, and C. H. Diaz, TSMC

**2.4 - 11:40 a.m.**
**Achieving Sub-ns switching of STT-MRAM for future embedded LLC applications through improvement of nucleation and propagation switching mechanisms,** G. Jan, L. Thomas, S. Le, Y.-J. Lee, H. Liu, J. Zhu, J. Iwata-Harms, S. Patel, R.-Y. Tong, S. Serrano-Guisan, D. Shen, R. He, J. Haq, J. Teng, V. Lam, R. Annapragada, Y.-J. Wang, T. Zhong, T. Torng, P.-K. Wang,TDK-Headway Technologies, Inc.

## Session 3 – Tapa I
## Technology Focus Session:
## System and Embedded Memory

Tuesday, June 14
Chairpersons: N. Ramaswamy, Micron Technology, Inc.
S. Chung, National Chiao Tung University

**3.1 – 1:30 p.m.**
**Memory: Welcome to the Era of Innovative Architectures (Invited),** D. Klein, Micron Technology, Inc.

**3.2 – 1:55 p.m.**
**High-Density User-Programmable Logic Array Based on Adjacent Integration of Pure-CMOS Crossbar Antifuse into Logic CMOS Circuits,** S. Yasuda, M. Oda, M. Matsumoto, K. Tatsumura, K. Zaitsu, Y.-H. Ho, M. Ono, Toshiba Corporation

**3.3 – 2:20 p.m.**
**Advanced Non-volatile Embedded Memories for a Wide Range of Applications (Invited),** S. Kimura, Hitachi, Ltd.

**3.4 – 2:45 p.m.**
**Random Soft Error Suppression by Stoichiometric Engineering: CMOS Compatible and Reliable 1Mb $HfO_2$-ReRAM with 2 Extra Masks for Embedded IoT Systems,** C. Ho, T. Y. Shen, P. Y. Hsu, S. C. Chang, S. Y. Wen, M. H. Lin, P. K. Wang, S. C. Liao, C. S. Chou, K. M. Peng, C. M. Wu, W. H. Chang, Y. H. Chen, F. Chen, L. W. Lin, T. H. Tsai, S. F. Lim, C. J. Yang, M. H. Shieh, H. H. Liao, C. H. Lin, P. L. Pai, T. Y. Chan, Y. C. Chiao, Winbond Electronics Corporation

## Session 4 – Tapa II
## Ge and SiGe Channel Devices

Tuesday, June 14
Chairpersons: L. Selmi, University of Udine
K. Tateiwa, Tower Panasonic Semiconductor, Ltd.

**4.1 - 1:30 p.m.**
**Understanding Charge Traps for Optimizing Si-passivated Ge nMOSFETs,** P. Ren, R. Gao, Z. Ji, H. Arimura*, J. F. Zhang, R. Wang**, M. Duan, W. Zhang, J. Franco*, S. Sioncke*, D. Cott*, J. Mitard*, L. Witters*, H. Mertens*, B. Kaczer*, A. Mocuta*, N. Collaert*, D. Linten*, R. Huang**, A. V.-Y. Thean*, and G. Groeseneken*, Liverpool John Moores University, *IMEC, **Peking University

**4.2 - 1:55 p.m.**

**A 2nd Generation of 14/16nm-Node Compatible Strained-Ge pFinFET with Improved Performance with respect to Advanced Si-channel FinFETs,** J. Mitard, L. Witters, Y. Sasaki, H. Arimura, A. Schulze, R. Loo, L.-Å. Ragnarsson, A. Hikavyy, D. Cott, T. Chiarella, S. Kubicek, H. Mertens, R. Ritzenthaler, C. Vrancken, P. Favia, H. Bender, N. Horiguchi, K. Barla, D. Mocuta, A. Mocuta, N. Collaert, A.V.-Y. Thean, IMEC

**4.3 - 2:20 p.m.**

**Selective $GeO_x$-Scavenging from Interfacial Layer on $Si_{1-x}Ge_x$ Channel for High Mobility $Si/Si_{1-x}Ge_x$ CMOS Application,** C. H. Lee, H. Kim*, P. Jamison, R. G. Southwick III, S. Mochizuki, K. Watanabe, R. Bao, R. Galatage*, S. Guillaumet**, T. Ando, R. Pandey*, A. Konar*, B. Lherron**, J. Fronheiser*, S. Siddiqui*, H. Jagannathan, V. Paruchuri, IBM Research, *GLOBALFOUNDRIES Inc., **STMicroelectronics

**4.4 - 2:45 p.m.**

**Demonstration of Record SiGe Transconductance and Short-Channel Current Drive in High-Ge-Content SiGe PMOS FinFETs with Improved Junction and Scaled EOT,** P. Hashemi, K.-L. Lee, T. Ando, K. Balakrishnan, J. A. Ott, S. Koswatta, S. U. Engelmann, D.-G. Park, V. Narayanan, R. T. Mo, E. Leobandung, IBM Research

Session 5 – Tapa III

**Device Reliability**

Tuesday, June 14

Chairpersons: C.-P. Chang, Applied Materials
T. Yamashita, Renesas Electronics Corporation

**5.1 - 1:30 p.m.**

**Demonstration of an InGaAs Gate Stack with Sufficient PBTI Reliability by Thermal Budget Optimization, Nitridation, High-*k* Material Choice, and Interface Dipole,** J. Franco, A. Vais*, S. Sioncke, V. Putcha*, B. Kaczer, B.-S. Shie, X. Shi, R. Mahlouji, L. Nyns, D. Zhou, N. Waldron, J.W. Maes**, Q. Xie**, M. Givens***, F. Tang***, X. Jiang***, H. Arimura, T. Schram, L.-Å Ragnarsson, A. Sibaja Hernandez, G. Hellings, N. Horiguchi, M. Heyns*, G. Groeseneken*, D. Linten, N. Collaert, A. Thean, imec Belgium, *also at KU Leuven; **ASM Belgium; ***ASM America

**5.2 - 1:55 p.m.**

**Application of CVS and VRS Method for Correlation of Logic CMOS Wear Out to Discrete Device Degradation Based on Ring Oscillator Circuits,** A. Kerber, T. Nigam, GLOBALFOUNDRIES Inc.

**5.3 - 2:20 p.m.**

**Deep Insight into Process-induced Pre-existing Traps and PBTI Stress-induced Trap Generations in High-*k* Gate Dielectrics through Systematic RTN Characterizations and *Ab-initio* Calculations,** J. Chen, Y. Nakasaki, Y. Mitani, Toshiba Corporation

**5.4 - 2:45 p.m.**

**Hot Carrier Degradation in Nanowire Transistors: Physical mechanisms, Width dependence and Impact of Self-Heating,** A. Laurent, X. Garros, S. Barraud, G. Mariniello, G. Reimbold, D. Roy*, E. Vincent*, G. Ghibaudo**, CEA-LETI, *STMicroelectronics, **IMEP-LAHC

Session 6 – Tapa I

**Novel 2D Materials and Devices**

Tuesday, June 14

Chairpersons: P. Ye, Purdue University
M. Kobayashi, The University of Tokyo

**6.1 - 3:25 p.m.**

**$MoS_2$ U-shape pMOSFET with 10 nm Channel Length and Poly-Si $MoS_2$ Source/Drain Serving as Seed for Full Wafer CVD $MoS_2$ Availability,** K.-S. Lee, B.-W. Wu, L.-J. Lee*, M.-Y. Lee*, C. Chin, K. Cheng***, C.-L. Hsu, C.-H. Lin, Y.-J. Chen, C.-C. Chen, C.-T. Wu, M.-C. Chen, J.-M. Shieh, W.-K. Yeh, Y.-L. Chueh♦, F.-L. Yang**, C. Hu◊, National Applied Research Laboratories, * King Abdullah University of Science and Technologies, ** Academia Sinica, ***National Chiao Tung University, ♦ National Tsing Hua University, ◊ University of California Berkeley

**6.2 - 3:50 p.m.**

**Serially Connected Monolayer MoS2 FETs with Channel Patterned by a 7.5 nm Resolution Directed Self-Assembly Lithography** A.Nourbakhsh, A. Zubair, A. Tavakkoli, R. Sajjad, X. Ling, M. Dresselhaus, J. Kong, K. K. Berggren, D. Antoniadis and T. Palacios, Massachusetts Institute of Technology

**6.3 - 4:15 p.m.**

**GDOT: A Graphene-Based Nanofunction for Dot-Product Computation,** N. C. Wang, S. K. Gonugondla*, I. Nahlus*, N. R. Shanbhag*, E. Pop, Stanford University, *University of Illinois Urbana-Champaign

**6.4 - 4:40 p.m.**

**Extremely Low Power C-Axis Aligned Crystalline In-Ga-Zn-O 60 nm Transistor Integrated with Industry 65 nm Si MOSFET for IoT Normally-Off CPU Application,** S. H. Wu, X. Y. Jia, M. Kui, C. C. Shuai, T. Y. Hsieh, H. C. Lin, D. Chen, C. B. Lin, J. Y. Wu, T. R. Yew, Y. Endo*, K. Kato*, S. Yamazaki*, UMC, *Semiconductor Energy Laboratory

**6.5 - 5:05 p.m.**

**A Sub-ns Three-terminal Spin-orbit Torque Induced Switching Device,** S. Fukami, T. Anekawa, A. Ohkawara, C. Zhang, H. Ohno, Tohoku University

Session 7 - Tapa II

**Contact Resistance Innovations for Sub-10nm Scaling**

Tuesday, June 14

Chairpersons: R. Arghavani, LAM Research
T.-R. Yew, United Microelectronics Corp.

**7.1 - 3:25 p.m.**

**Ultralow-Resistivity CMOS Contact Scheme with Pre-Contact Amorphization Plus Ti (Germano-) Silicidation,** H. Yu*, M. Schaekers, A. Hikavyy, E. Rosseel, A. Peter, K. Hollar**, F. A. Khaja**, W. Aderhold**, L. Date**, A. J. Mayur**, J.-G. Lee***, K. M. Shin#, B. Douhard, S. A. Chew, S. Demuynck, S.

Kubicek, D. Kim***, A. Mocuta, K. Barla, N. Horiguchi, N. Collaert, A.V.-Y. Thean, K. De Meyer*, Imec, *imec and Katholieke Universiteit Leuven, **Applied Materials, ***Samsung, #Samsung assegnee at imec

**7.2 - 3:50 p.m.**

**Ti and NiPt/Ti Liner Silicide Contacts for Advanced Technologies,** P. Adusumilli, E. Alptekin*, M. Raymond**, N. Breil*,□, F. Chafik◊,#, C. Lavoie*,♦, D. Ferrer***, S. Jain***, V. Kamineni**, A. Ozcan♦, S. Allen***, J. J. An***, V. Basker, R. Bolam*, H. Bu, J. Cai♦, J. Demarest, B. Doris♦, E. Engbrecht***, S. Fan, J. Fronheiser**, O. Gluschenkov, D. Guo, B. Haran, D. Hilscher***, H. Jagannathan, D. Kang***, Y. Ke***, J. Kim**, S. Koswatta♦, A. Kumar***, A. Labonte**, R. Lallement◊, W. Lee*, Y. Lee, J. Li, C-H Lin***, B. Liu**, Z. Liu, N. Loubet, N. Makela***, S. Mochizuki, B. Morgenfeld***, S. Narasimha***, T. Nesheiwat***, H. Niimi**, C. Niu**, M. Oh***, C. Park**, R. Ramachandran*, J. Rice***, V. Sardesai***, J. Shearer, C. Sheraw***, C. Tran***, G. Tsutsui, H. Utomo, K. Wong***, R. Xie**, T. Yamashita, Y. Yan***, C. Yeh♦, M. Yu***, N. Zamdmer*, N. Zhan***, B. Zhang***, V. Paruchuri, C. Goldberg◊, W. Kleemeier**, S. Stiffler***, R. Divakaruni*, W. Henson***, IBM Research, Albany, *IBM Systems, Hopewell Junction, **GLOBALFOUNDRIES, Albany, ***GLOBALFOUNDRIES, Hopewell Junction; ♦IBM Research, Yorktown Heights, ◊STMicroelectronics, Albany, □Now with Applied Materials, CA; # Now with Qualcomm Technologies

**7.3 - 4:15 p.m.**

**Ultra-Low NMOS Contact Resistivity Using a Novel Plasma-Based DSS Implant and Laser Anneal for Post 7 nm Nodes,** C.-N. Ni, K. V. Rao, F. Khaja, S. Sharma, S. Tang, J. J. Chen, K. E. Hollar, N. Breil, X. Li, M. Jin, C. Lazik, J. Lee, H. Maynard, N. Variam, A. J. Mayur, S. Kim, H. Chung, M. Chudzik, R. Hung, N. Yoshida, N. Kim, Applied Materials

**7.4 - 4:40 p.m.**

**Sub-2x10$^{-9}$ Ω-cm$^2$ N- and P-Contact Resistivity with Si:P and Ge:Ga Metastable Alloys for FinFET CMOS Technology,** H. Niimi, Z. Liu*, O. Gluschenkov*, S. Mochizuki*, J. Fronheiser, J. Kim, X. Miao*, J. Li*, J. Demarest*, C. Zhang*, C. Niu, P. Adusumilli*, B. Liu, J. Yang*, V. Kamineni, A. Carr*, M. Raymond, H. Jagannathan*, B. Haran*, V. Paruchuri*, A. Knorr, H. Bu*, T. Yamashita*, GLOBALFOUNDRIES Inc., *IBM Research

**7.5 - 5:05 p.m.**

**Ultra low p-type SiGe Contact Resistance FinFETs with Ti Silicide Liner using Cryogenic Contact Implantation Amorphization and Solid-Phase Epitaxial Regrowth (SPER),** Y. R. Yang, N. Breil*, C. Y. Yang, J. Hsieh, F. Chiang, B. Colombeau*, B. N. Guo**, K. H. Shim**, N. Variam**, G. Leung*, J. Hebb*, S. Sharma*, C. N. Ni*, J. Ren*, J. Wen*, J. H. Park*, H. Chen*, S. Chen***, M. Hou***, D. Tsai***, J. Kuo***, D. Liao***, M. Chudzik*, S. H. Lin, H. F. Huang, N. H. Yang, J. F. Lin, C. T. Tsai, G. C. Hung, S. C. Hsu, O. Cheng, J. Y. Wu, T. R. Yew, United Microelectronics Corp.(UMC), *Applied Materials, **Applied Materials-Varian Semiconductor Equipment, ***Applied Materials Taiwan

Session 8 – Tapa III

## High Density Non Volatile Memory

Tuesday, June 14

Chairpersons: G. Hemink, SanDisk
H. Miyake, Micron Memory Japan, Inc.

**8.1 - 3:25 p.m.**
**Comprehensive Evaluation of Early Retention (fast charge loss within a few seconds) Characteristics in Tube-type 3-D NAND Flash Memory,** B. Choi, S. H. Jang*, J. Yoon, J. Lee, M. Jeon, Y. Lee, J. Han, J. Lee, D. M. Kim, D. H. Kim, C. Lim*, S. Park*, S.-J. Choi, Kookmin University, *SK hynix Inc.

**8.2 - 3:50 p.m.**
**A Monte Carlo Simulation Method to Predict Large-density NAND Product Memory Window from Small-array Test Element Group (TEG) Verified on a 3D NAND Flash Test Chip,** C.-C. Hsieh, H.-T. Lue, T.-H. Hsu, P.-Y. Du, K.-H. Chiang and C.-Y. Lu, Macronix International Co., LTD.

**8.3 - 4:15 p.m.**
**Advanced a-VMCO Resistive Switching Memory through Inner Interface Engineering with Wide (>$10^2$) on/off Window, Tunable μA-range Switching Current and Excellent Variability,** B. Govoreanu*, L. Di Piazza*, J. Ma*, **, ***, T. Conard*, A. Vanleenhove*, A. Belmonte*, D. Radisic*, M. Popovici*, A. Velea*,***, A. Redolfi*, O. Richard*, S. Clima*, C. Adelmann*, H. Bender*, M. Jurczak*, *IMEC, **Liverpool John Moores University, ***KU Leuven

**8.4 - 4:40 p.m.**
**Fully CMOS Compatible 3D Vertical RRAM with Self-aligned Self-selective Cell Enabling Sub-5nm Scaling,** X. Xu, Q. Luo, T. Gong, H. Lv, S. Long, Q. Liu, S. S. Chung*, J. Li**, M. Liu, Institute of Microelectronics of the Chinese Academy of Sciences, *National Chiao Tung University, **University of Wisconsin-Madison

**8.5 - 5:05 p.m.**
**Te-Based Amorphous Binary OTS Device with Excellent Selector Characteristics for X-point Memory Applications,** Y. Koo, K. Baek, H. Hwang, POSTECH

## Technology Panel Sessions

Tuesday, June 14, 8:00 p.m. – 10:00 p.m.

Joint Technology / Circuits Panel Session
Organizers:

| | | | |
|---|---|---|---|
| Technology: | M. Jurczak, ASM | Circuits: | P. Kumar Hanumolu, University of Illinois |
| | W. Rachmady, Intel | | R. Navid, Rambus |
| | T. Tsunomura, TEL | | M. Ito, Renesas |

**PJ-1: "More Moore, More than Moore, or Mo(o)re Slowly"**
Moderator: Subramanian Iyer, University of California, Los Angeles

Over the past 50 years, rapid advancement of fabrication technology has allowed doubling the number of transistors in VLSI components every two years. This trend has continuously enabled new system features that had been previously impractical if not impossible. As a result of this, the growth of the global semiconductor market has been predominantly fueled by technology scaling in what can sometimes be referred to as a "more of the same is good enough" paradigm. As technology scaling slows down, this dynamic is changing and it is unclear what will drive future growth. Is the industry going to continue a

similar path through introduction of new devices and 3D integration? Or is the end of silicon scaling the end of brute force large-scale integration? If that is the case, what is the value of sensor and system integration? Can they generate enough demand to drive growth at a rate comparable to silicon integration? And what is the role of circuit innovation in this environment? One might argue that the "more of the same is good enough" attitude of the past few decades has been a major hindrance for emergence and adoption of many promising ideas at the circuit level? Is the end of scaling a blessing in disguise for the talented circuit designer who would love to tackle a more constrained problem? Renowned experts will attempt to answer these very important questions in this panel.

*Panelists:*

Fari Assadaraghi, NXP Semiconductors
Vivek De, Intel
Nicky Lu, Etron
Gary Patton, GLOBALFOUNDRIES
Thomas Skotnicki, STMicroelectronics
Jan Vardhaman, TechSearch International

Technology Panel Session

**P-2: "How Moore's Law, Industry Consolidation, and System Trends are Shaping the Memory Roadmap?"**

Organizers: M. Jurczak, ASM
W. Rachmady, Intel
T. Tsunomura, Tokyo Electron Ltd.

Moderators: Gary Bronner, Rambus and Fred Chen, Winbond

The roadmap for memory, both DRAM and Flash, has historically been driven by a self-fulfilling prophecy – memory cost must drop 35% / year on a cost per bit basis. Moore's law drove this exponential decrease in cost and increase in memory density for over 3 decades. But the last decade has seen interesting modifications to this historical trend. The emergence of NAND Flash memory led to even faster drops in price, with NAND now 16x cheaper than DRAM on a cost/bit basis. DRAM scaling limits are causing DRAM density improvement to slow and the price gap to widen. NAND Flash continues on a classical price/density roadmap but its performance is not sufficient to replace DRAM. Current systems and applications are facing a "Memory Wall" – cheap Flash bits don't meet CPU performance needs while DRAM bits are no longer cheap enough to meet the capacity needs of multicore CPUs. This has triggered a burst of innovation at all levels – technology, system, and software, creating a myriad of possibilities to be considered.

This panel will debate the technology roadmaps for DRAM, FLASH, SCM (storage class memory) and eNVM (embedded Non Volatile Memory) in light of the fundamental problems around memory cost, performance, and power. Can any of the emerging NVM technologies provide compelling solutions to current computer system and application needs? Which industry will drive the new memory technology - data centers or mobile chip vendors? What memory (or combination of memories) gives the lowest total cost of ownership? How will computer systems handle new levels of memory hierarchy? How does industry consolidation and the emergence of new players in the memory industry affect the roadmap?

These and other questions raised from the audience will be addressed by a distinguished panel of experts from industry. It is a most interesting time to be involved in the memory world!

*Panelists:*

Shekhar Borker, Intel
Takashi Kono, Renesas
Jae-Jin Lee, SK Hynix
Junhee Lim, Samsung
Gurtej Sandhu, Micron
Rob Sprinkle, Google

Session 9 – Tapa II
**Technology Scaling Beyond 10 nm**

Wednesday, June 15
Chairpersons: E. Pop, Stanford University
K. Miyashita, Toshiba Corporation

**9.1 - 10:15 a.m.**
**Demonstration of a sub-0.03 µm² High Density 6-T SRAM with Scaled Bulk FinFETs for Mobile SOC Applications Beyond 10nm Node,** S.-Y. Wu, C. Y. Lin, M. C. Chiang, J. J. Liaw, J. Y. Cheng, C. H. Chang, V. S. Chang, K. H. Pan, C. H. Tsai, C. H. Yao, T. Miyashita, Y. K. Wu, K. C. Ting, C. H. Hsieh, R. F. Tsui, R. Chen, C. L. Yang, H. C. Chang, C. Y. Lee, K. S. Chen, Y. Ku, S. M. Jang, Taiwan Semiconductor Manufacturing Company

**9.2 - 10:40 a.m.**
**First Demonstration of InGaAs/SiGe CMOS Inverters and Dense SRAM Arrays on Si Using Selective Epitaxy and Standard FEOL Processes,** L. Czornomaz, V. Djara, V. Deshpande, E. O'Connor, M. Sousa, D. Caimi, K. Cheng*, J. Fompeyrine, IBM Research Zurich, *IBM Research Albany

**9.3 - 11:05 a.m.**
**Replacement High-*k*/Metal-Gate High-Ge-Content Strained SiGe FinFETs with High Hole Mobility and Excellent SS and Reliability at Aggressive EOT ~7Å and Scaled Dimensions Down to Sub-4nm Fin Widths,** P. Hashemi, T. Ando, K. Balakrishnan, E. Cartier, M. Lofaro, J. A. Ott, J. Bruley, K.-L. Lee, S. Koswatta, S. Dawes, J. Rozen, A. Pyzyna, K. Chan, S. U. Engelmann, D.-G. Park, V. Narayanan, R. T. Mo, E. Leobandung, IBM Research

**9.4 - 11:30 a.m.**
**Zero-thickness Multi Work Function Solutions for N7 bulk FinFETs,** L.-Å. Ragnarsson, H. Dekkers, P. Matagne, T. Schram, T. Conard, N. Horiguchi, A. V.-Y. Thean, IMEC

Session 10 - Tapa III
**Technology/Circuits Joint Focus Session:**

**Smart Power**

Wednesday, June 15
Chairpersons: T. Palacios, Massachusetts Institute of Technology
H. Morioka, Socionext, Inc.

**10.1 – 10:15 a.m.**
**Smart Power Technologies Enabling Power SOC and SIP (Invited),** S. Pendharkar, Texas Instruments

**10.2 – 10:40 a.m.**
**A Dynamic/Static SRAM Power Management Schemes for DVFS and AVS in Automotive Infotainment SoCs (Invited),** K. Nii, M. Yabuuchi, Y. Ishii, M. Tanaka†, M. Igarashi, K. Fukuoka†, and S. Tanaka, Renesas Electronics Corporation, †Renesas System Design Corporation

**10.3 - 11:05 a.m.**
**A Multiple-String Hybrid LED Driver with 97% Power Efficiency and 0.996 Power Factor,** L. Li, Y. Gao, P. Mok, HKUST

**10.4 - 11:30 a.m.**
**A Sine-Reference Band (SRB)-Controlled Average Current Technique for a Phase-Cut Dimmable AC-DC Buck LED Driver without an Electrolytic Capacitor,** C. Shin, W. Lee*, S. W. Lee*, B. Jeong*, J. Lee*, U. Jang*, Y. G. Kim*, S. H. Lee, J. S. Bang, G. H. Cho, KAIST, *Silicon Works

Session 11 – Tapa II
**Technology/Circuits Joint Focus Session:**
**Analog / RF Integration and DTCO in CMOS**

Wednesday, June 15
Chairpersons: G. Yeric, ARM
Y.-C. Yeo, TSMC

**11.1 – 1:15 p.m.**
**Overcoming Scaling Barriers through Design Technology CoOptimization (Invited),** L. Liebmann, J. Zeng, X. Zhu, L. Yuan, G. Bouche, J. Kye, GLOBALFOUNDRIES

**11.2 – 1:40 p.m.**
**Analog/RF Wonderland: Circuits and Technology Co-optimization in Advanced FinFET Technology (Invited),** F.-L. Hsueh, Y-C Peng, C-H Chen, T-J Yeh, H-H Hsieh, C-H Chang, S-L Liu, M-C Chuang, M. Chen, Taiwan Semiconductor Manufacturing Company, Ltd.

**11.3 - 2:05 p.m.**
**200-280GHz CMOS RF Front-End of Transmitter for Rotational Spectroscopy,** N. Sharma, Q. Zhong, Z. Chen, W. Choi, J. P. McMillan*, C. F. Neese*, R. Schueler**, I. Medvedev**, F. De Lucia*, K. O, The University of Texas at Dallas, * Ohio State University, ** Wright State University

**11.4 - 2:30 p.m.**
**Broadband THz Spectroscopic Imaging based on a Fully Integrated 4×2 Digital-to-Impulse Radiating Array with a Full-Spectrum of 0.03-1.03THz in Silicon,** M. Mahdi Assefzadeh, A. Babakhani, Rice University

Session 12 – Tapa III
**Emerging Memory Technology (RRAM and PCM)**

Wednesday, June 15
Chairpersons: M. Jurczak, ASM
B.-H. Lee, Gwangju Institute of Science and Technology

**12.1 - 1:15 p.m.**
**RTN-based Defect Tracking Technique: Experimentally Probing the Spatial and Energy profile of the Critical Filament Region and its Correlation with $HfO_2$ RRAM Switching Operation and Failure Mechanism,** Z. Chai*, J. Ma*, W. Zhang*, B. Govoreanu**, E. Simoen**, J. F. Zhang*, Z. Ji*, R. Gao*, G. Groeseneken**, M. Jurczak**, *Dept. of Electronics & Electr. Eng., Liverpool John Moores University, **IMEC

**12.2 - 1:40 p.m.**
**Robust Cu Atom Switch with over-400°C Thermally Tolerant Polymer-solid Electrolyte (TT-PSE) for Nonvolatile Programmable Logic,** K. Okamoto, M. Tada, N. Banno, N. Iguchi, H. Hada, T. Sakamoto, M. Miyamura, Y. Tsuji, R. Nebashi, A. Morioka, X. Bai, T. Sugibayashi, NEC Corporation

**12.3 - 2:05 p.m.**
**Retention, Disturb and Variability improvements enabled by local Chemical-potential Tuning and controlled Hour-Glass filament shape in a novel W\$WO_3$\$Al_2O_3$\Cu CBRAM,** L. Goux*, A. Belmonte*,**, U. Celano*,**, J. Woo*, S. Folkersma*, C. Y. Chen*,**, A. Redolfi*, A. Fantini*, R. Degraeve*, S. Clima*, W. Vandervorst*,**, M. Jurczak*, *IMEC, **KU Leuven

**12.4 - 2:30 p.m.**
**A Novel Low Power Phase Change Memory Using Inter-Granular Switching,** H. L. Lung*, Y.H. Ho*, Y. Zhu**, W.C. Chien*, S. Kim**, W. Kim**, H.Y. Cheng*, A. Ray**, M. Brightsky** R. Bruce**, C.W. Yeh*, and C. Lam**, Macronix International Co., Ltd.*, IBM T. J. Watson Research Center*

Session 13 – Tapa II
**FDSOI and III-V Devices**

Wednesday, June 15
Chairpersons: C. Mazure, Soitec Group
S. Takagi, The University of Tokyo

**13.1 - 2:55 p.m.**

**Smart Solutions for Efficient Dual Strain Integration for Future FDSOI Generations,** A. Bonnevialle**,*,***, C. Le Royer*, Y. Morand**, S. Reboh*, C. Plantier*, N. Rambal*, J.-P. Pédini**, S. Kerdiles*, P. Besson*,**, J.-M. Hartmann*, D. Marseilhan*, B. Mathieu*, R. Berthelon*,**, M. Cassé*, F. Andrieu*, D. Rouchon*, O. Weber*, F. Bœuf**, M. Haond**, A. Claverie***, M. Vinet*, *CEA LETI, **STMicroelectronics, ***CEMES-CNRS

**13.2 - 3:20 p.m.**
**High Performance CMOS FDSOI Devices Activated at Low Temperature,** L. Pasini*, **, ***, P. Batude*, J. Lacord*, M. Casse*, B. Mathieu*, B. Sklenard*, F. Piegas Luce*, J. Micout*, ***, F. Mazen*, P. Besson*, E. Ghegin*, **, J. Borrel*, **, R. Daubriac♦, L. Hutin*, D. Blachier*, D. Barge**, S. Chhun**, A. Cros**, G. Ghibaudo***, J.-P. Barnes*, Z. Saghi*, V. Delaye*, N. Rambal*, V. Lapras*, J. Mazurier*, O. Weber*, F. Andrieu*, C. Fenouillet-Beranger*, Q. Rafhay***,G. Ghibadeau*** F. Cristiano♦, M. Haond**, F. Bœuf**, M. Vinet*, *CEA LETI, **STMicroelectronics, ***IMEP-LAHC, ♦LAAS-CNRS

**13.3 - 3:45 p.m.**
**High Aspect Ratio InGaAs FinFETs with Sub-20 nm Fin Width,** A. Vardi, J. Lin, W. Lu, X. Zhao and J. A. del Alamo, Massachusetts Institute of Technology

**13.4 - 4:10 p.m.**
**Junctionless Gate-All-Around Lateral and Vertical Nanowire FETs with Simplified Processing for Advanced Logic and Analog/RF Applications and Scaled SRAM Cells,** A. Veloso*, B. Parvais*, P. Matagne*, E. Simoen*, T. Huynh-Bao*, **, V. Paraschiv*, E. Vecchio*, K. Devriendt*, E. Rosseel*, M. Ercken*, B. T. Chan*, C. Delvaux*, E. Altamirano-Sánchez*, J. J. Versluijs*, Z. Tao*, S. Suhard*, S. Brus*, A. Sibaja-Hernandez*, N. Waldron*, P. Lagrain*, O. Richard*, H. Bender*, A. Chasin*, B. Kaczer*, T. Ivanov*, S. Ramesh*, ***, K. De Meyer*, ***, J. Ryckaert*, N. Collaert*, A. Thean*, *Imec, **Vrije Universiteit Brussel, ***KU Leuven

**13.5 - 4:35 p.m.**
**Record Mobility ($\mu_{eff}$ ~3100 cm$^2$/V-s) and Reliability Performance ($V_{ov}$~0.5V for 10yr Operation) of $In_{0.53}Ga_{0.47}As$ MOS Devices Using Improved Surface Preparation and a Novel Interfacial Layer,** A. Vais*,**, A. Alian*, L. Nyns*, J. Franco*, S. Sioncke*, V. Putcha*, **, H. Yu*, **, Y. Mols*, R. Rooyackers*, D. Lin*, J.W. Maes*, ***, Q. Xie*, ***, M. Givens*, ♦, F. Tang*, ♦, X. Jiang*, ♦, A. Mocuta*, N. Collaert*, K. De Meyer*, **, A. Thean*, *IMEC, **KULeuven, ***ASM Belgium, ♦ASM, AZ, USA

Session 14 – Tapa III
**STT-MRAM and Ferroelectric Memories**

Wednesday, June 15
Chairpersons: K. Baker, Freescale NXP
S.-W. Chung, SK Hynix Semiconductors, Inc.

**14.1 - 2:55 p.m.**
**Reliability Study of Perpendicular STT-MRAM as Emerging Embedded Memory Qualified for Reflow Soldering at 260°C,** M.-C. Shih, C.-Y. Wang, Y.-H. Lee, W. Wang, L. Thomas*, H. Liu*, J. Zhu*, Y.-J. Lee*, G. Jan*, Y.-J. Wang*, T. Zhong*, T. Torng*, P.-K. Wang*, D. Lin, T.-W. Chiang, K.-H. Shen, H. Chuang, W. J. Gallagher, Taiwan Semiconductor Manifacturing Company, TDK-Headway Technologies, Inc.

**14.2 - 3:20 p.m.**
**Sub-3 ns Pulse with Sub-100 µA Switching of 1x-2x nm Perpendicular MTJ for High-performance Embedded STT-MRAM Towards sub-20 nm CMOS,** D. Saida*, S. Kashiwada*, M. Yakabe*, T. Daibou*, N. Hase*, M. Fukumoto**, S. Miwa**, Y. Suzuki**, H. Noguchi*, S. Fujita*, J. Ito*, *Toshiba Corp., **Osaka University

**14.3 - 3:45 p.m.**
**First Demonstration and Performance Improvement of Ferroelectric $HfO_2$-based Resistive Switch with Low Operation Current and Intrinsic Diode Property,** S. Fujii, Y. Kamimuta, T. Ino, Y. Nakasaki, R. Takaishi, M. Saitoh, Toshiba Corporation

**14.4 - 4:10 p.m.**
**One-Transistor Ferroelectric Versatile Memory: Strained-Gate Engineering for Realizing Energy-Efficient Switching and Fast Negative-Capacitance Operation,** Y.-C. Chiu*, C.-H. Cheng**, C.-Y. Chang*,♦, Y.-T. Tang***, M.-C. Chen***, *National Chiao-Tung University, **National Taiwan Normal University, ***National Nano Device Laboratories, ♦Research Center for Applied Sciences, Academia Sinica

**14.5 - 4:35 p.m.**
**Study of Wake-up and Fatigue Properties in Doped and Undoped Ferroelectric $HfO_2$ in Conjunction with Piezo-Response Force Microscopy Analysis,** S. Shibayama*, **, L. Xu*, S. Migita***, A. Toriumi*, *The University of Tokyo, **JSPS research fellow PD, ***AIST

**Executive Panel Discussion**

Wednesday, June 15, 6:00 p.m. – 7:00 p.m.

Chairs: Raj Jammy, Carl Zeiss
Satoshi Inaba, Toshiba Electronics Korea Corporation

**Semiconductor Business: Inflections Beyond Scaling**
Moderator: Dan Hutcheson, CEO and Chairman of VLSI Research Inc and author of The Chip Insider

As semiconductor industry approaches seemingly finite limits of physical scaling, a number of inflections are unfolding around us that may require us to rethink how we design, develop and manufacture semiconductor devices. Sensing, positioning, energy-aware and predictive systems are becoming the norm, opening up wider applications and enormous growth potential for semiconductor industry. Yet, implementation of such technologies from research to reality also poses technical and business challenges. Such systems require ultra-low power, always-on sensing, connectivity, vast embedded and discrete memory, smart energy sources and management - all wrapped in to ever smaller form factors. IoT, self-driving automobiles, next generation 5G networks, machine learning, brain-inspired computing, virtual/immersive reality and many other emerging trends will also need large investments for successful deployment and business models for ROI. The cost of developing such technologies, acceptable standards,

security protocols, inter-platform operability, etc., will need unprecedented collaboration in the industry. The panel will deliberate on these topics and discuss trends, applications that are shaping around us, industry needs, infrastructural/manufacturing gaps and economic challenges.

Panelists:

Mike Cadigan, Senior Vice President, Global Sales and Business Development, GLOBALFOUNDRIES
Tze-Chiang Chen, IBM Fellow, IBM TJ Watson Research Center, IBM
SungJoo Hong, EVP and Head of R&D, SK Hynix
Steve Lloyd, Vice President, Engineering and New Product Development, InvenSense
Marie-Noelle Semaria, CEO, CEA LETI

Session 15 – Tapa II
**Gate All Around and III-V Devices**

Thursday, June 16
Chairpersons: W. Maszara, GLOBALFOUNDRIES
K. Endo, AIST

**15.1 - 8:05 a.m.**
**Gate-All-Around MOSFETs based on Vertically Stacked Horizontal Si Nanowires in a Replacement Metal Gate Process on Bulk Si Substrates,** H. Mertens, R. Ritzenthaler, A. Hikavyy, M. S. Kim, Z. Tao, K. Wostyn, S. A. Chew, A. De Keersgieter, G. Mannaert, E. Rosseel, T. Schram, K. Devriendt, D. Tsvetanova, H. Dekkers, S. Demuynck, A. Chasin, E. Van Besien, A. Dangol, S. Godny, B. Douhard, N. Bosman, O. Richard, J. Geypen, H. Bender, K. Barla, D. Mocuta, N. Horiguchi, A. V.-Y. Thean, IMEC

**15.2 - 8:30 a.m.**
**InAs Nanowire GAA n-MOSFETs with 12-15 nm Diameter,** T. Vasen, P. Ramvall, A. Afzalian, C. Thelander*, K. A. Dick*, M. Holland, G. Doornbos, S. W. Wang, R. Oxland, G. Vellianitis, M. J. H. van Dal, B. Duriez, J.-R. Ramirez**, R. Droopad**, L.-E. Wernersson*, L. Samuelson*, T.-K. Chen***, Y.-C. Yeo***, M. Passlack, TSMC Europe, *Lund Univeristy, **Texas State University, ***TSMC

**15.3 - 8:55 a.m.**
**InGaAs Nanowire MOSFETs with $I_{ON}$ = 555 µA/µm at $I_{OFF}$ = 100 nA/µm and $V_{DD}$ = 0.5 V,** C. B. Zota, F. Lindelöw, L.-E. Wernersson, E. Lind, Lund University

**15.4 - 9:20 a.m.**
**Top-down InGaAs Nanowire and Fin Vertical FETs with Record Performance,** S. Ramesh*, **, Ts. Ivanov**, E. Camerotto***, N. Sun♦, J. Franco**, A. Sibaja-Hernandez**, R. Rooyackers**, A. Alian**, J. Loo**, A. Veloso**, A. Milenin**, D. Lin**, P. Favia**, H. Bender**, N. Collaert**, A. V-Y. Thean**, K. De Meyer*, **, *IMEC, **KU Leuven, ***Lam Research Belgium, ♦Lam Research Corp. Fremont

**15.5 - 9:45 a.m.**

**Scalability of InGaAs Gate-All-Around FET Integrated on 300mm Si Platform: Demonstration of Channel Width down to 7nm and Lg down to 36nm,** X. Zhou*, N. Waldron*, G. Boccardi*, F. Sebaai*, C. Merckling*, G. Eneman*, S. Sioncke*, L. Nyns*, A. Opdebeeck*, J. W. Maes**, Q. Xie**, M. Givens***, F. Tang***, X. Jiang***, W. Guo*, B. Kunert*, L. Teugels*, K. Devriendt*, A. Sibaja Hernandez*, J. Franco*, D. van Dorp*, K. Barla*, N. Collaert*, A. V.-Y. Thean*, *IMEC, **ASM Belgium, ***ASM America

Session 16 – Tapa III
**Variability and Design Technology Co-Optimization**

Thursday, June 16
Chairpersons: L. Bair, AMD
N. Sugii, Hitachi, Ltd.

**16.1 - 8:05 a.m.**
**RTN and Low Frequency Noise on Ultra-scaled Near-ballistic Ge Nanowire nMOSFETs,** W. Wu*, **, ***, H. Wu*, M. Si*, N. Conrad*, Y. Zhao**, ***, P. D. Ye*, *Purdue University, **Nanjing University, ***Zhejiang University

**16.2 - 8:30 a.m.**
**Statistical Limits of Contact Resistivity Due to Atomistic Variation in Nanoscale Contacts,** G. Shine, C. E. Weber*, K. C. Saraswat, Stanford University, *Intel Corporation

**16.3 - 8:55 a.m.**
**Variability-aware TCAD Based Design-Technology Co-Optimization Platform for 7nm Node Nanowire and Beyond,** Y. Wang*, B. Cheng**, X. Wang***, E. Towie**, C. Riddet**, A. R. Brown**, S. M. Amoroso**, L. Wang***, D. Reid**, X. Liu*, J. Kang*, A. Asenov**, ***, *Peking University, **Gold Standard Simulations Ltd., ***University of Glasgow

**16.4 - 9:20 a.m.**
**Random Telegraph Noise (RTN) in 14nm Logic Technology: High Volume Data Extraction and Analysis,** S. Dongaonkar, M. D. Giles*, A. Kornfeld, B. Grossnickle, J. Yoon, Advanced Design, *Logic Technology Development, Intel Corporation

**16.5 - 9:45 a.m.**
**Design / Technology Co-optimization of Strain-Induced Layout Effects in 14nm UTBB-FDSOI CMOS: Enablement and Assessment of Continuous-RX Designs,** R. Berthelon*, F. Andrieu*, **, E. Josse*, R. Bingert*, O. Weber*, **, E. Serret*, A. Aurand*, S. Delmedico*, V. Farys*, C. Bernicot*, E. Bechet*, E. Bernard*, T. Poiroux*, **, D. Rideau*, P. Scheer*, E. Baylac*, P. Perreau*, **, M.-A. Jaud*, **, J. Lacord*, **, E. Petitprez*, A. Pofelski*, S. Ortolland*, P. Sardin*, D. Dutartre*, A. Claverie*, ***, M. Vinet*, **, J. C. Marin*, M. Haond*, *STMicroelectronics, **CEA-LETI, ***CEMES

Session 17 – Tapa II
**Technology Focus Session:**
**Interconnect and 3D Integration**

Thursday, June 16
Chairpersons: W. Rachmady, Intel Corporation
M. Tada, NEC Corporation

**17.1 – 10:25 a.m.**
**On-chip Interconnect Trends, Challenges and Solutions: How to Keep RC and Reliability Under Control (Invited),** Z. Tőkei, I. Ciofi, Ph. Roussel, P. Debacker, P. Raghavan, M. van der Veen, N. Jourdan, C. Wilson, V.V. Gonzalez, C. Adelmann, L. Wen, K. Croes, K. Moors, M. Krishtab, S. Armini, J. Boemmels, IMEC

**17.2 – 10:50 a.m.**
**Production-Worthy WOW 3D Integration Technology using Bumpless Interconnects and Ultra-Thinning Processes (Invited),** T. Ohba, Tokyo Institute of Technology

**17.3 - 11:15 a.m.**
**First Demonstration of a CMOS Over CMOS 3D VLSI CoolCube™ Integration on 300mm Wafers,** L. Brunet*, P. Batude*, C. Fenouillet-Beranger*, P. Besombes*, L. Hortemel*, F. Ponthenier*, B. Previtali*, C. Tabone*, A. Royer*, C. Agraffeil*, C. Euvrard-Colnat**, A. Seignard*, C. Morales*, F. Fournel*, L. Benaissa*, T. Signamarcheix*, P. Besson**, M. Jourdan*, R. Kachtouli*, V. Benevent*, J.-M. Hartmann*, C. Comboroure**, N. Allouti*, N. Posseme*, C. Vizioz*, C. Arvet**, S. Barnola*, S. Kerdiles*, L. Baud*, L. Pasini*, **, C.-M. V. Lu*, **, F. Deprat*, A. Toffoli*, G. Romano**, C. Guedj*, V. Delaye*, F. Boeuf**, O. Faynot*, M. Vinet*, *CEA LETI, **STMicroelectronics

**17.4 - 11:40 a.m.**
**A Highly Scalable Poly-Si Junctionless FETs Featuring a Novel Multi-Stacking Hybrid P/N Layer and Vertical Gate with Very High Ion/Ioff for 3D Stacked ICs,** Y.-C. Cheng*, **, H.-B. Chen**, C.-Y. Chang**, ♦, C.-H. Cheng***, Y.-J. Shih**, Y.-C. Wu*, *National Tsing Hua University, **National Chiao-Tung University, ***National Taiwan Normal University, ♦Academia Scienica

Session 18 – Tapa III
**Non Volatile Memories and Applications**

Thursday, June 16
Chairpersons: M. Vinet, CEA-LETI, MINATEC
H.-T. Lue, Macronix International Co., Ltd.

**18.1 – 10.25 a.m.**
**Direct Three-dimensional Observation of the Conduction in Poly-Si and $In_{1-x}Ga_xAs$ 3D NAND Vertical Channels,** U. Celano*, E. Capogreco*, **, J.G. Lisoni*, ***, A. Arreghini*, B. Kunert*, W. Guo*, G. Van den Bosch*, J. Van Houdt*, **, K. De Meyer*, **, A. Furnemont*, W. Vandervorst*, **, *IMEC, **KU Leuven, ***Universidad Austral de Chile

**18.2 - 10:50 a.m.**

**Four-Layer 3D Vertical RRAM Integrated with FinFET as a Versatile Computing Unit for Brain-Inspired Cognitive Information Processing,** H. Li, K.-S. Li*, C.-H. Lin*, J.-L. Hsu*, W.-C. Chiu*, M.-C. Chen*, T.-T. Wu*, J. Sohn, S. Burc Eryilmaz, J.-M. Shieh*, W.-K. Yeh*, H.-S. Philip Wong, Stanford University, *National Nano Device Laboratories

**18.3 - 11:15 a.m.**
**Novel RRAM-enabled 1T1R Synapse Capable of Low-power STDP via Burst-mode Communication and Real-time Unsupervised Machine Learning,** S. Ambrogio, S. Balatti, V. Milo, R. Carboni, Z. Wang, A. Calderoni*, N. Ramaswamy*, D. Ielmini, Politecnico di Milano, *Micron Technology Inc. Boise

**18.4 - 11:40 a.m.**
**A ReRAM-based Physically Unclonable Function with Bit Error Rate < 0.5% after 10 years at 125˚C for 40nm Embedded Application,** Y. Yoshimoto, Y. Katoh, S. Ogasahara, Z. Wei, K. Kouno, Panasonic Semiconductor Solutions Corporation

## Luncheon Talk

Thursday, June 16, 12:15 p.m. – 1:30 p.m.

**Cyborg insects and other things: building interfaces between the synthetic and the multicellular**

As the computation and communication circuits we build radically miniaturize (i.e. become so low power that 1 pJ is sufficient to bang out a bit of information over a wireless transceiver; become so small that 500 µm^2 of thinned CMOS can hold a reasonable sensor front-end and digital engine), the barrier to introducing these types of interfaces into organisms will get pretty low. Put another way, the rapid pace of computation and communication miniaturization is swiftly blurring the line between the technological base that created us and the technological based we've created. In this talk, I'll give an overview of recent work in my lab that touches on this concern. Most of the talk will cover our ongoing exploration of the remote control of insects in free flight via implantable radio-equipped miniature neural stimulating systems.; recent results with pupally-implanted neural interfaces and extreme miniaturization directions will be discussed. If time permits, I will show recent results building extremely small neural interfaces we call "neural dust," work done in collaboration with the Carmena, Alon and Rabaey labs.

Biography: Michel M. Maharbiz is an Associate Professor with the Department of Electrical Engineering and Computer Science at the University of California, Berkeley.

He received his Ph.D. from the University of California at Berkeley under Professor Roger T. Howe (EECS) and Professor Jay D. Keasling (ChemE); his work led to the foundation of Microreactor Technologies, Inc. which was acquired in 2009 by Pall Corporation. From 2003 to 2007, Michel Maharbiz was an Assistant Professor at the University of Michigan, Ann Arbor. He is the co-founder of Tweedle Technologies, Cortera Neurotech and served as vice-president for product development at Quswami, Inc. from July 2010 to June 2011.

Prof. Maharbiz is a Bakar Fellow and was the recipient of a 2009 NSF Career Award for research into developing microfabricated interfaces for synthetic biology. His group is also known for developing the

world's first remotely radio-controlled cyborg beetles. This was named one of the top ten emerging technologies of 2009 by MIT's Technology Review (TR10) and was in Time Magazine's Top 50 Inventions of 2009. Dr. Maharbiz has been a GE Scholar and an Intel IMAP Fellow. Professor Maharbiz's current research interests include building micro/nano interfaces to cells and organisms and exploring bio-derived fabrication methods. Michel's long term goal is understanding developmental mechanisms as a way to engineer and fabricate machines."

## Session 19 – Tapa II
## **High-K Metal Gate Variability and Scaling**

Thursday, June 16
Chairpersons: A. Ionescu, Swiss Federal Institute of Technology
T. Tsunomura, Tokyo Electron Ltd.

**19.1 - 1:30 p.m.**
**Gate Stack Solutions in Gate-First FDSOI Technology to meet High Performance, Low Leakage, $V_T$ centering and Reliability Criteria,** O. Weber*, E. Josse, X. Garros*, M. Rafik, X. Federspiel, C. Diouf*, A. Toffoli*, S. Zoll, O. Gourhant, V. Joseph, C. Suarez-Segovia, F. Domengie, V. Beugin*, B. Saidi, M. Gros-Jean, P. Perreau*, J. Mazurier*, E. Richard, M. Haond, STMicroelectronics, *CEA-LETI

**19.2 - 1:55 p.m.**
**A New Variation Plot to Examine the Interfacial-dipole Induced Work-function Variation in Advanced High-*k* Metal-gate CMOS Devices,** E. R. Hsieh, Y. D. Wang, S. S. Chung, J. C. Ke*, C. W. Yang*, S. Hsu*, National Chiao Tung University, *UMC

**19.3 - 2:20 p.m.**
**Novel N/PFET Vt control by TiN Plasma Nitridation for Aggressive Gate Scaling,** M. Togo, W. H. Tong, X. Zhang, D. H. Triyoso, J. Lian, Y. Mamy Randriamihja, S. Uppal, S. Dag, E. C. Silva, M. Kota, T. Shimizu, S. Patil, M. Eller, S. Samavedam, GLOBALFOUNDRIES

**19.4 - 2:45 p.m.**
**Complete Extraction of Defect Bands Responsible for Instabilities in n and pFinFETs,** G. Rzepa, M. Waltl, W. Goes, B. Kaczer*, J. Franco*, T. Chiarella*, N. Horiguchi*, T. Grasser, TU Wien, *IMEC

## Session 20 – Tapa III
## **Sensor Technology and Microsystems for IoT**

Thursday, June 16
Chairpersons: B.K. Liew, nVidia
S. Yamakawa, Sony Corporation

**20.1 - 1:30 p.m.**

**Low-Power, High-Performance S-NDR Oscillators for Stereo (3D) Vision using Directly-Coupled Oscillator Networks,** A. A. Sharma, Y. Kesim, M. Shulaker*, C. Kuo**, C. Augustine**, H. S.-P. Wong*, S. Mitra*, M. Skowronski, J. A. Bain, J. A. Weldon, Carnegie Mellon University, *Stanford University **Intel Corporation

**20.2 - 1:55 p.m.**
**Ultra Low Power Coupled Oscillator Arrays for Computer Vision Applications,** N. Shukla*, **, W.-Y. Tsai**, M. Jerry*, M. Barth**, V. Narayanan**, S. Datta*, **, *University of Notre Dame, **Pennsylvania State University

**20.3 - 2:20 p.m.**
**A 512×576 65-nm CMOS ISFET Sensor for Food Safety Screening with 123.8 mV/pH Sensitivity and 0.01 pH Resolution,** Y. Jiang, X. Liu, T. C. Dang, M. Yan*, H. Yu, J.-C. Huang**, C.-H. Hsieh**, T.-T. Chen**, Nanyang Technological University, *Illumina Inc., **TSMC

**20.4 - 2:45 p.m.**
**Integration of Neural Sensing Microsystem with TSV-embedded Dissolvable μ-Needles Array, Biocompatible Flexible Interposer, and Neural Recording Circuits,** Y.-C. Huang, Y.-C. Hu, P.-T. Huang, S.-L. Wu, Y.-H. You, J.-M. Chen, Y.-Y. Huang, H.-C. Chang, Y.-H. Lin, J.-R. Duann*, T.-W. Chiu, W. Hwang, C.-T. Chuang, J.-C. Chiou, K.-N. Chen, National Chiao Tung University, *China Medical University

## Session 21 – Tapa II
## **Steep Sub-Threshold Devices**

Thursday, June 16
Chairpersons: S. Salahuddin, University of California, Berkeley
M. Kobayashi, The University of Tokyo

**21.1 - 3:25 p.m.**
**Enabling High-Performance Heterogeneous TFET/CMOS Logic with Novel Circuits Using TFET Unidirectionality and Low-$V_{DD}$ Operation,** D. H. Morris, K. Vaidyanathan, U. E. Avci, H. Liu, T. Karnik, I. A. Young, Intel Corporation

**21.2 - 3:50 p.m.**
**Performance improvement of $In_xGa_{1-x}As$ Tunnel FETs with Quantum Well and EOT scaling,** D. H. Ahn, S. M. Ji, M. Takenaka, S. Takagi, The university of Tokyo, JST CREST

**21.3 - 4:15 p.m.**
**Complementary III-V Heterojunction Lateral NW Tunnel FET Technology on Si,** D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky, H. Riel, IBM Research Zurich

**21.4 - 4:40 p.m.**
**Phase-transition-FET Exhibiting Steep Switching Slope of 8mV/decade and 36% Enhanced ON Current,** J. Frougier*, N. Shukla**, D. Deng*, M. Jerry**, A. Aziz*, L. Liu*, G. Lavallee*, T. S. Mayer*, S. Gupta*, S. Datta*, **, *The Pennsylvania State University, **University of Notre-Dame

**21.5 - 5:05 p.m.**

**Circuit Performance Analysis of Negative Capacitance FinFETs,** S. Khandelwal, A. I. Khan, J. P. Duarte, A. B. Sachid, S. Salahuddin, C. Hu, University of California, Berkeley

Session 22 – Tapa III
**CMOS Image Sensors**

Thursday, June 16
Chairpersons: K. Benaissa, Texas Instruments
T. Tanaka, Tohoku University

**22.1 - 3:25 p.m.**
**White Spots Reduction by Ultimate Proximity Metal Gettering at Carbon Complexes Formed underneath Contact Area in CMOS Image Sensors,** T. Yamaguchi, T. Yamashita, T. Kamino*, Y. Goto*, T. Kuroi*, M. Matsuura, Renesas Electronics Corporation, *Renesas Semiconductor Manufacturing Corporation

**22.2 - 3:50 p.m.**
**Enabling Monolithic 3D Image Sensor Using Large-area Monolayer Transition Metal Dichalcogenide and Logic/Memory Hybrid 3D$^{+}$IC,** C.-C. Yang, K.-C. Chiu*, C.-T. Chou*, C.-N. Liao*, M.-H. Chuang*, T.-Y. Hsieh, W.-H. Huang, C.-H. Shen, J.-M. Shieh, W.-K. Yeh, Y.-H. Chen*, M.-C. Wu*, Y.-H. Lee*, National Nano Device Laboratories, * National Tsing Hua University

**22.3 - 4:15 p.m.**
**Germanium-Tin Heterojunction Phototransistor: Towards High-Efficiency Low-Power Photodetection in Short-Wave Infrared Range,** W. Wang, Y. Dong, S. Y. Lee*, W. K. Loke*, X. Gong, S. F. Yoon*, G. Liang, Y.-C. Yeo, National University of Singapore, *Nanyang Technological University

**22.4 - 4:40 p.m.**
**Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF,** H. Takahashi, H. Tanaka, M. Oda, M. Ando, N. Niisoe, S. Kawai*, T. Asano*, M. Sudo*, M. Yoshita*, T. Yamada*, TowerJazz Panasonic Semiconductor Co., Ltd., *Panasonic Semiconductor Solutions Co., Ltd.

**22.5 - 5:05 p.m.**
**Back-illuminated Voltage-domain Global Shutter CMOS Image Sensor with 3.75µm Pixels and Dual In-pixel Storage Nodes,** L. Stark*, **, J. M. Raynor**, F. Lalanne**, R. K. Henderson*, *University of Edinburgh, **STMicroelectronics