2017 SYMPOSIA ON VLSI TECHNOLOGY & CIRCUITS

Semiconductor industry's premier event on advances in microelectronics technology & circuits

RIHGA Royal Hotel
KYOTO
June 5-8, 2017


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2017 VLSI SYMPOSIA THEME
Harmonious Integration toward Next Dimensions

In 2017, for the first time, both Symposia on VLSI Technology and Circuits will be fully overlapped to showcase "Harmonious integration" of Circuits and Technology, and will start on Monday June 5 at the same location. A single registration allows participants to attend both Symposia. The 2017 Symposia feature not only Joint Circuits and Technology Focus Sessions, Joint Evening Panels, but also various Short Courses, and a new Joint Demo Session.

SYMPOSIUM ON VLSI TECHNOLOGY

SYMPOSIUM ON VLSI CIRCUITS

PLENARY PRESENTATIONS

Tuesday morning, June 6

5G and it's surrounding situations until 2020
– Takashi Tsutsui, SVP & Chief Scientist, SoftBank Corp.

Internet of Thing (IoT) (TBD)
– Fari Assaderaghi, CTO & SVP, NXP Semiconductors

Innovative Solutions towards the Society Which AI, Robotics, IoT Lead Us to, and Expectation for VLSI
– Takeshi Yukitake, CTO, Connected Solutions Company, Panasonic Corporation

Inside Waymo's Self-Driving Car: My Favorite Transistors
– Daniel Rosenband, Google

EVENING PANEL DISCUSSION

Tuesday evening, June 6

Transistor Future; How Does it Evolve after FinFET Era?

Moderator: Jason Woo, UCLA

Affiliations of expected panelists: Experts from GLOBALFOUNDRIES, Qualcomm, imec, IBM, SOITEC, etc.

Although electrical characteristics are improved with alternative transistor structures like nanosheet or nanowire, size scaling will approach physical limitation. Adopting 3D structures is one of ways to maintain "equivalent size scaling". In this panel discussion, future roadmap of FET will be discussed by 1D, 2D, and 3D FET experts.

TECHNOLOGY FOCUS SESSIONS

1D and 2D Atomic Thin Materials and Devices
Emerging Memory Technology

JOINT PROGRAM HIGHLIGHTS

Demo Session NEW!!

Monday evening, June 5

Newly established venue for in-depth discussion with authors:

- Demonstration of chip operation highlighting key results
- Systems showcasing potential applications for circuit-level innovations
- Table-top real-time demonstration of new device characterization
- Visual illustration of technological concepts and analyses

JOINT FOCUS SESSIONS

Wednesday, June 7 & Thursday, June 8

Joint Circuits and Technology Focus Sessions will be offered in the following special topics of joint interest:

- Design in scaled technologies for IoT and ULP
- New Computing: Artificial intelligence, beyond von neumann computing
- Embedded memory and emerging memory technology and design
- 3D and heterogeneous integration
- Design enablement

JOINT EVENING PANEL DISCUSSION

Tuesday evening, June 6

How will We Survive the Post-Scaling Era?

We are approaching the biggest challenge yet in our industry. What happens when technology scaling stops? This panel will discuss different aspects of how we can innovate in such circumstances - from fab perspective, from design/architecture perspective and how we can continue to offer value to end-customers.

- Moderator: Ted Letavic, GLOBALFOUNDRIES
- Affiliations of expected panelists: Experts from ARM, IBM, Huawei, STMicroelectronics, imec, etc.

LUNCHEON
Thursday, June 8

JOINT RECEPTION
Monday, June 5

JOINT BANQUET
Wednesday, June 7

EVENING PANEL DISCUSSION

Tuesday morning, June 6

The Most Important Circuits of 2037
What kinds of VLSI circuits will be presented, and for what kind of applications, at the 2037 Symposium (20 years later from now)?

Moderator: Kofi Makinwa, TU Delft

Panelists: James Myers/ARM, Pieter Harpe/Eindhoven Univ. of Technology, Hirotaka Tamura/Fujitsu, Chintan Thakkar/Intel, Jerald Yoo/National University of Singapore, Koichi Nose/Renesas, Kevin Zhang/TSMC, etc.

30 YEARS ANNIVERSARY PARTY

Tuesday evening, June 6

TECHNOLOGY SHORT COURSE

Technology Enablers for 5nm and Next Wave of Integration

Monday, June 5

This Short course features key technologies of 5nm node and new integration scheme of 3D, memory and analog devices.

1. CMOS Device Technology Enablers and Challenges for 5nm, Pouya Hashemi, and Terence B. Hook, IBM Research
2. Heterogeneous integration of Ge, III-V, and 2D on Si – from More Moore to Beyond CMOS –, Mitsuru Takenaka, University of Tokyo
3. Design & Technology co-optimization for High Performance Mobile SoC, Paul Penzes, Qualcomm
4. The Duality of Interconnect Scaling in sub-10nm Technology Nodes: Increasingly Complex, Increasingly Important, Robert Fox, GLOBALFOUNDRIES
5. Heterogeneous 3D/2.5D Integration toward IoT and AI era, Mitsumasa Koyanagi, Tohoku University
6. Device Challenges for Scaled Analog/RF, Fu-Lung Hsueh, TSMC
7. Embedded Memory Design Differentiates Microcontroller Solutions, Thomas Jew, NXP
8. On Die Processing In Memory, Fabrice Devaux, uPmem

CIRCUITS SHORT COURSE

Integrated Circuits for Smart Connected Cars and Automated Driving

Monday, June 5

The course demystifies recent advances in automotive electronics covering wireless/wireline communication, powertrain, and various sensors from the fundamentals to future trend.

1. An Overview of Automotive Electronics, Christoph Lang, Bosch
2. Intra-Vehicle Wireline Networks, Alexander Tan, Marvell
3. Image Sensors for Automotive Applications, Shoji Kawahito, Shizuoka Univ.
4. LIDAR System Design for Automotive Applications, Eduardo Bartolome, TI
5. Automotive Sensors and Interfaces, Bill Clark, Analog Devices
6. Key Technologies that Support EV Motor Control, Sugako Otani, Renesas
7. Autonomous Vehicles Platform: Processor/Software Architecture, Machine Learning and Security, Jack Weast, Intel

Machine Learning for Circuit Designers

Monday, June 5

This short course introduces the audience to the basics and recent developments in machine learning, gives an overview of the promising applications, and provides insight into state-of-the-art implementation techniques.

1. Machine Learning Basics and Its Applications to Internet-of-Things, Hiroshi Maruyama, Preferred Networks
2. Machine-learning-enabled Design Space for Energy-efficient Mixed-signal Inference Systems, Naveen Verma, Princeton University
3. Designing Efficient Deep Learning Accelerators: Challenges and Opportunities, Joel Emer, MIT/NVidia
4. Advanced Techniques for High-Speed Deep Learning on Large-scale Neural Network in the Cloud, Yasumoto Tomita, Fujitsu Laboratories
5. Deep Learning for Mobile and Embedded Devices, Raheel Khan, Qualcomm
6. Vision-Centric Devices at the Network Edge using Deep-Networks and Computer Vision, David Moloney, Intel/Movidius
7. Mobile/Embedded DNN and AI SoCs, Hoi-Jun Yoo, KAIST

SATELLITE WORKSHOPS

IEEE Silicon Nanoelectronics Workshop, June 4-5
Spintronics Workshop on LSI, June 5

International Forum on Singularity: Exponential X (Friday Forum) NEW!!

Friday, June 9 (the following day of VLSI Symposia)
- Subject: TBD (topics of high-level integration beyond VLSI will be discussed)
- Co-Sponsor: JSPS 165th Committee and VLSI Symposia

For complete conference and registration information, visit: **http://www.vlsisymposium.org/**

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