VLSI Communities Come Together to Identify New Dimensions for Continuing Exponential Growth beyond Moore's Law

Program unveiled for 2017 Symposia on VLSI Technology & Circuits – includes short courses, focus sessions, panel discussions and demo session on "Harmonious Integration toward Next Dimensions" theme

Comment by Satoshi Inaba of Toshiba Memory Corporation, chair of the 2017 Symposium on VLSI Technology:

This year, for the first time, we will have a three-day program overlapping with the 2017 Symposium on VLSI Circuits at the same location. In line with our common theme of "Harmonious Integration toward Next Dimensions," the various events during the two Symposia will stimulate harmonious co-optimization between device technology and circuit design. In addition, the Symposium on VLSI Technology will present 7nm CMOS, emerging memory, and 3D integration technologies. We expect the combination of activities in the two Symposia will generate new dimensions of engagement to maintain the continuous growth of our VLSI community.

Comment by Masato Motomura of Hokkaido University, chair of the 2017 Symposium on VLSI Circuits:

Our Symposium on VLSI Circuits will celebrate its 30th anniversary this year. We've introduced several changes to sustain the continued growth of this premier conference. The three-day overlap mentioned above allows us to start a new associated event, the "International Forum on Singularity: Exponential X," in which distinguished presenters will talk about integrations beyond VLSI.

Plenary Talks (June 6)

On Tuesday morning, two consecutive welcome and plenary sessions will be held in the same conference room. First, in the Technology plenary session, Dr. Takashi Tsutsui, Chief Scientist & SVP, SoftBank Corporation, Japan, will talk about state-of-the-art 5G communication technology and its context up until 2020 and Dr. Fari Assaderaghi, CTO & SVP, NXP Semiconductors, USA, will talk about the latest IoT technology topics. In the following Circuits plenary session, Dr. Takeshi Yukitake, CTO, Connected Solutions Company, Panasonic

Corporation, Japan, will give a talk about the innovative solutions for society to which AI, robotics and IoT will lead us. The final talk of the plenary sessions will be given by Dr. Daniel Rosenband, Google, USA, about leading-edge self-driving car technology.

Focus Sessions (June 6, 7, 8)

Focus sessions for both Symposia will explore different aspects of the conference theme of harmonious integration. Technology focus sessions include "1D and 2D Atomic Thin Materials and Devices" and "Emerging Memory Technology," addressing perspectives on the further development of 1D/2D devices, and the future direction of embedded memories. The Circuits focus sessions are "Ultra-Low Power Wireless Transceivers for IoT Systems" and "Advanced Sensing Systems," examining the development of wireless systems and sensing systems. Joint focus sessions shared by the Technology and Circuits programs include "Ultra Low Power for IoT," "Computing beyond von Neumann," "Emerging Reliability Solutions," and "Advanced Assembly," enabling participants from each of the Symposia to share ideas on the cross-linkage of these critical technology areas.

Panel Discussions (June 6)

Panel discussions provide an opportunity for Symposia participants to interact with leading industry experts in examining critical issues surrounding major industry developments.

"Transistor Future; How Does It Evolve after FinFET Era?" (Tech. Panel)
It is uncertain whether FinFETs can satisfy performance requirements beyond 5nm. Alternative FET structures such as nano-sheets/wires or 2D channels may emerge to secure scaling, but these devices struggle with drive current improvement. To maintain the area scaling, 3D monolithic structures may emerge, but they also have some issues (cost, thermal budget, Joule heating, etc.). A FET roadmap for the post-FinFET era will be discussed by device experts.

"How Will We Survive the Post-Scaling Era?" (Joint Panel)
For many decades the semiconductor industry has enjoyed the benefits of scaling. While we have largely maintained area scaling, it has been difficult to obtain even modest node-to-node improvements in performance and power. What happens when scaling slows to the point that it has, for practical purposes, stopped? How will we survive the post-scaling era? The panel of experts, spanning VLSI technology, circuits, and business, looks at the difficulties ahead and potential ways forward.

"The Most Important Circuits of 2037" (Circuit Panel)
Many innovative circuit design techniques have been presented during the history of 30 years of the Symposium on VLSI Circuits, but what kinds of VLSI circuits will be presented, and for what kind of applications, 20 years from now? Answers will be revealed by a mix of young specialists and senior specialists from across the circuit spectrum.

Full-day Short Courses (June 5)

VLSI Technology Short Course: "Technology Enablers for 5nm and the Next Wave of Integration." This short course will introduce various technology innovations for enabling the 5nm node and a new integration scheme for the Internet of Things and AI era. The course comprises eight lectures given by distinguished experts in their respective fields, covering CMOS device technology, design and technology co-optimization (DTCO), interconnect, 2.5D/3D integration, scaled Analog/RF, embedded memory, and in-memory computing.

VLSI Circuit Short Course: Two circuit short courses will be held. First, "Machine Learning for Circuit Designers" introduces the audience to the basics and to recent developments in machine learning, gives an overview of promising applications, and provides insight into state-of-the-art implementation techniques. Second, "Integrated Circuits for Smart Connected Cars and Automated Driving" demystifies recent advances in automotive electronics covering wireless/wireline communication, powertrain, and various sensors, from the fundamentals to future trends.

Symposia Demo Session (June 5)

The newly-created demo session will provide an opportunity for in-depth interaction with authors of outstanding papers selected from both Technology and Circuits sessions. More than 10 demonstrations will illustrate technological concepts and analyses, table-top real-time presentations of new device characterization, their chip operation highlighting key results, and systems showcasing potential applications for circuit-level innovations.

The annual Symposia on VLSI Technology and Circuits have been held together since 1987, providing an opportunity for the world's top device technologists, circuit and system designers to exchange leading-edge research related to VLSI, with venues alternating between Japan and Hawaii. This year, the Symposia will be held at the Rihga Royal Hotel, Kyoto, Japan from June 5 to 8, 2017, with a fully-overlapping schedule for the first time. The full-day short courses and the demo session are on Monday June 5, plenary talks are on the morning of Tuesday June 6, and the panel discussions are on the evening of Tuesday June 6. This year marks the 37th anniversary for the Symposium on VLSI Technology, and the 31st for the Symposium on VLSI Circuits. The Circuits' 30th anniversary ceremony will be held just before the panel discussions on the evening of June 6. The Symposia are followed by a special event on Friday June 9, the "International Forum on Singularity: Exponential X," details of which will be announced shortly. In order to emphasize synergies between technology and circuits, the 2017 Symposia on VLSI Technology & Circuits offer the attendees an opportunity to participate in both the Technology and Circuits symposia with a single registration.

Sponsoring Organizations

The Symposium on VLSI Technology is sponsored by the Japan Society of Applied Physics and the IEEE Electron Devices Society, in cooperation with the IEEE Solid-State Circuits Society.

The Symposium on VLSI Circuits is sponsored by the Japan Society of Applied Physics and the IEEE Solid-State Circuits Society, in cooperation with the Institute of Electronics, Information and Communication Engineers.

Further information, registration, and a complete program, visit: http://www.vlsisymposium.org.

Media Contacts:
(Japan and Asia)
   Secretariat for VLSI Symposia
   c/o JTB Communication Design, Inc.
   Celestine Shiba Mitsui Bldg., 3-23-1 Shiba, Minato-ku, Tokyo 105-8335, Japan
   Tel: +81-3-5657-0777   E-mail: vlsisymp@jtbcom.co.jp

(North America and EU)
   BtB Marketing
   Chris Burke
   BtB Marketing, co-Media Relations Director
   Tel: +1-919-872-8172   E-mail: chris.burke@btbmarketing.com