2019 Symposium on VLSI Technology

Sunday Workshops

Organizers: K. Tomida, Sony Semiconductor Solutions Corp.
N. Miura, Kobe Univ.

Sunday Workshop 1

Impact of Atomic Layer Processing and Selective Area Patterning on Device Fabrication and Performance [Shunju III]

Sunday, June 9, 19:00-22:00

Organizer: E. A. Joseph, IBM Research

Session 1

19:00 **Effect of ALE on Semiconductor Device Properties,** G.-Y. Yeom, Sungkyunkwan Univ.

19:25 **Surface Reaction Analyses for Atomic Scale Processing by Beam Experiments,** K. Karahashi, Osaka Univ.

19:50 **Selective and Self-Limited Thin Film Processes for the Atomic Scale Era,** R. Clark, TEL

20:15 **Break**

Session 2

20:30 **Plasma-Based Selective Atomic Layer Deposition and Etching to Enable 5nm and Beyond Device Technology,** E. Kessels, Eindhoven Univ. of Tech.

20:55 **Selective Deposition: The Devil is in the Defects,** H. J. Yoo, Intel

21:20 **Creating 3D Nanoscale Structures by Area-Selective Deposition,** A. Delabie, KU Leuven / imec

Sunday Workshop 2

Two Dimensional Materials and Applications [Le Bois]

Sunday, June 9, 19:00-22:00

Organizer: I. Radu, imec

Session 1

19:00 **Path towards Scaling: 2D Materials,** I. Radu, imec

19:30 **Controlled Synthesis of High-Quality 2D Materials for Device Applications,** H. Ago, Kyushu Univ.

20:00 **How to Understand Interface Properties in 2D Heterostructure FETs,** K. Nagashio, The Univ. of Tokyo

20:30 **Electronic, Thermal, and (Some) Unusual Applications of 2D Materials,** E. Pop, Stanford Univ.

21:00 **(Opto-)Electronics: from 2D Materials to Devices,** T. Mueller, TU Vienna

21:30 **Workshop Wrap-Up,** All

Sunday Workshop 3

Low Thermal Budget Dopant Activation for Sequential-3D Integration [La Cigogne]

Sunday, June 9, 19:00-22:00

Organizers: R. Choi, Inha Univ.
J.-M. Shieh, Narlabs-NDL
P. Batude, Leti

Session 1

19:00 **Advanced Annealing Processes for Fin/GAA FETs Fabrications,** Y.-. Lee, NDL - Narlabs

19:25 **Various Junction Formation Techniques for Monolithic 3D Integration,** R. Choi, Inha Univ.

19:50 **SPER Optimized Junction for High Performance Devices within 500°C Thermal Budget,** P. Batude, CEA-Leti

20:15 **Break**

Session 2

20:30 **Low Thermal Budget Pulsed Laser Thermal Annealing for 3D Sequential Integration,** K. Huet, Screen LASSE

20:55 **Review on SPER Process in Si and SiGe (Damage Formation, Dopant Activation and Stability, Impact on Stress Relaxation),** F. Cristiano, CNRS-LAAS

21:20 **Low Temperature Epitaxial films: Challenges and New Enabling Process Technologies,** M. Hemkar, AMAT

Short Course 1

CMOS Technology Enablers for Pushing the Limits of Semiconductors: Materials to Packaging [Shunju II, III]

Monday, June 10, 8:25-16:50

Organizers: M. Tada, NEC Corp.
N. Ramaswamy, Micron Technology, Inc.

8:25 **Introduction**

8:30 **Breaking the Limitations of FinFET Scaling,** M. Y. Liu and C. E. Weber, Intel Corp.

9:20 **Emerging Interconnect Technologies for Nanoelectronics,** K. Saraswat, Stanford Univ.

10:10 **Break**

10:40 **Advanced Process Technologies Required for Future Scaling and Devices,**
R. D. Clark, TEL Technology Center

11:30 **DTCO in 2019: The Precious Metal Stack and the Route to Better Designs,** B. Cline and D. Prasad, Arm Ltd.

12:20 **Lunch**

13:10 **3D Integration for More-Moore and More-than-Moore,** C. H. Tung, TSMC

14:00 **Recent STT-MRAM Technology: From Lab to Fab,** Y. J. Song, Samsung Electronics Co., Ltd.

14:50 **Break**

15:10 **Emerging Logic Devices for Future Computing,** S. Salahuddin, Univ. of California, Berkeley

16:00 **Overview in Three-Dimensionally Arrayed Flash Memory Technology,** R. Katsumata, Toshiba Memory Corp.

Short Course 2

Advanced 5G Circuits, Systems and Applications [Suzaku I]

Monday, June 10, 8:25-16:50

Organizers: H.-J. Song, POSTECH
A. Loke, TSMC

8:25 **Introduction**

8:30 **5G Real and Future,** T. Nakamura, NTT Docomo, Inc.

9:20 **mmWave RFIC Technologies for 5G Infrastructure Applications,** S.-G. Yang, Samsung Electronics Co., Ltd.

10:10 **Break**

10:40 **The Hitchhiker's Guide to Save Moore's Law in 5G Era,** H.-J. Lee, Intel Corp.

11:30 **Multi-Band, Low-IPN LO Generation for 5G and Beyond,** J. Choi, UNIST

12:20 **Lunch**

13:10 **Acoustic Filter for 5G Smartphones,** H. Nakamura, Skyworks

14:00 **Substrate Material and Packaging Technology for 5G Millimeter Wave Communication,**
K. Sudo, Murata Manufacturing Co., Ltd.

14:50 **Break**

15:10 **Beamforming Circuits, Systems, and Operations for 5G MIMO Systems,** H. Wang, Georgia Institute of Tech.

16:00 **Built-In Test and Calibration of Phased Arrays,** B. Floyd, NC State Univ.

Short Course 3

Opportunities and Challenges at the Intersection of Security and AI [Suzaku II]

Monday, June 10, 8:25-16:50

Organizers: M. Hashimoto, Osaka Univ.
X. Zhang, IBM
K. Maekawa, Renesas Electronics Corp.
N. Ramaswamy, Micron Technology, Inc.

8:25 **Introduction**

8:30 **Introduction to Artificial Intelligence and Security,** R. Aitken, Arm Research

9:20 **Deep Learning Processors: Turning Challenges into Opportunities,** H.-J. Yoo, KAIST

10:10 **Break**

10:40 **AI Computing Architectures and Hardware,** J. L. Burns, IBM Research

11:30 **Nonvolatile Circuits for AI Edge Applications,** M.-F. Chang, National Tsing-Hua Univ.

12:20 **Lunch**

13:10 **RRAM Fabric for Neuromorphic and Reconfigurable Compute-In-Memory Systems,** W. D. Lu, Univ. of Michigan

14:00 **Circuit Design Resistant to Side Channel Attacks,** N. Homma, Tohoku Univ.

14:50 **Break**

15:10 **Energy-Efficient Circuits for Cryptography and Entropy Generation,** S. Mathew, Intel Corp.

16:00 **Introduction to Electromagnetic Information Security,** Y. Hayashi, Nara Institute of Science and Technology

Demo Session & Reception [Suzaku I, II, III]

Monday, June 10, 17:30-19:30

Organizers: S. Otani, Renesas Electronics Corp.
K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.
R. Aitken, ARM Ltd.
V. Narayanan, IBM

T2-5
Monolithic Three-Dimensional Imaging System: Carbon Nanotube Computing Circuitry Integrated Directly Over Silicon Imager, T. Srimani, G. Hills, C. Lau and M. Shulaker, Massachusetts Institute of Technology, USA

T8-4
First Demonstration of A Fully-Printed MoS_2 RRAM on Flexible Substrate with Ultra-Low Switching Voltage and Its Application as Electronic Synapse, X. Feng*, Y. Li*, L. Wang*, Z. G. Yu**, S. Chen**, W.-C. Tan*, N. Macadam***, G. Hu***, X. Gong*, T. Hasan***, Y.-W. Zhang**, A. V.-Y. Thean* and K.-W. Ang*, *National Univ. of Singapore, **Institute of High Performance Computing, Singapore and ***Univ. of Cambridge, UK

JFS2-3
Low-Power and ppm-Level Detection of Gas Molecules by Integrated Metal Nanosheets, T. Tanaka*, K. Tabuchi*, K. Tatehora*, Y. Shiiki*, S. Nakagawa*, T. Takahashi**, R. Shimizu*, H. Ishikuro*, T. Kuroda*, T. Yanagida** and K. Uchida*,***, *Keio Univ., **Kyushu Univ. and ***The Univ. of Tokyo, Japan

JFS3-4
Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses, S. Bianchi*, I. Muñoz-Martin*, G. Pedretti*, O. Melnic*, S. Ambrogio** and D. Ielmini*, *Politecnico di Milano, Italy and **IBM Research, USA

C5-1
A 48 MHz 880-nW Standby Power Normally-Off MCU with 1 Clock Full Backup and 4.69-µs Wakeup Featuring 60-nm Crystalline In−Ga−Zn Oxide BEOL-FETs, T. Ishizu*, Y. Yakubo*, K. Furutani*, A. Isobe*, M. Fujita*, T. Atsumi*, Y. Ando*, T. Murakawa*, K. Kato*, M. Fujita** and S. Yamazaki*, *Semiconductor Energy Laboratory Co., Ltd. and **The Univ. of Tokyo, Japan

C5-2
A Microwatt-Class Always-On Sensor Fusion Engine Featuring Ultra-Low-Power AOI Clocked Circuits in 14nm CMOS, S. Hsu, A. Agarwal, M. Kar, M. Anders, H. Kaul, R. Kumar, S. Satpathy, V. Suresh, S. Mathew, R. Krishnamurthy and V. De, Intel Corp., USA

C6-4
A CMOS Temperature Stabilized 2-Dimensional Mechanical Stress Sensor with 11-bit Resolution, U. Nurmetov*, T. Fritz**, E. Muellner**, C. Dougherty**, F. Kreupl* and R. Brederlow**, *Technical Univ. of Munich and **Texas Instruments Freising, Germany

C8-3
A 1.53 mm³ Crystal-Less Standards-Compliant Bluetooth Low Energy Module for Volume Constrained Wireless Sensors, R. Wiser*, K. A. Sankaragomathi*, J. Schauer*, S. Korhummel*, A. Kavousian*, D. Yeager*, N. Arumugam*, N. Pletcher*, D. Barkin*, R. Parker**, L. Callaghan**, R. Ruby** and B. Otis*, *Verily Life Sciences and **Broadcom Ltd., USA

C9-1
A 1.02pJ/b 417Gb/s/mm USR Link in 16nm FinFET, A. Tajalli*,***, M. Bastani*, D. Carnelli*, C. Cao*, J. Fox**, K. Gharibdoust*, D. Gorret*, A. Gupta**, C. Hall**, A. Hassanin*, K. Hofstra*, B. Holden*, A. Hormati*, J. Keay**, Y. Mogentale*, G. Paul*, V. Perrin*, J. Phillips**, S. Raparthy**, A. Shokrollahi*, D. Stauffer*, R. Simpson**, A. Stewart**, G. Surace**, O. T. Amirii*, E. Truffa*, A. Tschank**, R. Ulrich*, C. Walter* and A. Singh*, *Kandou Bus, Switzerland, **Kandou Bus, UK and ***Univ. of Utah, USA

C16-1
A 50Gb/s Hybrid Integrated Si-Photonic Optical Link in 16nm FinFET, M. Raj*, Y. Frans*, S. L. C. Ambatipudi*, D. Mahashin*, P. De Heyn**, S. Balakrishnan**, J. Van Campenhout**, J. Grayson***, M. Epitaux*** and K. Chang*, *Xilinx, Inc., USA, **imec, Belgium and ***Samtec, Inc., USA

C17-4
The Demonstration of Gate Dielectric-Fuse 4kb OTP Memory Feasible for Embedded Applications in High-K Metal-gate CMOS Generations and Beyond, E. R. Hsieh*,**, C. W. Chang*, C. C. Chuang*, H. W. Chen*,*** and S. Chung*, *National Chiao Tung Univ., Taiwan, **Stanford Univ., USA and ***United Microelectronics Corp., Taiwan

C20-1
A 4900μm² 839Mbps Side-Channel Attack Resistant AES-128 in 14nm CMOS with Heterogeneous Sboxes, Linear Masked MixColumns and Dual-Rail Key Addition, R. Kumar, V. Suresh, M. Kar, S. Satpathy, M. Anders, H. Kaul, A. Agarwal, S. Hsu, G. Chen, R. Krishnamurthy, V. De and S. Mathew, Intel Corp., USA

JFS3-3
A Ternary Based Bit Scalable, 8.80 TOPS/W CNN Accelerator with Many-Core Processing-in-Memory Architecture with 896K Synapses/mm², S. Okumura, M. Yabuuchi, K. Hijioka and K. Nose, Renesas Electronics Corp., Japan

Joint Evening Panel Discussion

The Semiconductor Industry at a Tipping Point: What's Next? [Shunju II, III]

Monday, June 10, 20:00-21:30

Organizers: P. Yue, Hong Kong Univ. of Science and Technology
M. Kobayashi, The Univ. of Tokyo
K. Okada, Tokyo Institute of Technology
E. Naviasky, Cadence
G. Yeric, ARM Ltd.

Moderator: K. Makinwa, Delft Univ. of Technology

Panelists: B. Nauta, Univ. of Twente
Z. Wang, Tsinghua Univ.
F. Yinug, SIA
A. Piovaccari, Silicon Labs
S. Sumida, Woodside Capital Partners
J. Chang, TSMC

The field that has transformed the world and which we have annually gathered to celebrate is undergoing a metamorphosis. Economics no longer inexorably points down Moore's curve, price per gate has leveled or is rising. The leading edge nodes have become the territory of the very few companies that dare to use them. Simultaneously, the number of startups has shrunk by orders of magnitude. So where are we going? Together with you, a panel of experts with backgrounds ranging from academia, industry association, and companies from start-ups to established will attempt to provide some insights into our future.

SESSION 1

Joint Opening and Plenary Session 1 [Shunju I, II, III]

Tuesday, June 11, 8:00-10:00

8:00-
Joint Welcome and Opening Remarks
M. Masahara, AIST
M. Ikeda, The Univ. of Tokyo
C.-P. Chang, Applied Materials, Inc.
K. Chang, Xilinx Inc

8:40-
Plenary
Chairpersons: K. Takeuchi, Chuo Univ.
T. Palacios, MIT

C1-1 - 8:40 (Plenary)
Virtual Cyborg: Beyond Human Limits, M. Inami, The Univ. of Tokyo, Japan

The social revolutions have accompanied innovation of the view of the body. If we regard the information revolution as establishment of a virtual society against the real society, it is necessary to design a new view of body “JIZAI body (Virtual Cyborg)”, which can adapt freely to the change of social structure, and establish a new view of the body.
In this talk, we discuss how we understand of basic knowledge about the body editing for construction of JIZAI body (Virtual Cyborg) based on VR, AR and Robotics. Superhuman Sports: Applying Human Augmentation to Physical Exercise.
This talk will also present Superhuman Sports, a form of “Human-Computer Integration” to overcome somatic and spatial limitation of humanity by merging technology with the body. In Japan, official home of the 2020 Olympics and Paralympics , we hope to create a future of sports where everyone, strong or weak, young or old, non-disabled or disabled, can play and enjoy playing without being disadvantaged.

T1-1 - 9:20 (Plenary)
Managing Moore's Inflection: DARPA's Electronics Resurgence Initiative, W. Chappell, DARPA, USA

In June 2017, the DARPA Microsystems Technology Office (MTO) announced the upwards of $1.5 billion Electronics Resurgence Initiative (ERI) to ensure far-reaching improvements in electronics performance well beyond the limits of traditional scaling. The gains that came as electronics technology sprinted forward according to Moore’s Law were not guaranteed but realized through ingenuity and close collaboration between commercial industry, academia, and government. The present moment, beyond his law, is where Gordon Moore had true prescience. ERI is building on the long tradition of successful partnerships to foster the environment needed for the next wave of U.S. and allied semiconductor innovation.

SESSION 2

Highlight [Shunju I, II, III]

Tuesday, June 11, 10:30-12:35

Chairpersons: K. Miyashita, Toshiba Electronic Devices & Storage Corp.
G. Jurczak, Lam Research

T2-1 - 10:30
Enhanced Reliability of 7nm Process Technology Featuring EUV, K. Choi, H. C. Sagong, W. Kang, H. Kim, J. Hai, M. Lee, B. Kim, S. Lee, H. Shim, J. Park, Y. Cho, H. Rhee and S. Pae, Samsung Electronics Co., Ltd., Korea

In this paper, we report the reliability characterization of 7nm FinFET technology, in which the highly scaled 6th generation of FinFETs and 256Mbit SRAM cells was newly developed by utilizing EUV. The single EUV patterning of MOL and BEOL resulted in significantly improved reliability distribution as compared to the previous nodes with multiple patterning techniques. The successful demonstration on product reliability including SRAM, Logic HTOL, and SER as technology evaluation was performed, indicating the 7nm technology+EUV is ready for high volume manufacturing.

T2-2 - 10:55
Technology Challenges and Enablers to Extend Cu Metallization to Beyond 7 nm Node, T. Nogami*, H. Huang*, H. Shobha*, R. Patlolla*, J. Kelly*, C. Penny*, C.-K. Hu*, D. Sil*, S. DeVries*, J. Lee*, S. Nguyen*, S. Lian**, D. Edelstein*, B. Haran*, L. Jiang*, J. Demarest*, J. Li*, G. Lian*, M. Ali*, P. Bhosale*, N. Lanzillo*, K. Motoyama*, T. Standaert* and G. Bonilla*, *IBM Research and **Samsung Electronics Co., Ltd., USA

Electromigration (EM) and TDDB reliability of Cu interconnects with a barrier/wetting layer as thin as 2 nm employing a PVD-reflowed through-Co self-forming barrier (tCoSFB) is demonstrated to meet the required specifications for 7 nm BEOL. The resulting Cu EM lifetime is 2000X longer than Cu interconnects with a standard scaled barrier/wetting layer. This tCoSFB Cu EM and TDDB reliability performance were equivalent to pure Co metal interconnects, but with a 50% lower line resistance even down to 30 nm pitch dimensions. However, the annealing process for PVD-reflow Cu seed that enhances EM reliability caused Cu agglomeration at dual damascene line-end vias, leading to poor via-chain yield. Resolving this geometry-sensitive via-fill problem was identified as key to extending Cu manufacturability to 7 nm and beyond. We propose, and show preliminary data, for Cu/tCoSFB metallization with CVD Co via pre-fill as potential solution.

T2-3 - 11:20
3D Multi-Chip Integration with System on Integrated Chips (SoIC™), M.-F. Chen, C.-C. Hu, W.-C. Chiou and D. C. H. Yu, TSMC, Taiwan

The electrical characterization of System on Integrated Chips (SoIC™), an innovative 3D heterogeneous integration technology manufactured in front-end of line with known-good-die is reported. Chiplets integration of devices including foundry leading edge 7nm FinFET technology with SoIC™ illustrates its advantages in high bandwidth density and high power efficiency, as compared with 2.5D and conventional 3D-IC with micro-bump/TSV.

T2-4 - 11:45
In-Memory Reinforcement Learning with Moderately-Stochastic Conductance Switching of Ferroelectric Tunnel Junctions, R. Berdan*, T. Marukame*, S. Kabuyanagi**, K. Ota**, M. Saitoh**, S. Fujii**, J. Deguchi** and Y. Nishi*, *Toshiba Corp. and **Toshiba Memory Corp., Japan

Building compact and efficient reinforcement learning (RL) systems for mobile deployment requires departure from the von-Neumann computing architecture and embracing novel in-memory computing, and local learning paradigms. We exploit nano-scale ferroelectric tunnel junction (FTJ) memristors with inherent analogue stochastic switching arranged in selectorless crossbars to demonstrate an analogue in-memory RL system, which, via a hardware-friendly algorithm, is capable of learning behavior policies. We show that commonly undesirable stochastic conductance switching is actually, in moderation, a beneficial property which promotes policy finding via a process akin to random search. We experimentally demonstrate path-finding based on reinforcement, and solve a standard control problem of balancing a pole on a cart via simulation, outperforming similar deterministic RL systems.

T2-5 - 12:10
Monolithic Three-Dimensional Imaging System: Carbon Nanotube Computing Circuitry Integrated Directly Over Silicon Imager, T. Srimani, G. Hills, C. Lau and M. Shulaker, Massachusetts Institute of Technology, USA

Here we show a hardware prototype of a monolithic three-dimensional (3D) imaging system that integrates computing layers directly in the back-end-of-line (BEOL) of a conventional silicon imager. Such systems can transform imager output from raw pixel data to highly processed information. To realize our imager, we fabricate 3 vertical circuit layers directly on top of each other: a bottom layer of silicon pixels followed by two layers of CMOS carbon nanotube FETs (CNFETs) (comprising 2,784 CNFETs) that perform in-situ edge detection in real-time, *before* storing data in memory. This approach promises to enable image classification systems with improved processing latencies.

Diversity Luncheon [Le Bois]

Tuesday, June 11, 12:45-13:55

SESSION 3

Focus Session - Quantum & Neuromorphic Computing [Shnju II, III]

Tuesday, June 11, 14:00-15:40

Chairpersons: K. Endo, AIST
M. Vinet, CEA-LETI, MINATEC

T3-1 - 14:00 (Invited)
Superconductive Parametric Devices, T. Yamamoto, NEC Corp., Japan

Superconducting parametric amplifier, originally developed more than half a century ago, gained renewed interests in some experiments of superconducting quantum electronics about a decade ago, and now has become an indispensable tool in the field of superconducting quantum information processing. More recently, there are several proposals, where a parametric oscillator, which is a parametric amplifier pumped above the threshold, is used as a quantum bit and the network of the parametric oscillators solve some computational tasks. Here, we briefly introduce the research activity on the development of the superconducting parametric devices, including our results, with some historical backgrounds.

T3-2 - 14:25 (Invited)
Towards Scalable Quantum Computing Based on Silicon Spin, T. Meunier*, L. Hutin***, B. Bertrand***, Y. Thonnart***, G. Pillonnet***, G. Billiot***, H. Jacquinot***, M. Cassé***, S. Barraud***, Y.-J. Kim***, V. Mazzocchi***, A. Amisse***.**, H. Bohuslavskyi***.**, L. Bourdet**, A. Crippa**, X. Jehl**, R. Maurand**, Y.-M. Niquet**, M. Sanquer**, B. Venitucci**, B. Jadot*, E. Chanrion*, P.-A. Mortemousque*, C. Spence*, M. Urdampilleta*, S. De Franceschi** and M. Vinet***, *CNRS, **CEA, INAC and ***CEA, LETI, France

T3-3 - 14:50
Monolithic 3D$^+$-IC Based Reconfigurable Compute-in-Memory SRAM Macro, S. Srinivasa*, Y.-N. Tu**, X. Si**, C.-X. Xue**, C.-Y. Lee**, F.-K. Hsueh***, C.-H. Shen***, J.-M. Shieh***, W.-K. Yeh***, A. K. Ramanathan*, M.-S. Ho****, J. Sampson*, M.-F. Chang** and V. Narayanan*, *The Pennsylvania State Univ., USA, **National Tsing Hua Univ., ***Taiwan Semiconductor Research Institute and ****National Chung Hsing Univ., Taiwan

This paper presents the first monolithic 3D two-layer reconfigurable SRAM macro capable of executing multiple Compute-in-Memory (CiM) tasks as part of data readout. Fabricated using low cost FinFET based 3D$^+$-IC, the SRAM offers concurrent data read from both layers and write from layer 2 with 0.4V V_{ddmin}. 12.8x improved computation latency is achieved as compared to near memory computation of successive Boolean operations.

T3-4 - 15:15
Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway Toward All-Spin Artificial Deep Neural Network, M.-H. Wu*, M.-C. Hong*, C.-C. Chang*, P. Sahu*, J.-H. Wei**, H.-Y. Lee**, S.-S. Sheu** and T.-H. Hou*,**, *National Chiao Tung Univ. and **Industrial Technology Research Institute of Taiwan, Taiwan

This work reports the complete framework from device to architecture for deep learning acceleration in an all-spin artificial neural network (ANN) built by highly manufacturable STT-MRAM technology. The most compact analog integrate-and-fire neuron reported to date is developed based on the back-hopping oscillation in magnetic tunnel junctions. This novel device is unique because it performs numerous essential neural functions simultaneously, including current integration, voltage spike generation, state reset, and 4-bit precision. The device itself is also a stochastic binary synapse, and thus eases the implementation of the compact all-spin ANN with high accuracy for online training.

SESSION 4

Ferroelectric I [Shunju I]

Tuesday, June 11, 14:00-15:40

Chairpersons: M. Kobayashi, The Univ. of Tokyo
N. Ramaswamy, Micron Technology Inc.

T4-1 - 14:00
Energy-Efficient Edge Inference on Multi-Channel Streaming Data in 28nm HKMG FeFET Technology, S. Dutta, W. Chakraborty, J. Gomez, K. Ni, S. Joshi and S. Datta, Univ. of Notre Dame, USA

We present a system implementing extremely energy-efficient inference on multi-channel biomedical-sensor data. We leverage FeFETs to perform classification directly on analog sensor signals. We demonstrate: (i) voltage-controlled multi-domain ferroelectric polarization switching to obtained 8 distinct transconductance (g_m) states in a 28nm HKMG ferroelectric FET (FeFET) technology [1], (ii) 30x tunable range in g_m over the bandwidth of interest, (iii) successful implementation of artifact removal, feature extraction and classification for seizure detection from CHB-MIT EEG dataset with 98.46% accuracy and <0.375/hr. false alarm rate for two patients, (iv) ultra-low energy of 47 fJ/MAC with 1,000x improvement in area compared to alternative mixed-signal MAC.

T4-2 - 14:25
Fundamental Understanding and Control of Device-To-Device Variation in Deeply Scaled Ferroelectric FETs, K. Ni, W. Chakraborty, J. Smith, B. Grisafe and S. Datta, Univ. of Notre Dame, USA

In this work, we present a comprehensive Kinetic Monte Carlo (KMC) modeling based statistical framework to evaluate the device-to-device variation of thin-film HfO_2 ferroelectric FET (FeFET). We conclude that the closing of the memory window in a FeFET array with device scaling can be attributed to: 1) limited number of domains; 2) variation among domains; 3) intrinsic stochasticity of individual domain switching. To enable further scaling of FeFET, co-optimization approaches from material, process, and device operation to control variation are proposed: i) increase the number of domains through material/process optimization (e.g. decrease of deposition temperature, etc.); ii) improve the uniformity of domains (e.g. minimizing the domain size variation and defect distribution, etc.); iii) increase the pulse amplitude/width to ensure deterministic switching of individual domains.

T4-3 - 14:50
Experimental Demonstration of Ferroelectric HfO_2 FET with Ultrathin-Body IGZO for High-Density and Low-Power Memory Application, F. Mo, Y. Tagawa, C. Jin, M. Ahn, T. Saraya, T. Hiramoto and M. Kobayashi, The Univ. of Tokyo, Japan

We have experimentally demonstrated a ferroelectric HfO_2 FET with memory operation by introducing ultrathin IGZO as a channel material. Ultrathin-body IGZO ferroelectric FET (FeFET) shows high mobility with deposited channel material, nearly ideal subthreshold slope, and controllable memory characteristics with the use of back-end compatible process. These results are attributed to the properties of IGZO channel: junctionless FET operation, nearly-zero low-k interfacial layer on metal-oxide channel and good capping effect for realizing ferroelectric phase formation with $HfZrO_2$. IGZO FeFET will open a new path for high-density memory application.

T4-4 - 15:15
Ferroelectric and Anti-Ferroelectric Hafnium Zirconium Oxide: Scaling Limit, Switching Speed and Record High Polarization Density, X. Lyu, M. Si, X. Sun, M. A. Capano, H. Wang and P. D. Ye, Purdue Univ., USA

The ferroelectric (FE) and anti-ferroelectric (AFE) properties of hafnium zirconium oxide (HZO) are investigated systematically down to 3 nm. The ferroelectric polarization, switching speed and the impact of atomic layer deposited (ALD) tungsten nitride (WN) electrodes are studied. Record high remnant polarization (P_r) on FE HZO and record high saturation polarization (P_S) on AFE HZO are achieved with WN electrodes, especially in ultrathin sub-10 nm regime. A high dielectric constant of 30.4 is achieved on AFE HZO. The polarization switching speed of FE and AFE HZO, associated with C-V frequency dispersion, are also studied. For the first time, it is found polarization switching speed is faster in AFE HZO than FE HZO, suggesting AFE-FET could be more promising for high speed memory devices.

SESSION 5

Focus Session - 3D Integration and Packaging [Shnju II, III]

Tuesday, June 11, 16:00-18:05

Chairpersons: Y. Masuoka, Samsung Electronics Co., Ltd
M. Delaus, Analog Devices, Inc.

T5-1 - 16:00 (Invited)
The Future of Advanced Package Solutions, D.-W. Kim and T. Hwang, Samsung Electronics Co., Ltd., Korea

As the 4th industry revolution emerges into the semiconductor industry, high computing power and high data bandwidth are required for semiconductor devices. These demands lead to the adaption of the advanced packaging technology. For mobile application, fan-out technologies are used for smart phones due to small form factors and thermal performances. For server applications, 2.5D and 3D technologies are employed for cloud and artificial intelligence in terms of high memory bandwidth and a big die. However, there are two significant issues to resolve for advanced packaging. One is a thermal issue and the other is an electrical issue. Novel thermal materials and package structures are expected to improve the thermal performances. Redistribution substrate and through silicon via will reduce electrical loss for high speed signals. In this paper, we will investigate how the packaging technologies evolve in the future.

T5-2 - 16:25 (Invited)
Heterogeneous Integration Roadmap - Driving Force & Enabling Technology for Systems of the Future, W. Chen* and B. Bottoms**, *ASE and **3MTS, USA

Our industry has reinvented itself through multiple disruptive changes in market, products, and technology. We are at the triple inflection point, brought about by tech company disruption, Moore's Law plateauing, and the explosive growth of the digital economy. Continued progress will require a new vision for electronic innovations. This paper shows examples of Heterogeneous Integration (SiP) for two market segments, Smart Phone and HPC Server and describes the purpose and organization of the Heterogeneous Integration Roadmap.

T5-3 - 16:50
High Performance Heterogeneous Integration on Fan-Out RDL Interposer, S.-M. Chen, M. C. Yew, F. C. Hsu, Y. J. Huang, Y. H. Lin, M. S. Liu, K. Lee, P. C. Lai, T. M. Lai and S.-P. Jeng, TSMC, Taiwan

The fan-out packaging technology has recently been adopted in mobile application processors due to its advantages in form factor, fine pitch traces, and efficient thermal dissipation. This paper demonstrates heterogeneous integration on a fan-out redistribution layer (RDL) interposer. The package has a full-reticle size Si die and two HBMs. Si die and memory modules are attached to a fanout RDL and are then attached to a multilayer substrate. This advanced package meets both electrical and mechanical requirements. The fanout RDL interposer is comprised of polymer and copper traces, and it is relatively mechanically flexible. Such flexibility enhances C4 joint integrity, and allows the new package to scale up its size to meet more complex functional demands.

T5-4 - 17:15
1 Kbit 6T SRAM Arrays in Carbon Nanotube FET CMOS, P. S. Kanhaiya, C. Lau, G. Hills, M. Bishop and M. M. Shulaker, Massachusetts Institute of Technology, USA

We experimentally demonstrate the first static random-access memory (SRAM) arrays based on carbon nanotube (CNT) field-effect transistors (CNFETs). We demonstrate full 1 Kbit 6 transistor (6T) SRAM arrays fabricated with CNFET CMOS (totalling 6,144 p- and n-type CNFETs), with all 1,024 cells functioning correctly without any per-unit customization. We demonstrate robust operation by writing and reading multiple patterns to the Kbit arrays and characterize single-cell SRAM variability (write and read margins) and repeat cycling of cells. Due to low-temperature BEOL-compatible processing, CNFET SRAM enables new opportunities for digital systems, since: (1) CNFET SRAM can be fabricated directly on top of computing logic, and (2) buried power rails (i.e., as in our demonstration where the power rails are fabricated underneath the FET) can potentially enable smaller-area SRAM layouts.

T5-5 - 17:40
Buried Metal Line Compatible with 3D Sequential Integration for Top Tier Planar Devices Dynamic V_{th} Tuning and RF Shielding Applications., A. Vandooren*, Z. Wu*, A. Khaled*, J. Franco*, B. Parvais*,***, W. Li*, L. Witters*, A. Walke*, L. Peng*, N. Rassoul*, P. Matagne*, G. Jamieson*, F. Inoue*, B.-Y. Nguyen**, H. Debruyn*, K. Devriendt*, L. Teugels*, N. Heylen*, E. Vecchio*, T. Zheng*, D. Radisic*, E. Rosseel*, W. Vanherle*, A. Hikavyy*, B. T. Chan*, G. Besnard**, W. Schwarzenbach**, G. Gaudin**, I. Radu**, N. Waldron*, V. De Heyn*, S. Demuynck*, J. Boemmels*, J. Ryckaert*, N. Collaert* and D. Mocuta*, *imec, Belgium, **Soitec, France and ***Vrije Universiteit Brussel, Belgium

3D sequential integration is shown to be compatible with a back gate implementation suitable for dynamic V_{th} tuning of the FDSOI top tier devices. The back gate is inserted seamlessly into the 3D sequential process flow during the top Si layer transfer, providing a close proximity to the top tier device, as well as a uniform and high quality thermal back oxide. A threshold voltage tuning of ~103mV/V and ~139mV/V is obtained in p- and nMOS top tier junction-less devices, respectively, over a back gate bias range of +/-2V. BTI reliability measurements show no detrimental impact of the back gate bias. Back-gating can therefore be used to enhance the I_{ON} performance with no reliability penalty. The buried metal line is also shown to lower crosstalk by metal shielding insertion between top and bottom tier metal lines, with a reduction larger than 10dB up to 45GHz.

SESSION 6

PCM & ReRAM [Shunju I]

Tuesday, June 11, 16:00-17:40

Chairpersons: M. Tada, NEC Corp.
P. Ye, Purdue Univ.

T6-1 - 16:00
Comprehensive Scaling Study on 3D Cross-Point PCM Toward 1Znm Node for SCM Applications, W. C. Chien*, H. Y. Ho*, C. W. Yeh*, C. H. Yang*, H. Y. Cheng*, W. Kim**, I. T. Kuo*, L. M. Gignac**, E. K. Lai*, N. Gong**, Y. C. Chou*, R. L. Bruce**, M. BrightSky**, H. L. Lung*, C. W. Cheng**, Y. F. Lin**, J. M. Papalia**, F. Carta** and A. Ray**, *Macronix International Co., Ltd., Taiwan and **IBM Corp., USA

We present a scaling study toward 1Znm node 3D Cross-point PCM (XPCM) for Storage Class Memory (SCM) applications. The low operation current, and low metal line loading resistance are desired to avoid a wide operation voltage distribution in a cross-point array. For the first time, AC threshold voltage (Vth) of 1S1R OTS-PCM was studied, which will impact the operation scheme. To achieve Tera bits per chip density, six layers 1Znm 3D XPCM with OTS showing high Vth and low leakage current, and scalable periphery circuit are required.

T6-2 - 16:25
Ultra-Thin (<10nm) Dual-Oxide (Al_2O_3/TiO_2) Hybrid Device (Memory/Selector) with Extremely Low I_{off} (<1nA) and I_{reset} (<1nA) for 3D Storage Class Memory, C. Sung, J. Song, D. Lee, S. Lim, M. Kwak and H. Hwang, POSTECH, Korea

We demonstrate ultra-thin ALD-processed dual-oxide (Al_2O_3/TiO_2) hybrid device with memory and selector characteristics by engineering the stability of metal filament in Al_2O_3 and TiO_2 layer. The optimized hybrid memory device shows outstanding performances such as low off current (<1nA), low reset current (<1nA), and high on/off ratio (>10^4). Inserting a Ti buffer layer which has a low electrode potential value, we observed excellent uniformity and retention property. Finally, an outstanding read/write margins and ultra-low power consumption are confirmed through array simulations of the proposed hybrid memory device.

T6-3 - 16:50
Monte Carlo Model of Resistance Evolution in Embedded PCM with Ge-Rich GST, O. Melnic*, M. Borghi**, E. Palumbo**, P. Zuliani**, R. Annunziata** and D. Ielmini*, *Politecnico di Milano and **STMicroelectronics N.V., Italy

This work presents an optimized model for resistance evolution in PCM cells with Ge-rich GeSbTe (GST) alloy as active material. Unlike conventional $Ge_2Sb_2Te_5$, the low-resistance (set) state of Ge-rich GST shows a resistance drift to high resistance R, similar to the high resistance (reset) state, which could be a potential risk for data reliability. We develop a Monte Carlo (MC) model which predicts the time evolution of R at the statistical level of a memory array at various temperature T. The model is validated against variable temperature annealing, such as the soldering profile in embedded PCM, supporting the good reliability of Ge-rich GST at high T.

T6-4 - 17:15
Confined PCM-Based Analog Synaptic Devices Offering Low Resistance-Drift and 1000 Programmable States for Deep Learning, W. Kim*, R. L. Bruce*, T. Masuda**, G. W. Fraczak*, N. Gong*, P. Adusumilli*, S. Ambrogio**, H. Tsai**, J. Bruley*, J.-P. Han*, M. Longstreet*, F. Carta*, K. Suu*** and M. BrightSky*, *IBM T. J. Watson Research Center, **IBM Research, USA and ***ULVAC, Inc., Japan

We have demonstrated, for the first time, a combination of outstanding linearity of analog programming with matched PCM pairs, small analog programming noise, an extremely low resistance drift (R-drift) coefficient (0.005, median) and high endurance for a CVD-based confined phase change memory (PCM) with a thin metallic liner. In-depth analysis of linear analog programming is also presented. MNIST simulations using a pair of these confined PCM devices as a synaptic element yield a high test accuracy of 95%.

Technology Evening Panel Discussion

What Will the Foundries of the Future Do? [Shunju I]

Tuesday, June 11, 20:00-21:30

Organizers: M. Kobayashi, The Univ. of Tokyo
G. Yeric, ARM Ltd.

Moderator: A. DeVilliers, TEL

Panelists: K. Mistry, Intel Corp.
A. Yu, GLOBALFOUNDRIES Inc.
C. Chidambaram, Qualcomm Technologies, Inc.
P. Jung, Samsung
T. Ohba, Tokyo Tech. Univ.
K. Zhang, TSMC

Conventional process node scaling has been extremely successful for many decades, but the challenges below 5 nm may require us to question our assumptions about the foundries of the future if we want the semiconductor industry to thrive in the next decade:
・Is EUV enough for patterning requirements? What is a key stopper?
・How long can FinFET/nanowire/nanosheet push the silicon MOSFET?
Will something different be required?
・How specifically can “More-than-Moore” provide value beyond scaling?
・How much can 3D chiplets provide?
・Are there opportunities for other fab styles? Minimal fab vs. giga fab?
In this panel, we will discuss technology challenges and opportunities as well as new deliverable values to market, in order to provide perspective on the foundries of the future.

SSCS & EDS Young Professionals and Students Micro-Mentoring and Career Coaching Session [La Cigogne]

Tuesday, June 11, 18:15-19:15

SESSION 7

Remarks, Awards and Plenary Session 2 [Shunju I, II, III]

Wednesday, June 12, 8:00-10:00

8:00-
Remarks and Award Ceremony
M. Masahara, AIST
M. Ikeda, The Univ. of Tokyo
C.-P. Chang, Applied Materials, Inc.
K. Chang, Xilinx Inc

8:40-
Plenary
Chairpersons: S. Yamakawa, Sony Semiconductor Solutions Corp.
B. Ginsburg, Texas Instruments

C10-1 - 8:40 (Plenary)
Computational Directions for Augmented Reality Systems, S. Rabii, E. Beigne, V. Chandra, B. De Salvo, R. Ho and R. Pendse, Facebook Inc., USA

Augmented reality (AR) is a set of technologies that will fundamentally change the way we interact with our environment. It represents a merging of the physical and the digital worlds into a rich, context aware and accessible user interface delivered through a socially acceptable form factor such as eyeglasses. One of the biggest challenges in realizing a comprehensive AR experience is managing power consumption to ensure both adequate battery life and a physically comfortable thermal envelope. This presentation reviews advanced concepts in minimizing power in data transfer across components, leveraging highly efficient accelerators while maintaining programmability, and the potential of emerging nonvolatile memories for low power computing.

T7-1 - 9:20 (Plenary)
Si Platform for Developing Spin-Based Quantum Computing, S. Tarucha, RIKEN Center for Emergent Matter Science, RIKEN and Tokyo Univ. of Science, Japan

To date basic techniques of implementing spin-based quantum computing have been developed using quantum dots, including single and two-qubit gates, initialization and readout. But improving the operation fidelity as well as increasing the qubit number is still a challenge in realizing fault-tolerant quantum computing. Electron spins confined to Si quantum dots have a long decoherence time and the physical area for implementing a qubit is very small, smaller than 0.1 mm^2. We have developed a fast gating technique for the Si quantum dots to operate the qubits with high fidelity thanks to the weakness of decoherence. I will first discuss the spin dephasing measured for Si quantum dots and how to suppress it to raise the gate fidelity well exceeding the threshold of fault tolerant computation. I will then review the current research and development to scale up the qubit system, including integration technologies of the quantum processor and cryo-electronics to improve the performance of the large-scale quantum circuit.

SESSION 8

AI I [Shnju II, III]

Wednesday, June 12, 10:30-12:10

Chairpersons: S. S. Chung, National Chiao Tung Univ.
V. Narayanan, IBM

T8-1 - 10:30
Inference of Long-Short Term Memory Networks at Software-Equivalent Accuracy Using 2.5M Analog Phase Change Memory Devices, H. Tsai, S. Ambrogio, C. Mackin, P. Narayanan, R. M. Shelby, K. Rocki, A. Chen and G. W. Burr, IBM Research, USA

We report accuracy for forward inference of long-short-term-memory(LSTM) networks using weights programmed into the conductances of >2.5M phase-change memory (PCM) devices. We demonstrate strategies for software weight-mapping and programming of hardware analog conductances that provide accurate weight programming despite significant device variability. Inference accuracy very close to software model baselines is achieved on several language modeling tasks.

T8-2 - 10:55
Gait Identification Using Stochastic OXRRAM-Based Time Sequence Machine Learning, R. Degraeve*, J. Doevenspeck*,**, A. Fantini*, P. Debacker*, D. Linten* and D. Verkest*, *imec and **KU Leuven, Belgium

A machine learning method is demonstrated for building a model of gait data for identification purpose. In contrast to 'deep learning' algorithms, our algorithm allows for a very fast, 'one shot' or 'few shots' learning. The algorithm is completely implementable in oxygen vacancy-based RRAM, and uses an intrinsic SET-dependent RESET probability in TaOx filamentary OXRRAM as local learning rule. Equal error rate down to ~10% is reached using less than 1Mb memory. Our algorithm relates to Non-Linear Dynamic Systems (NDS), allowing for interpretation and minimized hardware dimensioning.

T8-3 - 11:20
RRAM-Based Spiking Nonvolatile Computing-In-Memory Processing Engine with Precision-Configurable in Situ Nonlinear Activation, B. Yan*, Q. Yang*, W.-H. Chen**, K.-T. Chang**, J.-W. Su**,***, C.-H. Hsu***, S.-H. Li***, H.-Y. Lee***, S.-S. Sheu***, M.-S. Ho****, Q. Wu*****, M.-F. Chang**, Y. Chen* and H. Li*, *Duke Univ., USA, **National Tsing Hua Univ., ***Industrial Technology Research Institute of Taiwan, ****National Chung Hsing Univ., Taiwan and *****Air Force Research Laboratory, USA

This work presents a hybrid CMOS-RRAM integration of spiking nonvolatile computing-in-memory (nvCIM) processing engine (PE) that includes a 64Kb RRAM macro and a novel in situ nonlinear activation (ISNA) module. We integrate the computing controller and nonlinear activation function on-chip to compute convolutional or fully-connected neural network. ISNA merges A/D conversion and activation computation by leveraging its nonlinear working region. This eliminates the need for additional circuits to realize nonlinearity and reduces area by 43.7 times w.r.t. the ADC scheme. The activation precision of ISNA can be configured from 1 to 8 bits to balance throughput, accuracy and power efficiency. The measurement of 4-layer LeNet shows such optimization improves 23.1% of computing speed via compromising a 2.5% relative accuracy drop. The proposed nvCIM PE achieves 16.9 TOPS/W power efficiency and a maximum spike frequency of 99.24 MHz.

T8-4 - 11:45
First Demonstration of A Fully-Printed MoS_2 RRAM on Flexible Substrate with Ultra-Low Switching Voltage and Its Application as Electronic Synapse, X. Feng*, Y. Li*, L. Wang*, Z. G. Yu**, S. Chen**, W.-C. Tan*, N. Macadam***, G. Hu***, X. Gong*, T. Hasan***, Y.-W. Zhang**, A. V.-Y. Thean* and K.-W. Ang*, *National Univ. of Singapore, **Institute of High Performance Computing, Singapore and ***Univ. of Cambridge, UK

We demonstrate the first fully-printed resistive random access memory (RRAM) on flexible substrate using 2D layered dichalcogenides, exhibiting ultra-low switching voltage down to 0.18 V and an on/off ratio up to 10^7. The novel switching medium is printed by formulating multilayer molybdenum disulfide (MoS_2) into 3D-printable ink. Both volatile and non-volatile resistive switching are achieved within a single device by varying current compliance, which enables the implementation of electronic synapse with neuromorphic functionality including short-term plasticity (STP) and long-term plasticity (LTP).

SESSION 9

Ge & SiGe FET [Shunju I]

Wednesday, June 12, 10:30-12:35

Chairpersons: K. Tomida, Sony Semiconductor Solutions Corp.
S-C. Song, Qualcomm Inc.

T9-1 - 10:30
A Record G_{mSAT}/SS_{SAT} and PBTI Reliability in Si-Passivated Ge nFinFETs by Improved Gate Stack Surface Preparation, H. Arimura, D. Cott, G. Boccardi, R. Loo, K. Wostyn, S. Brus, E. Capogreco, A. Opdebeeck, L. Witters, T. Conard, S. Suhard, D. van Dorp, K. Kenis and L.-A. Ragnarsson, J. Mitard, F. Holsteyns, V. De Heyn, D. Mocuta, N. Collaert and N. Horiguchi, imec, Belgium

We have demonstrated Ge nFinFETs with a record high $G_{m,SAT}/SS_{,SAT}$ and PBTI reliability by improving the RMG high-k last process. The SiO_2 dummy gate oxide (DGO) deposition and removal processes have been identified as knobs to improve electron mobility and PBTI reliability even with a nominally identical Si-passivated Ge gate stack. Surface oxidation of Ge channel during the DGO deposition is considered to impact the final gate stack. By suppressing the Ge channel surface oxidation, increasing mobility with decreasing fin width is obtained, whereas PBTI reliability, D_{IT} of scaled fin as well as high-field mobility are improved by extending the DGO in-situ clean process, resulting in the record $G_{m,SAT}/SS_{,SAT}$ of 5.4 at 73 nm Lg.

T9-2 - 10:55
High Performance Strained Germanium Gate All Around P-Channel Devices with Excellent Electrostatic Control for Sub-30nm L_G, E. Capogreco*, H. Arimura*, L. Witters*, A. Vohra*,**, C. Porret*, R. Loo*, A. De Keersgieter *, E. Dupuy*, D. Marinov*, A. Hikavyy*, F. Sebaai*, G. Mannaert*, L.-A. Ragnarsson*, Y. K. Siew*, C. Vrancken*, A. Opdebeeck*, J. Mitard*, R. Langer*, E. Altamirano Sanchez*, F. Holsteyns*, S. Demuynck*, K. Barla*, V. De Heyn*, D. Mocuta*, N. Collaert* and N. Horiguchi*, *imec and **KU Leuven, Belgium

This paper demonstrates high performance strained p-type double stacked Ge Gate-All-Around (GAA) devices at significantly reduced gate lengths (L_G~25nm) compared to our previous work. Excellent electrostatic control is maintained down to L_G=25nm by using extension-less scheme, while the performance is kept by appropriate spacer scaling and implementation of highly B-doped Ge or GeSn as source/drain (S/D) material.

T9-3 - 11:20
SiGe Channel CMOS: Understanding Dielectric Breakdown and Bias Temperature Instability Tradeoffs, R. G. Southwick III, M. Wang, S. Mochizuki, X. Miao, J. Li and C. H. Lee, IBM Research, USA

Breakdown and bias temperature instability for n/pFETs are studied on a wide composition of SiGe channels on different strain relaxation buffers. This study represents the first in-depth look at AC/DC PBTI trends of low Ge% SiGe nFinFETs. Dielectric breakdown is shown to be largely independent of channel composition over the re-gion studied. Finally, we calculate the end-of-life performance benefit compared to Si, demonstrating the potential benefit of CMOS SiGe as a technology element.

T9-4 - 11:45
Channel Strain Dependence of Tinv in Strained Si and $Si_{1-x}Ge_x$ FETs: Internal Strain-Induced Modification of Chemical Oxidation, C. H. Lee, S. Mochizuki, X. Miao, J. Li and R. G. Southwick III, IBM Research, USA

Self-limiting chemical oxidation behaviors on SiGe channels with biaxial and uniaxial strain are studied to understand the role of the internal channel strain in the interfacial layer (IL) formation. Biaxial strain accelerates chemical oxidation on Si and SiGe regardless of Ge content in the channel, forming a thicker IL in planar FETs. On the other hand, chemical oxidation is not sensitive to uniaxial strain thanks to the less strain in the out-of-plane direction, forming a thinner IL in FinFETs. The universal relationship of Tinv and channel strain from both planar FETs and FinFETs is discussed.

T9-5 - 12:10
Improvement of SiGe MOS Interface Properties with A Wide Range of Ge Contents by Using TiN/Y_2O_3 Gate Stacks with TMA Passivation, T.-E. Lee, K. Kato, M. Ke, M. Takenaka and S. Takagi, The Univ. of Tokyo, Japan

We demonstrate the low interface trap density at SiGe p-MOS interfaces with TiN/Y_2O_3 gate stacks by employing the Trimethylaluminum (TMA) passivation. PMA temperature is optimized to maximize scavenging of GeO_x. The impact of the gate electrode among TiN, Al, Au and W is studied for Y_2O_3/SiGe interfaces. The TiN/Y_2O_3/ SiGe interfaces with PMA at 450oC minimize interface trap density (D_{it}), hysteresis and gate leakage current. TMA passivation is found to further improve the interfacial properties. The record-low minimum D_{it} of 2.7×10^{10}, 5.4×10^{10}, 1.7×10^{11}, 2.0×10^{11}, 7.4×10^{11} and 4.2×10^{12} $eV^{-1}cm^{-2}$ are obtained for SiGe MOS interfaces with the Ge contents of 0.13, 0.22, 0.32, 0.38, 0.49, and 0.62, respectively.

SESSION 10

Advanced FinFET & GAA I [Shunju II, III]

Wednesday, June 12, 14:00-15:40

Chairpersons: K. Maekawa, Renesas Electronics Corp.
Y. Liang, nVidia

T10-1 - 14:00
7nm Mobile SoC and 5G Platform Technology and Design Co-Development for PPA and Manufacturability, M. Cai*, H. Park*, J. Yang*, Y. Suh*, J. Chen*, Y. Gao*, L. Chang*, J. Zhu*, S. Song*, J. Choi*, G. Chen*, B. Yu*, X.-Y. Wang*, W. Chung**, V. Huang*, G. Reddy*, N. Kelageri*, D. Kidd*, P. Penzes*, S. H. Yang**, S. B. Lee**, B. Z. Tien**, G. Nallapati*, S.-Y. Wu** and P. R. Chidambaram*, *Qualcomm Technologies, Inc., USA and **TSMC, Taiwan

We report on Qualcomm Snapdragon SDM855 mobile SoC and world's first commercial 5G platform using industry-leading 7nm FINFET technologies. SDM855 exhibits >30% CPU performance gain over the previous generation thanks to a new design architecture enabled by dual poly pitch process integration. Low voltage operation and tight spread in power consumption has been achieved through process and design co-development, delivering a high performance and low power solution for both mobile and AI applications. Extending the 7nm technology with 2nd-year process enhancement demonstrates up to 50mV CPU Vmin reduction without any change to de-sign rules, which paves the road for an integrated 5G mobile platform with >10Gbps connectivity.

T10-2 - 14:25
Accurate High-Sigma Mismatch Model for Low Power Design in Sub-7nm Technology, T. H. Choi*,**, H. Choi*, J. Choi*, H. Choo*, H. Jung*, H. Kim*, T. Song*, J. Kye* and S.-O. Jung**, *Samsung Electronics Co., Ltd. and **Yonsei Univ., Korea

High-sigma yield simulation analysis based on accurate SPICE mismatch model is required for high volume product design. Especially for the low power design in sub-7nm technology, the non-Gaussian behavior of the transistor drain currents (I_{ds}) is intensifying due to large mismatch variation. To achieve reliable high-sigma simulation, SPICE mismatch model needs to accurately reflect the non-Gaussian I_{ds} distribution obtained from the silicon data. Gaussian distribution modeling of channel resistance factor (R_{ch_f}) and source/drain external resistance (R_{ext}) is proven to be effective to model the skewed Gaussian distribution shape of massive silicon Ids data.

T10-3 - 14:50
Sub-10 nm Advanced FinFET Design for Different Applications in Various Vdd and Temperature Operation Ranges, S. Kim*,**, S. K. Kim*, J. C. Kim*, B. H. Choi*, B.-G. Park**, Y. Y. Masuoka* and S. D. Kwon*, *Samsung Electronics Co., Ltd. and **Seoul National Univ., Korea

An advanced FinFET design is identified to improve both variation and minimum operation voltage (V_{min}) in various temperature and supply voltage (V_{dd}) ranges, using sub-10 nm FinFET transistors. Through a clarification of each electrical parameter impact on both variation and operation voltage, a suitable FinFET design is successfully demonstrated to reduce I_{eff} variation by 0.4x, as well as Idoff variation by 0.8x in various V_{dd} ranges. This paper also provides Tr. design to improve V_{min} by 35 mV with the switching energy 0.87x reduction.

T10-4 - 15:15
Fin Bending Mitigation and Local Layout Effect Alleviation in Advanced FinFET Technology Through Material Engineering and Metrology Optimization, T.-Y. Wen*, B. Colombeau**, C.-I. Li*, S.-Y. Liu*, B. Guo**, H. v. Meer**, C.-C. Huang*, H.-P. Chen*, C.-W. Huang*, J.-C. Lin*, K. Shim**, I. Holcman**, K. Nafisi**, J. Fernandez**, M. Hou****, B. Yang****, H. C. Feng*, C. F. Hsu*, Y. T. Tasi*, S. A. Huang*, C. H. Chen*, J. Kuo****, S. Lee****, D. Fung**, N. H. Yang*, J. Y. Wu* and G. C. Hung*, *United Microelectronics Corp., Taiwan and **Applied Materials, Inc., USA

In advanced FinFET devices, STI gap fill and ILD_0 stress are responsible for fin defects, fin bending as well as device performance degradations due to the local layout effect (LLE). In this paper, for the first time, we look at different ways to modulate the stress from the Flowable CVD (FCVD) films either by additional UV treatment and/or ion beam treatment (hot Helium implantation). By leveraging in-line e-beam metrology capabilities of PROVision for massive measurements of critical dimensions (CDs), the process impact on fin spacing and LLEs are characterized and analyzed. Significant improvement for LLE is observed for nFET device which correlates to fin bending improvement. In addition, ~5% drive current gain for pFET is observed after ILD_0 stress optimization.

SESSION 11

Embedded Memory [Shunju I]

Wednesday, June 12, 14:00-15:40

Chairpersons: K. Tateiwa, TowerJazz Panasonic Semiconductor Co., Ltd.
Y. Pan, Lam Research

T11-1 - 14:00
High-Speed and Ultra-Low Power IoT One-Chip (MCU + Connectivity-Chip) on a Robust 28-nm Embedded Flash Process, C. Jeon*, J. Woo*, K. Yeom*, S. Lee*, H. Min*, C. Kim**, H. Sung**, S. Yoon**, E. S. Jung**, Y. K. Lee*, K. C. Park*, G. Jeong*, J. Yoon*, E. Jung*, M. Seo*, E. Hong*, Y. Jeong*, D. Kim*, H. C. Lee*, S. Cho*, M. H. Oh*, J.-S. Kim*, H. Lee*, J. C. Park* and J. Kim**, *Foundry Business, Samsung Electronics Co., Korea and **SYS. LSI Business, Samsung Electronics Co., Korea

Based on robust 28-nm embedded flash (eFlash) process, IoT One-chip for high-speed and low power applications which MCU-chip (10Mb eFlash) and connectivity-chip (BLE/Zigbee) are integrated for the first time. By introducing new devices on 28-nm low-power eFlash process, high-speed (>40MHz random read), ultra-low power (<3uA sleep mode current, 10/13mA RF current at Tx/Rx mode) and robust reliability (-40~125°C stable operation, 100K cycle endurance, 150C/RT retention up to 200K hours) are achieved. LDD-first IO transistor with low Vth (~0.5V) for low-Vdd (~1.0V) operation and ultra-low leakage (ULL) SRAM bit-cell (0.1x *vs*. normal) supporting low sleep mode chip current are applied to extend battery life-time. Stable endurance and high (/low)-temperature retention after cycling stress are achieved by robust split-gate type eFlash cell.

T11-2 - 14:25
Turning Logic Transistors into Secure, Multi-Time Programmable, Embedded Non-Volatile Memory Elements for 14 nm FINFET Technologies and Beyond, F. Khan, D. Moy, D. Anand, E. H. Schroeder, R. Katz, L. Jiang, E. Banghart, N. Robson and T. Kirihata, GLOBALFOUNDRIES Inc., USA

Described is a secure, multi-time programmable memory (MTPM) solution for the 14 nm FINFET node and beyond, which turns as-fabricated standard logic transistors into embedded non-volatile memory (eNVM) elements, without the need for any process adders or additional masks. These logic transistors, when employed as eNVM elements, are dubbed "Charge Trap Transistors" (CTTs). Outlined are the technological breakthroughs required for employing logic transistors as an MTPM. An erase technique, called "Self-heating Temperature Assisted eRase" (STAR), is introduced which enables 100% erase efficiency, as compared to < 50% erase efficiency using conventional methods, in turn enabling MTPM functionality in CTTs. For the first time, hardware results demonstrate an endurance of > 10^4 program/erase cycles. Data retention lifetime of > 10 years at 125°C and scalability to 7 nm have been confirmed.

T11-3 - 14:50
Embedded PUF on 14nm HKMG FinFET Platform: A Novel 2-Bit-Per-Cell OTP-Based Memory Feasible for IoT Secuirty Solution in 5G Era, E. R. Hsieh*,****, H. W. Wang**, C. H. Liu**, S. Chung*, T. P. Chen***, S. A. Huang***, T. J.Chen*** and O. Cheng***, *National Chiao Tung Univ., **National Taiwan Normal Univ., ***United Microelectronics Corp., Taiwan and ****Stanford Univ., USA

In this work, a novel concept of 2-bit-per-cell (2B/C) is introduced to realize high-density OTP PUF from a new scheme of dielectric breakdown. This PUF shows 10^5x of large window, good immunity to high-temperature disturbance, and excellent retention under 150°C baking, which are particularly for automotive applications. In terms of security, this PUF exhibits near ideal normal distribution of hamming distance and narrow distribution of hamming weight. The bit error rates are low, 0.78% at 25°C and 1.95% at 150°C, benchmarked on a 256-bit array. Finally, the security test of this PUF against the hackers attack from the machine learning process has been proved to have high security. Overall, the proposed 2B/C OTP PUF demonstrated great potential for IoT security in 5G era.

T11-4 - 15:15
Novel Quad Interface MTJ Technology and Its First Demonstration with High Thermal Stability and Switching Efficiency for STT-MRAM Beyond 2Xnm, K. Nishioka, H. Honjo, S. Ikeda, T. Watanabe, S. Miura, H. Inoue, T. Tanigawa, Y. Noguchi, M. Yasuhira, H. Sato and T. Endoh, Tohoku Univ., Japan

We have proposed novel quad-interface magnetic tunnel junction (MTJ) technology which brings forth an increase of both thermal stability factor Δ and switching efficiency Δ/I_{C0} by a factor of 1.5-2 compared with conventional double-interface MTJ technology. We successfully fabricated the quad-interface MTJ using 300mm process based on novel low damage integration process including PVD, RIE and so on. By developing the quad-interface MTJ, we have achieved about two times larger Δ and Δ/I_{C0}. Moreover, we have achieved about two times larger TMR ratio/*RA* by the stack development specific for the quad-interface MTJ technology. The developed quad-interface MTJ technology regarded as post-double-interface MTJ technology will become an essential technology for the scaling of the STT-MRAM beyond 20nm.

Technology / Circuits Joint Focus Session 1

New Computing [Suzaku III]

Wednesday, June 12, 14:00-15:40

Chairpersons: M. Yamaoka, Hitachi, Ltd.
A. Wang, Psikick

JFS1-1 - 14:00 (Invited)
A Cloud-Ready Scalable Annealing Processor for Solving Large-Scale Combinatorial Optimization Problems, M. Hayashi, T. Takemoto, C. Yoshimura and M. Yamaoka, Hitachi, Ltd., Japan

This paper presents a CMOS annealing processor (CMOS-AP) that accelerates ground state searches of the Ising model. The main feature of this processor is its inter-chip connection interface for making a larger chip. A credit card sized compute node integrating two CMOS-APs was also developed as an interface with existing computer systems. The compute node can handle up to 61,952 spins at a time. A performance evaluation using the node improved the CPU speed by 55 times in solving a minimum vertex cover problem, one of the NP-hard combinatorial optimization problems. Finally, we describe a cloud interface for the compute node to make the CMOS-APs more useful and to promote application development for it.

JFS1-2 - 14:25
A 7.3 M Output Non-Zeros/J Sparse Matrix-Matrix Multiplication Accelerator Using Memory Reconfiguration in 40 nm, S. Pal*, D.-H. Park*, S. Feng*, P. Gao**, J. Tan*, A. Rovinski*, S. Xie**, C. Zhao**, A. Amarnath*, T. Wesley*, J. Beaumont*, K.-Y. Chen*, C. Chakrabarti***, M. Taylor**, T. Mudge*, D. Blaauw*, H.-S. Kim* and R. Dreslinski*, *Univ. of Michigan, **Univ. of Washington and ***Arizona State Univ., USA

A Sparse Matrix-Matrix multiplication (SpMM) accelerator with 48 heterogeneous cores and a reconfigurable memory hierarchy is fabricated in 40 nm CMOS. On-chip memories are reconfigured as scratchpad or cache and interconnected with synthesizable coalescing crossbars for efficient memory access in each phase of the algorithm. The 2.0 mm x 2.6 mm chip exhibits 12.6x (8.4x) energy efficiency gain, 11.7x (77.6x) off-chip bandwidth efficiency gain and 17.1x (36.9x) compute density gain against a high-end CPU (GPU) across a diverse set of synthetic and real-world power-law graph based sparse matrices.

JFS1-3 - 14:50
Spoken Vowel Classification Using Synchronization of Phase Transition Nano-Oscillators, S. Dutta, A. Khanna, W. Chakraborty, J. Gomez, S. Joshi and S. Datta, Univ. of Notre Dame, USA

The paradigm of biologically-inspired computing endows the components of a neural network with dynamical functionality, such as self-oscillations, and harnesses emergent physical phenomena like synchronization, to learn and classify complex temporal patterns. In this work, we exploit the synchronization dynamics of a network of ultra-compact, low power Vanadium dioxide (VO_2) based insulator-to-metal phase-transition nano-oscillators (IMT-NO) to classify complex temporal pattern for speech discrimination. We successfully train a network of four capacitively coupled IMT- NOs to recognize spoken vowels by tuning their oscillation frequencies electrically according to a real-time learning rule and achieve high recognition rates of 90.5% for spoken vowels. Such an energy-efficient compact hardware with a small number of functional elements are a promising technology option for edge artificial intelligence.

JFS1-4 - 15:15
A 250mW 5.4G-Novel-Pixel/s Photorealistic Refocusing Processor for Full-HD Five-Camera Applications, P.-H. Chen, S.-W. Yang, S.-Y. Huang, L.-D. Chen and C.-T. Huang, National Tsing Hua Univ., Taiwan

In this paper, we present an integrated circuit which supports Full-HD photorealistic refocusing. In contrast to the conventional single-image blurring, it provides physically-correct bokeh effect by rendering and then averaging hundreds of novel views from five images taken in different perspectives. To address the huge requirement of DRAM bandwidth and computing power, we adopt a block-based multi-rate framework and further propose two techniques: four-direction view generation and highly-parallel view rendering. The former provides a compact system architecture to save 32% of SRAM area and 92% of DRAM bandwidth without noticeable quality degradation. The latter efficiently generates 5.4G novel pixels per second to provide high-quality refocusing. This chip is fabricated in 40nm CMOS process, and the core area is 3.61 mm^2. It consumes 250mW when operating at 200MHz and 0.9V to support Full-HD photorealistic refocusing up to 40 fps.

SESSION 12

AI II [Shunju II, III]

Wednesday, June 12, 16:00-17:40

Chairpersons: T. Tanaka, Tohoku Univ.
S. Datta, Univ. of Notre Dame

T12-1 - 16:00
Split-Gate FeFET (SG-FeFET) with Dynamic Memory Window Modulation for Non-Volatile Memory and Neuromorphic Applications, V. P.-H.Hu*, H.-H. Lin*, Z.-A. Zheng*, Z.-T. Lin*, Y.-C. Lu*, T.-Y. Ho*, Y.-W. Lee*, C.-W. Su* and C.-J. Su**, *National Central Univ. and **Taiwan Semiconductor Research Institute, Taiwan

In this work, we propose a novel split-gate FeFET (SG-FeFET) with two separate external gates to dynamically modulate the memory window (MW) for non-volatile memory and neuromorphic applications. During read operation, only one gate is turned on to decrease the area ratio (A_{FE}/A_{IL}) of ferroelectric layer to insulator layer, which increases MW and read current ratio (I_{Read_1}/I_{Read_0}). During write operation (program/erase), both two gates are turned on to increase A_{FE}/A_{IL}, which decreases MW, thereby resulting in lower write voltage (V_{Write}). Compared to FeFET, SG-FeFET (1) Demonstrates lower V_{Write} (1.85V) and 59.5% reduction in write energy at fixed I_{Read_1}/I_{Read_0}; (2) Exhibits lower read energy (-11.3%) and higher I_{Read_1}/I_{Read_0} (8.6E6) at fixed V_{Write}; (3) Allows random access and eliminates half-select disturb; (4) Preserves higher endurance due to lower V_{Write} and charge trapping. SG-FeFET as synaptic device also exhibits superior symmetry and linearity for potentiation and depression process.

T12-2 - 16:25
Bio-Inspired Neurons Based on Novel Leaky-FeFET with Ultra-Low Hardware Cost and Advanced Functionality for All-Ferroelectric Neural Network, C. Chen, M. Yang, S. Liu, T. Liu, K. Zhu, Y. Zhao, H. Wang, Q. Huang and R. Huang, Peking Univ., China

For the brain-inspired neuromorphic computing, various emerging memory devices, including FeFET, have been applied to develop the artificial synapses, while the artificial neurons are still mostly CMOS-implemented and suffer from high-hardware-cost issue, especially when expanding advanced functions. In this work, a novel leaky-FeFET (L-FeFET) based on partially crystallized $Hf_{0.5}Zr_{0.5}O_2$ layer is designed to mimic biological neurons. For the first time, we propose and experimentally demonstrate a capacitor-less L-FeFET neuron for basic leaky-integrate-and-fire function with ultra-low hardware cost of only one transistor and one resistor. Furthermore, a new hybrid L-FeFET-CMOS neuron is implemented to expand advanced spike-frequency adaption with almost half of hardware cost compared with CMOS neuron. This work provides a highly-integrated and inherently-low-energy implementation for neuron and the possibility for all-ferroelectric neural networks.

T12-3 - 16:50
A Novel Architecture to Build Ideal-Linearity Neuromorphic Synapses on a Pure Logic FinFET Platform Featuring 2.5ns PGM-Time and 10^{12} Endurance, E. R. Hsieh*.***, H. Y. Chang*, S. Chung*, T. P. Chen**, S. A. Huang**, T. J. Chen**, O. Cheng** and S. S. Wong***, *National Chiao Tung Univ., **United Microelectronics Corp., Taiwan and ***Stanford Univ., USA

We will explore pure logic FinFET devices to realize the functionality of linear weight tuning capability as electric synapses. The unit cell of this new FinFET synapse is composed of two identical FinFETs in series, one serves as control and the other one as storage. This new FinFET synapse exhibits ideal linearity with nearly infinity training cycles (>10^{12}), much lower programming voltage, 0.85V, and faster speed, 2.5ns. It can also analogically increase or decrease the transistor V_{th} to vary the drain conductance. For its analog performance, it performs excellent linearity and a wide tuning-window (20x) of weight-tuning. 1kb synaptic array has been designed. The Spice-simulated results have shown that new FinFET synaptic array can expand the array size to 64x64, given 300x of SNR, w.r.t. that of RRAM array. Finally, the training accuray can achieve 97.43% accuracy as high as the GPU one does.

T12-4 - 17:15
Biologically Plausible Energy-Efficient Ferroelectric Quasi-Leaky Integrate and Fire Neuron, S. Dutta*, A. Saha**, P. Panda**, W. Chakraborty*, J. Gomez*, A. Khanna*, S. Gupta**, K. Roy** and S. Datta*, *Univ. of Notre Dame and **Purdue Univ., USA

Biologically plausible mechanism like homeostasis compliments Hebbian learning to allow unsupervised learning in spiking neural networks[1]. In this work, we propose a novel ferroelectric-based quasi-LIF neuron that induces intrinsic homeostasis. We experimentally characterize and perform phase-field simulations to delineate the non-trivial transient polarization relaxation that underlines the Q-LIF behavior. Performing network level simulations with our Q-LIF neuron model exhibits a 2.3x reduction in firing rate compared to traditional LIF neuron while maintaining iso-accuracy of 84- 85% across varying network sizes. Such an energy-efficient hardware for spiking neuron can enable ultra-low power data processing in energy constraint environments like health monitoring with wearable systems.

SESSION 13

Process [Shunju I]

Wednesday, June 12, 16:00-17:40

Chairpersons: T. Tsunomura, Tokyo Electron Ltd.
B. Colombeau, Applied Materials, Inc.

T13-1 - 16:00
Gate-Cut-Last in RMG to Enable Gate Extension Scaling and Parasitic Capacitance Reduction, A. Greene*, H. Zhou*, R. Xie*, C. Park*, L. Economikos**, V. Chan*, K. Akarvardar**, R. Bao*, I. Seshadri*, R. Conti*, M. Wang*, M. Sankarapandian*, J. Demarest*, J. Li*, L. Jiang*, K. Zhao*, R. Robison*, T. Ando*, N. Cave**, A. Knorr**, D. Gupta*, S. Kanakasabapathy***, D. Guo*, B. Haran*, V. Basker* and H. Bu*, *IBM Research, **GLOBALFOUNDRIES Inc., USA and ***Currently at LAM Research

In this paper, we present for the first time a Gate Cut Last integration scheme completed within the Replacement Metal Gate (RMG) module. This novel gate cut (CT) technique allows the scaling of gate extension length past the end fin which reduces parasitic capacitance, leakage and performance variation. In addition, we demonstrate that CT in RMG is a promising alternative integration process that can enable scaling for future logic technology nodes. Device, circuit and reliability results are shown to compare this novel CT in RMG process to the conventional gate cut method.

T13-2 - 16:25
Direct Partition Measurement of Parasitic Resistance Components in Advanced Transistor Architectures, Z. Liu, H. Wu, C. Zhang, X. Miao, H. Zhou, R. Southwick, T. Yamashita and D. Guo, IBM Research, USA

More-Moore logic device technology roadmap suggests Lateral/Vertical Gate-All-Around (LGAA / VGAA) device architectures beyond FinFETs for further scaling and performance. At extremely scaled gate pitches, parasitic resistance significant impacts the performance of the devices. Direct partition measurement of the resistance components in FinFETs has been established. Stacked LGAA devices at further scaled gate pitches exhibit high S/D series resistance and contact resistance which can be partitioned with similar Kelvin measurement. VGAA transistors have a very different structure from FinFETs or LGAAs. Their asymmetric bottom and top S/D results in significant spreading resistance and different contact resistance values. Separate partition of the resistances at the bottom and top is needed. In this paper, VGAA test structures and measurement methodology is introduced for partitioning the resistance components.

T13-3 - 16:50
Self-Aligned Gate Contact (SAGC) for CMOS Technology Scaling Beyond 7nm, R. XIE*, C. Park*, R. Conti*, R. Robison*, H. Zhou*, I. Saraf*, A. Carr*, S. C. Fan*, K. Ryan**, M. Belyansky*, S. Pancharatnam*, A. Young*, J. Wang*, A. Greene*, K. Cheng*, J. Li*, R. Conte*, H. Tang*, K. Choi*, H. Amanapu*, B. Peethala*, R. Muthinti*, M. Raymond**, C. Prindle**, Y. Liang**, S. Tsai**, V. Kamineni**, A. Labonte**, N. Cave**, D. Gupta*, V. Basker*, N. Loubet*, D. Guo*, B. Haran*, A. Knorr* and H. Bu*, *IBM Research and **GLOBALFOUNDRIES Inc., USA

We demonstrate a novel self-aligned gate contact (SAGC) scheme with conventional oxide/nitride materials that allows superior process integration for scaling while simplifying the SRAM cross-couple wiring. We show that the key feature to avoid both gate-contact (CB) to source-drain local interconnect (LI) shorts and the LI contact (CA) to gate shorts is the shape of the LI cap. A trapezoid-shaped oxide (SiO_2) LI cap with an appropriate taper angle eliminates shorting between the contacts in the gate and source-drain region. We further demonstrate that this oxide LI cap is fully compatible with Cobalt (Co) metallization with a novel selective tungsten (W) growth process. Additionally, this process enables the SRAM cross-couple (XC) in the same metallization level, eliminating the need for an upper level wiring and greatly simplifying routing in the SRAM cell.

T13-4 - 17:15
A Novel Fast-Turn-Around Ladder TLM Methodology with Parasitic Metal Resistance Elimination, and 2×10^{-10} Ω-cm² Resolution: Theoretical Design and Experimental Demonstration, Y. Wu*, H. Xu*, L.-H. Chua**, K. Han*, W. Zou**, T. Henry**, J. Zhang*, C. Wang*, C. Sun* and X. Gong*, *National Univ. of Singapore, Singapore and **Applied Materials, Inc., USA

A novel ladder transmission line method (LTLM) that features eliminated parasitic resistance from contact metal and access electrodes, simple fabrication process, and 2×10^{-10} Ω-cm² resolution for highly-accurate extraction of specific contact resistivity (ρ_c) in the ~10^{-10} to 10^{-9} Ω-cm² regime is demonstrated. The current distribution and extraction of ρ_c in LTLM are verified by TCAD and numerical distributive-resistor-network method, respectively. The extraction error caused by the current spreading and crowding in LTLM are modeled, and design guidelines to achieve 10^{-10} Ω-cm² resolution for ρ_c extraction are provided. By applying LTLM to the Ni p^+-$Ge_{0.95}Sn_{0.05}$ contact, a record-low ρ_c down to 4.0×10^{-10} Ω-cm² was obtained. LTLM is insensitive to variation of metal resistance, unlike the refined TLM (RTLM) which could overestimate ρ_c by at least tens of times.

Technology / Circuits Joint Focus Session 2

IoT & Sensor [Suzaku III]

Wednesday, June 12, 16:00-18:05

Chairpersons: M. Hashimoto, Osaka Univ.
D. Markovic, Univ. of California, Los Angeles

JFS2-1 - 16:00
Integrated Power Management and Microcontroller for Ultra-Wide Power Adaptation Down to nW, L. Lin, S. Jain and M. Alioto, National Univ. of Singapore, Singapore

This paper presents a power management unit (PMU) driving a microcontroller, and controlling a power knob that enables adaptation to the sensed power availability over an ultra-wide range, well beyond voltage scaling. Conventional battery-powered operation is augmented with pure harvesting. Wide power adaptation is enabled by comparator delay self-biasing and zero-current switching scheme shared among all power modes with single-cycle convergence.

JFS2-2 - 16:25
A 10mm^3 Light-Dose Sensing IoT^2 System with 35-to-339nW 10-to-300klx Light-Dose-to-Digital Converter, I. Lee*, E. Moon*, Y. Kim*,**, J. Phillips* and D. Blaauw*,**, *Univ. of Michigan and **CubeWorks, Inc., USA

This paper presents a 10mm^3 Internet-of-Tiny-Things (IoT^2) system that measures light dose using custom photovoltaic cells and a light-dose-to-digital converter (LDDC). The LDDC nulls diode leakage for temperature stability and creates headroom without power overhead by dual forward-biased photovoltaic cells. It also adaptively updates the current mirror ratio and accumulation weighting factor for a low, near-constant power consumption. The system can operate energy-autonomously at >500lx light level. The LDDC achieves a 3-sigma inaccuracy of ±3.8% and σ/μ of 2.4% across a wide light intensity range from 10lx to 300klx while consuming only 35 - 339nW.

JFS2-3 - 16:50
Low-Power and ppm-Level Detection of Gas Molecules by Integrated Metal Nanosheets, T. Tanaka*, K. Tabuchi*, K. Tatehora*, Y. Shiiki*, S. Nakagawa*, T. Takahashi**, R. Shimizu*, H. Ishikuro*, T. Kuroda*, T. Yanagida** and K. Uchida*,***, *Keio Univ., **Kyushu Univ. and ***The Univ. of Tokyo, Japan

Ppm-level hydrogen and ammonia in air were recognized by low-power, integrated sensors consisting of catalytic metal nanosheets. Thermal energy necessary for catalytic reactions were given by Joule heating not by external heaters. The thermal-aware design of sensors reduces the power consump-tion to 0.14 mW. The low-power and small-area properties enable large-scale, on-chip integration of molecular sensors, which will be useful in IoT era. A sensor array was successful-ly connected to a platform with wireless connectivity.

JFS2-4 - 17:15
Record-High Performance Trantenna Based on Asymmetric Nano-Ring FET for Polarization-Independent Large-Scale/ Real-Time THz Imaging, E.-S. Jang*, M. W. Ryu*, R. Patel*, S. H. Ahn*, H. J. Jeon*, K. Han** and K. R. Kim*, *Ulsan National Institute of Science and Technology and **Dongguk Univ., Korea

We demonstrate a record-high performance monolithic trantenna (transistor-antenna) using 65-nm CMOS foundry in the field of a plasmonic terahertz (THz) detector. By applying ultimate structural asymmetry between source and drain on a ring FET with source diameter (d_S) scaling from 30 to 0.38 micrometer, we obtained 180 times more enhanced photoresponse (Δu) in on-chip THz measurement. Through free-space THz imaging experiments, the conductive drain region of ring FET itself showed a frequency sensitivity with resonance frequency at 0.12 THz in 0.09 ~ 0.2 THz range and polarization-independent imaging results as an isotropic circular antenna. Highly-scalable and feeding line-free monolithic trantenna enables a high-performance THz detector with responsivity of 8.8 kV/W and NEP of 3.36 pW/Hz$^{0.5}$ at the target frequency.

JFS2-5 - 17:40 (Invited)
Custom Silicon and Sensors Developed for a 2nd Generation Augmented Reality User Interface, P. O'Connor, C. Meekhof, C. McBride, C. Mei, C. Bamji, D. Rohn, H. Strande, J. Forrester, M. Fenton, R. Haraden, T. Ozguner and T. Perry, Microsoft, USA.

Microsoft Hololens 2, like its predecessor, is an untethered holographic mixed reality (MR) headset that transforms the way we communicate, create, and explore. Hololens 2 advances MR ergonomics, intuitive interactions, and immersion. We describe the custom sensors and compute silicon developed to give hands-free user control of the headset and applications. With 3D Time of Flight (TOF) depth sensing, eye tracking and spatial array microphones, working with low power compute blocks aggregated in a custom ASIC, the hardware enables a comfortable, low latency user interface that sets the user free to focus on their work. We conclude with a look at how these building blocks can enable further innovation in the Intelligent Edge.

Technology / Circuits Joint Banquet [Shunju I, II, III]

Wednesday, June 12, 19:00-21:00

Technology / Circuits Joint Focus Session 3

Technology and System for AI [Shunju II, III]

Thursday, June 13, 8:30-10:10

Chairpersons: H. Wu, Tsinghua Univ.
G. Yeric, ARM Ltd.

JFS3-1 - 8:30 (Invited)
Considerations of Integrating Computing-In-Memory and Processing-In-Sensorinto Convolutional Neural Network Accelerators for Low-Power Edge Devices, K.-T. Tang*, W.-C. Wei*, Z.-W. Yeh*, T.-H. Hsu*, Y.-C. Chiu*, C.-X. Xue*, Y.-C. Kuo*, T.-H. Wen*, M.-S. Ho**, C.-C. Lo*, R.-S. Liu*, C.-C. Hsieh* and M.-F. Chang*, *National Tsing Hua Univ. and **National Chung Hsin Univ., Taiwan

In quest to execute emerging deep learning algorithms at edge devices, developing low-power and low-latency deep learning accelerators (DLAs) have become top priority. To achieve this goal, data processing techniques in sensor and memory utilizing the array structure have drawn much attention. Processing-in-sensor (PIS) solutions could reduce data transfer; computing-in-memory (CIM) macros could reduce memory access and intermediate data movement. We propose a new architecture to integrate PIS and CIM to realize low-power DLA. The advantages of using these techniques and the challenges from system point-of-view are discussed.

JFS3-2 - 8:55 (Invited)
Computational Memory-Based Inference and Training of Deep Neural Networks, A. Sebastian*, I. Boybat*,**, M. Dazzi*,***, I. Giannopoulos*,***, V. Jonnalagadda*, V. Joshi*,****, G. Karunaratne*,***, B. Kersting*,*****, R. Khaddam-Aljameh*,***, S. R. Nandakumar*,****, A. Petropoulos*,******, C. Piveteau*,***, T. Antonakopoulos******, B. Rajendran****, M. Le Gallo* and E. Eleftheriou*, *IBM Research, **EPFL, ***ETH Zürich, Switzerland, ****New Jersey Institute of Technology, USA, *****RWTH, Germany and ******Univ. of Patras, Greece

In-memory computing is an emerging computing paradigm where certain computational tasks are performed in place in a computational memory unit by exploiting the physical attributes of the memory devices. Here, we present an overview of the application of in-memory computing in deep learning, a branch of machine learning that has significantly contributed to the recent explosive growth in artificial intelligence. The methodology for both inference and training of deep neural networks is presented along with experimental results using phase-change memory (PCM) devices.

JFS3-3 - 9:20
A Ternary Based Bit Scalable, 8.80 TOPS/W CNN Accelerator with Many-Core Processing-in-Memory Architecture with 896K Synapses/mm^2, S. Okumura, M. Yabuuchi, K. Hijioka and K. Nose, Renesas Electronics Corp., Japan

A Processing-In-Memory (PIM) accelerator with ternary SRAM is proposed for low-power, large-scale deep neural network (DNN) processing. The accelerator consists of Ternary Neural Arithmetic Memory (TNAM) which is capable of bit-scalable MAC (multiply and accumulation) operation in accordance with target accuracy and power limit. An ADC less readout circuits to reduce analog-digital conversion power and a system-level variation avoidance technique utilizing features of TNAM are also proposed. A test chip with large-scale PIM is fabricated and successfully operate convolutional neural networks (CNNs) with 8.8TOPS/W and highest accuracy and area density among recent SRAM-type PIMs are obtained.

JFS3-4 - 9:45
Energy-Efficient Continual Learning in Hybrid Supervised-Unsupervised Neural Networks with PCM Synapses, S. Bianchi*, I. Muñoz-Martin*, G. Pedretti*, O. Melnic*, S. Ambrogio** and D. Ielmini*, *Politecnico di Milano, Italy and **IBM Research, USA

Artificial neural networks (ANNs) can outperform the human ability of object recognition by supervised training of synaptic parameters with large datasets. Contrarily to the human brain, however, ANNs cannot continually learn, i.e. acquire new information without catastrophically forgetting previous knowledge. To solve this issue, we present a novel hybrid neural network based on CMOS logic and phase change memory (PCM) synapses, mixing a supervised convolutional neural network (CNN) with bio-inspired unsupervised learning and neuronal redundancy. We demonstrate high classification accuracy in MNIST and CIFAR10 datasets (98% and 85%, respectively) and energy-efficient continual learning of up to 30% of non-trained classes with 83% average accuracy.

SESSION 14

GeSn Device [Shunju I]

Thursday, June 13, 8:30-10:10

Chairpersons: N. Sugii, Hitachi, Ltd.
N. Collaert, imec

T14-1 - 8:30
High Performance GeSn Photodiode on a 200 mm Ge-On-Insulator Photonics Platform for Advanced Optoelectronic Integration with Ge CMOS Operating at 2 µm Band, S. Xu*, K. Han*, Y.-C. Huang**, Y. Kang*, S. Masudy-Panah*, Y. Wu*, D. Lei *, Y. Zhao*, X. Gong* and Y.-C. Yeo*, *National Univ. of Singapore, Singapore and **Applied Materials, Inc., USA

We report the first demonstration of high performance germanium-tin (GeSn) multiple-quantum-well (MQW) photodiode (PD) on a 200 mm GeOI platform realized using a low temperature wafer bonding process. Record-low leakage of 25 mA/cm^2 was achieved for GeSn PDs using this new architecture. Both Ge p- and n-FinFETs were also realized on the GeOI platform to substantiate the promising monolithic integration of all GeOI-based photonics components with Ge CMOS on this architecture via top-down processing approach. This work paves way for advanced optoelectronic integrated circuits (OEIC) operating at 2 um band and beyond using GeSn as photo detection material for communication and sensing applications.

T14-2 - 8:55
Record Low Contact Resistivity ($4.4\times10^{-10}\Omega$-cm^2) to Ge Using *In-Situ* B and Sn Incorporation by CVD with Low Thermal Budget (≤400°C) and without Ga, F.-L. Lu*, C.-E. Tsai*, C.-H. Huang*, H.-Y. Ye*, S.-Y. Lin* and C. W. Liu*,**, *National Taiwan Univ. and **Taiwan Semiconductor Research Institute, Taiwan

The record low contact resistivity of $4.4\times10^{-10}\Omega$-cm^2 is achieved in Ti metal contact to *in-situ* B-doped GeSn using B (>1×10^{21}cm^{-3}) and Sn (>12%) segregations at the Ti and GeSn:B interface. Sn incorporation into Ge lowers the Schottky barrier height of holes. Increasing B doping at the Ti and GeSn:B interface reduces the hole tunneling distance. Thanks to the low growth temperature (305°C) of the chemical vapor deposition using Ge_2H_6, the GeSn:B with the bulk active [B] of 2.1×10^{20}cm^{-3} (>>the solid solubility of B in Ge equivalent to 5.5×10^{18}cm^{-3}) and the bulk [Sn] of 4.9% is successfully grown. Without the needs of the previously reported Ga dopants and the high temperature annealing for dopant activation, the record low contact resistivity is achieved with all the process temperatures ≤400°C.

T14-3 - 9:20
First Vertically Stacked, Compressively Strained, and Triangular $Ge_{0.91}Sn_{0.09}$ pGAAFETs with High I_{ON} of 19.3µA at V_{OV}=V_{DS}=-0.5V, G_m of 50.2µS at V_{DS}=-0.5V and Low SS_{lin} of 84mV/Dec by CVD Epitaxy and Orientation Dependent Etching, Y.-S. Huang*, H.-Y. Ye*, F.-L. Lu*, Y.-C. Liu*, C.-T. Tu*, C.-Y. Lin*, S.-Y. Lin*, S.-R. Jan* and C. W. Liu*,**, *National Taiwan Univ. and **Taiwan Semiconductor Research Institute, Taiwan

The natural etching stop on {111} facets yields the small dangling bond density and roughness, enabling low SS and high I_{ON} on {111} sidewalls of the GAA channels. In addition, the ~2% uniaxial compressive strain and [Sn]= 9% in the channel can reduce the hole effective mass. As a result, 50% improvement of I_{ON}= 120µA/µm (perimeter), and 71% improvement of G_m= 312µS/µm are achieved than our previous 3 stacked GeSn {001} nanosheets. Record high I_{ON} of 19.3µA per stack at V_{OV}=V_{DS}=-0.5V and record G_m of 50.2µS per stack at V_{DS}=-0.5V among all GeSn FinFETs and GAAFETs are achieved. The SS_{lin} as low as 84mV/dec is also obtained, 22% reduction than our previous work.

T14-4 - 9:45
First Demonstration of Complementary FinFETs and Tunneling FinFETs Co-Integrated on a 200 mm GeSnOI Substrate: A Pathway Towards Future Hybrid Nano-Electronics Systems, K. Han*, Y. Wu*, Y. Huang**, S. Xu*, E. Kong*, A. Kumar*, Y. Kang*, J. Zhang*, C. Wang*, H. Xu*, C. Sun* and X. Gong*, *National Univ. of Singapore, Singapore and **Applied Materials, Inc., USA

For the first time, complementary FinFETs and tunneling FinFETs with fin with (W_{Fin})of 20 nm and fin height (H_{Fin})of 40 nm were co-integrated on the same substrate, enabled by the formation of high quality GeSn-on-insulator (GeSnOI) substrate with 200 mm wafer size. Decent electrical characteristics were realized for both GeSn n-and p-FinFETs and n-and p-tunneling FinFETs. We also performed simulation study to show the promise of the GeSnOI platform that is not only able to suppress the off-state leakage current and improve the I_{on}/I_{off} ratio of tunneling FETs, but also capable of providing the powerful flexibility of using back bias to achieve superior electrical characteristic beyond the benefits of incorporation of Sn into Ge for tunneling FETs.

Technology / Circuits Joint Focus Session 4

The Future of Memory [Shunju II, III]

Thursday, June 13, 10:30-12:35

Chairpersons: H.-T. Lue, Macronix International Co., Ltd.
G. Hemink, Western Digital Corp.

JFS4-1 - 10:30 (Invited)
Circuit and Systems Based on Advanced MRAM for Near Future Computing Applications, S. Fujita, S. Takaya, S. Takeda and K. Ikegami, Toshiba, Japan

Recently MRAM technologies have been intensively developed. This paper describes novel solutions using advanced MRAM for near future computing applications. Three beneficial applications with MRAM are presented: energy saving, data reliability and performance improvement.

JFS4-2 - 10:55
Ag Ionic Memory Cell Technology for Terabit-Scale High-Density Application, S. Fujii*, R. Ichihara*, T. Konno*, M. Yamaguchi*, H. Seki*, H. Tanaka*, D. Zhao*, Y. Yoshimura*, M. Saitoh* and M. Koyama*, Toshiba Memory Corp., Japan

We demonstrated a cross-point memory array composed of 40nm Ag ionic memory cell with sub-μA and selectorless operation and 10-year data retention, making it a promising candidate for terabit-scale high-density memory application. Discontinuous conductive path with large and dense Ag clusters enabled 10-year retention even at sub-μA current with keeping high non-linearity in I-V. We implemented, for the first time, the improved cell into a 40nm cross-point array and demonstrated narrow read distribution which satisfies requirements for reliable array operation.

JFS4-3 - 11:20 (Invited)
Recent Progress and Next Directions for Embedded MRAM Technology, W. J. Gallagher, E. Chien, T.-W. Chiang, J.-C. Huang, M.-C. Shih, C.Y. Wang, C. Bair, G. Lee, Y.-C. Shih, C.-F. Lee, R. Wang, K.-H. Shen, J. J. Wu, W. Wang and H. Chuang, TSMC, Taiwan

MRAM can play a variety of on-chip memory roles in advanced VLSI technology spanning from high retention, solder-reflow-capable non-volatile memory (NVM) to dense non-volatile or high retention working RAMs. This paper describes results for a solder-reflow-capable MRAM NVM and for extensions that trade off high retention against speed, power, and density.

JFS4-4 - 11:45 (Invited)
The PCM Way for Embedded Non Volatile Memories Applications, P. Zuliani, A. Conte and P. Cappelletti, STMicroelectronics, Italy

A comparative analysis of different Resistive Memories proposed as Non Volatile Memories for embedded applications is here presented. Based on today scenario of industry-standard Floating Gate solutions, key factors as performances, reliability and technology maturity are considered when facing more innovative memory cells. In particular the race seems to be open at 28nm, where different players are proposing different memories integrated in the Back End Of the Line. Original results obtained on multi-megabits array integrating Phase Change Memories are here discussed covering cell scalability, High Temperature data retention and extended endurance capability, all in line with eNVM application requirements.

JFS4-5- 12:10 (Late News)
Manufacturable 300mm Platform Solution for Field-Free Switching SOT-MRAM, K. Garello, F. Yasin, H. Hody, S. Couet, L. Souriau, S. H. Sharifi, J. Swerts, R. Carpenter, S. Rao, K. Sethu, J. Wu, D. Crotti, A. Furnémont, G. S. Kar, W. Kim, M. Pak and N. Jossart, imec, Belgium

We propose a field-free switching SOT-MRAM concept that is integration friendly and allows for separate optimization of the field component and SOT/MTJ stack properties. We demonstrate it on a 300 mm wafer, using CMOS-compatible processes, and we show that device performances are similar to our standard SOT-MTJ cells: reliable sub-ns switching with low writing power across the 300mm wafer. Our concept/design opens a new area for MRAM (SOT, STT and VCMA) technology development.

SESSION 15

Advanced FinFET & GAA II [Shunju I]

Thursday, June 13, 10:30-12:35

Chairpersons: H. Morioka, Socionext Inc.
W. Rachmady, Intel Corp.

T15-1 - 10:30
12-EUV Layer Surrounding Gate Transistor (SGT) for Vertical 6-T SRAM: 5-nm-Class Technology for Ultra-Density Logic Devices, M. S. Kim*, N. Harada**, Y. Kikuchi*, J. Boemmels*, J. Mitard*, T. Huynh-Bao*, P. Matagne*, Z. Tao*, W. Li*, K. Devriendt*, L.-A. Ragnarsson*, C. Lorant*, D. Mocuta*, F. Masuoka**, F. Sebaai*, C. Porret*, E. Rosseel*, A. Dangol*, D. Batuk*, G. Martinez-Alanis*, J. Geypen*, N. Jourdan*, A. Sepulveda*, H. Puliyalil*, G. Jamieson*, M. van der Veen*, L. Teugels*, Z. El-Mekki*, E. Altamirano-Sanchez*, Y. Li** and H. Nakamura**, *imec, Belgium and **Unisantis, Singapore

For the first time, we establish a fabrication process flow of an EUV-era ultra-density 6-surrounding-gate-transistor SRAM with 0.0205 μm^2 unit cell area and demonstrate nMOS surrounding-gate-transistor function. In this paper, 6-surrounding-gate-transistor SRAM design layout is shown, and the fabrication process flow and key process steps are explained in detail. NMOS functional device characteristics of surrounding-gate-transistor is analyzed.

T15-2 - 10:55
Self-Heating Temperature Behavior Analysis for DC - GHz Design Optimization in Advanced FinFETs, S.-L. Liu, J. J. Horng, A. Akundu, Y. C. Hsu, B. S. Lien, S. F. Liu, C. W. Chang, H. D. Hsieh, D. S. Huang, Y. C. Peng, S. Liu and M. Chen, TSMC, Taiwan

This paper presents an 3D thermal impedance network approach to study self-heating effects in advanced FinFETs that are difficult to be analyzed in conventional models: (i) temperature distribution analysis for large FinFET devices used in high current drivers, (ii) transient thermal modeling for heat accumulation in GHz digital circuits, and (iii) investigation for layout methods to reduce FinFET self-heating temperature.

T15-3 - 11:20
Economics of Semiconductor Scaling, A Cost Analysis for Advanced Technology Node, A. Mallik, J. Ryckaert, R.-H. Kim, P. Debacker, S. Decoster, F. Lazzarino, R. Ritzenthaler, N. Horiguchi, D. Verkest and A. Mocuta, imec, Belgium

Moores law, the principle that has powered semiconductor scaling for the past 50 years is nearing its end. However, the industry would like to pursue a dimensional scaling roadmap to reap the full benefit of technology innovation. Results shown on this paper demonstrate traditional dimensional scaling approaches involving multi-patterned lithography would skyrocket the manufacturing cost. Design level techniques collectively known as scaling boosters, and innovative Complementary FET (CFET) devices would help to reduce the cost of the technology nodes. To the best of our knowledge, this is the first approach where semiconductor node transitions are benchmarked based on their economic feasibility. To summarize, we have formulated a cost-driven approach that can guide the industry to continue semiconductor scaling.

T15-4 - 11:45
Device-, Circuit- & Block-Level Evaluation of CFET in a 4 Track Library, P. Schuddinck*, O. Zografos*, P. Weckx*, P. Matagne*, S. Sarkar*, Y. Sherazi*, R. Baert*, D. Jang*, D. Yakimets*, A. Gupta*, B. Parvais*.**, J. Ryckaert*, D. Verkest* and A. Mocuta*, *imec and **Vrije Universiteit Brussel, Belgium

The structure of the complementary FET (CFET) with NMOS stacked on top of PMOS, inherently yields standard cells and SRAM cells with 25% smaller layout area, 25% higher pin density and 2x higher routing flexibility than FinFET with same overall active footprint. Moreover, our work, based on advanced modelling, demonstrates that 4 track CFET can match and even outperform 5 track FinFET, without the need to lower S/D contact resistivity down to 5e-10Ω.cm^2 or to elevate the channel stress up to 2 GPa. All gains in power-performance-area at circuit-level are maintained at block-level, making 4 track CFET a suitable candidate for N3 & N2 technologies.

T15-5 - 12:10
2nm Node: Benchmarking FinFET Vs Nano-Slab Transistor Architectures for Artificial Intelligence and Next Gen Smart Mobile Devices, S. C. Song*, C. Chidambaram*, B. Colombeau**, M. Bauer**, S. Natarajan**, V. Moroz***, X.-W. Lin***, D. Sherlekar***, M. Choi***, J. Huang***, P. Asenov**** and B. Cheng****, *Qualcomm Technologies, Inc., **Applied Materials, Inc., ***Synopsys, Inc., USA and ****Synopsys, Inc., UK

We explore four different technology and design options for transistors and library cells for a low power supply voltage of 0.4 V and circuit statistics representative of artificial intelligence (AI) applications. The design rules correspond to 2nm node with cell heights of 100~110 nm and 30 nm gate pitch. Holistic analysis of the RO (Ring Oscillator) behavior, including MOL parasitics, all major variability sources, and stress proximity effects suggests that different FinFET and nanoslab transistor design options exhibit a wide range of power and performance differences. The key to improve FinFET PPA is to avoid fin cuts to maintain strong PMOS performance, and a key to improve SS corner delay is to use nanoslabs with tighter variability control.

Luncheon Talk [Suzaku I]

Thursday, June 13, 12:35-14:00

Developing Visual Systems for Entertainment and Art, Y. Hanai, Rhizomatiks, Japan

Rhizomatiks Research is our division dedicated to exploring new possibilities in the realms of technical and artistic expression. Focusing on media art, data art, and other RD-intensive projects, our team strives to deliver cutting edge solutions that have not yet been seen on a global stage. Rhizomatiks Research is accountable for all steps of a project, from hardware/software development up through operation. Additionally, we study the relationship between people and technology, and collaborate on projects with a myriad of creators. In this presentation, we'll introduce our past projects which mainly utilized vision technologies such as AR/VR.

SESSION 16

3D NAND [Shnju II, III]

Thursday, June 13, 14:00-15:40

Chairpersons: K. Hamada, Micron Memory Japan, Inc.
G. Hemink, Western Digital Corp.

T16-1 - 14:00
Advantage of Extremely-Thin Body (Tsi~3nm) Device to Boost The Memory Window for 3D NAND Flash, H.-T. Lue, C. C. Hsieh, T. H.Hsu, W. C. Chen, C. P. Chen, C. Chiu, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

The advantage of using extremely-thin body (ETB, Tsi=3nm) device has been demonstrated in a 3D NAND Flash test chip. Net P/E memory window gain of >1.3V is observed for devices using ETB poly-Si. This substantial gain can be explained by the quantum confinement that raises effective Si bandgap and in turn reduces the tunneling barrier height. Simulation model has been validated and it shows equivalent barrier height reduction of ~0.16eV and 0.07eV for electron and hole, respectively for Tsi=3nm. However, the Idsat is degraded to only 160nA for Tsi=3nm, which is attributed to the larger effective mass or higher contact resistance. The degraded Idsat can be accommodated by lower Isense<30nA for page buffer circuit tuning. Random telegraph noise (RTN) is significantly reduced by extremely-thin body, and it shows tighter program-verify (PV) distribution in the MLC/TLC operation.

T16-2 - 14:25
A Novel Confined Nitride-Trapping Layer Device for 3D NAND Flash with Robust Retention Performances, C.-H. Fu, H.-T. Lue, T.-H. Hsu, W.-C. Chen, G.-R. Lee, C.-J. Chiu, K.-C. Wang and C.-Y. Lu, Macronix International Co., Ltd., Taiwan

For the first time, we have fabricated a confined nitride (SiN) trapping layer device for 3D NAND Flash and demonstrated excellent post-cycling retention performances. The key process step is to develop a uniform sidewall lateral recess in the 3D stack, followed by a SiN pull back process to isolate the SiN trapping layer in a self-aligned way. Excellent retention with only ~600mV shift of charge loss (out of initial 7V window) after 125C 1-week high-temp baking for a post 1K cycled device was obtained. It is far superior to the control sample without confined SiN structure. Arrhenius analysis at various baking temperatures shows that the retention may pass >100 years at 60C, and is even longer at room temperature. The device has potential to meet the low-cost long-retention archive memory applications.

T16-3 - 14:50
Modeling of Charge Loss Mechanisms During The Short Term Retention Operation in 3-D NAND Flash Memories, C. Woo*, M. Lee**, S. Kim*, J. Park*, G.-B. Choi**, M.-S. Seo**, K. H. Noh**, M. Kang*** and H. Shin*, *Seoul National Univ., **SK hynix Inc. and ***Korea National Univ. of Transportation, Korea

Right after program, stored electrons in the shallow nitride trap level can be released less than a few seconds. By setting the delay between program and reading phase to as small as 10μs, we found that several mechanisms are mixed when stored electrons are emitted during short term retention of 3-D NAND Flash. For the first time, we have confirmed that the charge loss mechanisms consist of three mechanisms and have separated each mechanism. In particular, the vertical redistribution of electrons in the charge trap layer, observed only during short term, was analyzed for the first time. Short term retention data measured at various temperatures (25-115) and at several program verify levels (PV3, PV5, PV7) in solid (S/P) and checker-board patterns (C/P) were analyzed using our model. Finally, the activation energy (E_a) of each mechanism was extracted by the Arrhenius law and the magnitudes of E_a were compared.

T16-4 - 15:15
Pre-Shipment Data-Retention/Read-Disturb Lifetime Prediction & Aftermarket Cell Error Detection & Correction by Neural Network for 3D-TLC NAND Flash Memory, M. Abe, T. Nakamura and K. Takeuchi, Chuo Univ., Japan

This paper proposes 2 neural network techniques for 3D-TLC NAND flash memory. The first proposal is to predict data-retention/read-disturb lifetime for chip sorting during pre-shipment test. The second proposal is to detect and correct errors in aftermarket. First, in pre-shipment test, Neural Network-based Lifetime Prediction (NNLP) predicts future ECC decoding fail rate and estimates data-retention/read-disturb lifetime at higher endurance by using low endurance data. Then, NNLP sorts NAND flash memories into read-cold or read-hot applications. Chips with long data-retention lifetime are shipped to read-cold applications such as archives and cold flash storage. Chips immune to read-disturb are shipped to read-hot applications such as entertainment devices and cache of hierarchical storage. Second, in aftermarket, Neural Network-based Error Detection (NNED) detects and corrects errors. When ECC cannot correct errors, NNED detects and corrects part of errors and then BCH ECC completely corrects remaining errors. NNED decreases bit-error rate by 81.4%.

SESSION 17

Ferroelectric II [Shunju I]

Thursday, June 13, 14:00-15:40

Chairpersons: S. Takagi, The Univ. of Tokyo
K. Benaissa, Texas Instruments

T17-1 - 14:00
Transient Negative Capacitance as Cause of Reverse Drain-Induced Barrier Lowering and Negative Differential Resistance in Ferroelectric FETs, C. Jin, T. Saraya, T. Hiramoto and M. Kobayashi, The Univ. of Tokyo, Japan

We have investigated transient I_d-V_g and I_d-V_d characteristics of ferroelectric FET (FeFET) by simulation with ferroelectric (FE) model considering polarization switching dynamics. For the first time, we show transient negative capacitance (TNC) with polarization reversal and depolarization effect results in sub-60 *SS*, reverse drain-induced barrier lowing (R-DIBL), and negative differential resistance (NDR) without traversing the quasi-static negative capacitance (QSNC) region in S-shaped *P-V* based on Landau theory. The mechanism demonstrated in this work can be a possible explanation for the previously reported negative capacitance FET (NCFET) with steep *SS*, R-DIBL, and NDR.

T17-2 - 14:25
A Comprehensive Kinetical Modeling of Polymorphic Phase Distribution of Ferroelectric-Dielectrics and Interfacial Energy Effects on Negative Capacitance FETs, Y.-T. E. Tang*, C.-L. Fan**, Y.-C. Kao**, N. Modolo**, C.-J. Su*, T.-L. Wu**, K.-H. Kao***, P.-J. Wu****, S.-W. Hsaio****, A. Useinov**, P. Su**, W.-F. Wu*, G.-W. Huang*, J.-M. Shieh*, W.-K. Yeh* and Y.-H. Wang***, *Taiwan Semiconductor Research Institute, **National Chiao Tung Univ., ***National Cheng Kung Univ. and ****National Synchrotron Radiation Research Center, Taiwan

This paper clarifies for the first time the origin of ferroelectricity in the Negative Capacitance Field-Effect Transistors (NCFETs) by molecular dynamics (MD) simulation. MD simulation considering atomic interactions between all atoms enables accurate predictions for the microstructure even at all interfaces. By incorporating the results from MD simulations into a kinetic model, it is able to predict the conditions of crystallization and phase transition during RTP and cooling processes that govern ferroelectricity in FETs. Our simulation reveals that the lower discrepancy between orthorhombic (o-) phase and tetragonal (t-) phase of interfacial energies, together with in-plane tensile stress, will improve t-o transaction efficiency in the cooling down process, leading more ferroelectricity in NCFETs. Finally, design methodology to maintain the electric variation of NCFETs is also proposed

T17-3 - 14:50
Negative Capacitance CMOS Field-Effect Transistors with Non-Hysteretic Steep Sub-60mV/Dec Swing and Defect-Passivated Multidomain Switching, C. Liu*, H.-H. Chen*, C.-C. Hsu*, C. C. Fan*, H.-H. Hsu** and C.-H. Cheng***, *National Chiao Tung Univ., **National Taipei Univ. of Technology and ***National Taiwan Normal Univ., Taiwan

We demonstrated that the 2.5nm-thick $HfAlO_x$ N-type NCFET based on defect-passivated multidomain switching can achieve a minimum 9 mV/dec subthreshold swing (*SS*), a negligible hysteresis of 1mV, an ultralow I_{off} of 135 fA/μm, a large I_{on}/I_{off} ratio of 8.7×10^7 and a sub-60 mV/dec SS over 5 decade. For P-type NCFET, the non-hysteretic steep-slope switch is still reached under the synergistic effect of gate stress, defect passivation and doping engineering. The Al doping and defect passivation play the key role for reducing trap-related leakage, enhancing NC, and stabilizing multidomain switching. The highly scaled $HfAlO_x$ CMOS NCFET shows the potential for low power logic applications.

T17-4 - 15:15
Microscopic Crystal Phase Inspired Modeling of Zr Concentration Effects in $Hf_{1-x}Zr_xO_2$ Thin Films, A. K. Saha*, B. Grisafe**, S. Datta** and S. Gupta*, *Purdue Univ. and **Univ. of Notre Dame, USA

In this paper, we theoretically and experimentally investigate the Zr concentration dependent crystal phase transition of $Hf_{1-x}Z_xO_2$ (HZO) and the corresponding evolution of dielectric (DE), ferroelectric (FE) and anti-ferroelectric (AFE) characteristics. Providing the microscopic insights of strain induced crystal phase transformations, we propose a physics based model that shows good agreement with our experimental results for 10nm $Hf_{1-x}Z_xO_2$ (with x=0 through 1). Utilizing our model, we analyze HZO-FET operation as a nonvolatile memory device for different x.

SESSION 18

ReRAM & Selector [Shunju II, III]

Thursday, June 13, 16:00-18:05

Chairpersons: S.-W. Chung, SK Hynix Semiconductor Ltd.
F. Arnaud, ST Microelectronics

T18-1 - 16:00
Non-Volatile RRAM Embedded into 22FFL FinFET Technology, O. Golonzka, U. Arslan, P. Bai, M. Bohr, O. Baykan, Y. Chang, A. Chaudhari, A. Chen, J. Clarke, C. Connor, N. Das, C. English, T. Ghani, F. Hamzaoglu, P. Hentges, P. Jain, C. Jezewski, I. Karpov, H. Kothari, R. Kotlyar, B. Lin, M. Metz, J. ODonnell, D. Ouellette, J. Park, A. Pirkle, P. Quintero, D. Seghete, M. Sekhar, A. Sen Gupta, M. Seth, N. Strutt, C. Wiegand, H. J. Yoo and K. Fischer, Intel Corp., USA

This paper presents key specifications of RRAM-based non-volatile memory embedded into Intel 22FFL FinFET Technology. 22FFL is a high performance, ultra low power technology developed for mobile and RF applications providing extensive high voltage and analog support and high design flexibility combined with low manufacturing costs. Embedded RRAM technology presented in this paper achieves 10^4 cycle endurance combined with 85°C 10-year retention and high die yield. Technology data retention, endurance and yield are demonstrated on 7.2Mbit arrays. We describe device characteristics, bit cell integration into the logic flow, as well as key considerations for achieving high endurance and retention properties.

T18-2 - 16:25
A 40nm 2Mb ReRAM Macro with 85% Reduction in FORMING Time and 99% Reduction in Page-Write Time Using Auto-FORMING and Auto-Write Schemes, Y.-C. Chiu*, H.-W. Hu*, L.-Y. Lai*, T.-Y. Huang*, H.-Y. Kao*, K.-T. Chang*, M.-S. Ho**, C.-C. Chou***, Y.-D. Chih***, T.-Y. Chang*** and M.-F. Chang*, *National Tsing Hua Univ., **National Chung Hsing Univ. and ***TSMC, Taiwan

This work proposes (1) an auto-forming (AF) scheme to shorten the macro forming time (T_{FM-M}) and testing costs; (2) an auto-RESET (ARST) scheme to shorten page-RESET time ($T_{W-PAGE-RST}$) for expanding the applications of hidden-RESET operation in standby mode, and (3) an auto-SET (ASET) scheme to shorten page-write time (T_{W-PAGE}) combined with hidden-RESET scheme. A fabricated 40nm 2Mb ReRAM macro achieved 85+% reduction in T_{FM-M}, and 99+% reduction in T_{W-PAGE} for a page. For the first time, AF, ARST, and ASET schemes are demonstrated in silicon for ReRAM.

T18-3 - 16:50
Application-Induced Cell Reliability Variability-Aware Approximate Computing in TaO_x-Based ReRAM Data Center Storage for Machine Learning, C. Matsui, S. Fukuyama, A. Hayakawa and K. Takeuchi, Chuo Univ., Japan

This paper proposes Variability-Aware Approximate Computing (V-AC) for TaO_x ReRAM storage at data centers with 6 design strategies. For the first time, this paper shows that application-induced variability degrades the performance. To solve this problem, V-AC fully utilizes error resilience of machine learning (ML) applications and decreases bit-error rate of typical cells by removing extra data copy and enlarging BER difference among memory cells. By combining device measurement and system emulations, this paper realizes system, circuit and device co-design (SCDCD). Proposed SCDCD platforms combines device measurement and transaction-level-modeling system emulator. V-AC is the key enabling technology to push the limits of performance, power, chip size and scaling of ReRAM for ML. Performance, energy and cell area of ReRAM storage improves by 7.0 times, 90% and 8.5%, respectively. Moreover, lower 20% Set/Reset voltage reduces driving current specification of selector devices and will extends the scaling of future ReRAM.

T18-4 - 17:15
$Nb_{1-x}O_2$ Based Universal Selector with Ultra-High Endurance (>10^{12}), High Speed (10ns) and Excellent V_{th} Stability, Q. Luo*, J. Yu*, X. Zhang*, K.-H. Xue**, J.-H. Yuan**, Y. Cheng***, T. Gong*, H. Lv*, X. Xu*, P. Yuan*, J. Yin*, J. Li****, S. Long*, X. Miao**, L. Tai*, Q. Liu* and M. Liu*, *Institute of Microelectronics of the Chinese Academy of Sciences, **Huazhong Univ. of Science and Technology, ***East China Normal Univ., China and ****Univ. of Wisconsin-Madison, USA

In this work, we demonstrate a high performance $Nb_{1-x}O_2$ based selector with thermal feedback mechanism for 3D X-point application. Ultra-high endurance (>10^{12}), high operation speed (10ns), bidirectional operation and excellent V_{th} stability were achieved. By adding a barrier layer between $Nb_{1-x}O_2$ film and electrode, the off-state leakage current was reduced by one order of magnitude (selectivity as high as 500). This work provides a universal selector solution for various emerging memories, including RRAM, MRAM and PCM.

T18-5 - 17:40
Evidence of Filamentary Switching and Relaxation Mechanisms in Ge_xSe_{1-x} OTS Selectors, Z. Chai*, W. Zhang*, R. Degraeve**, S. Clima**, F. Hatem*, J. F. Zhang*, P. Freitas*, J. Marsland*, A. Fantini**, D. Garbin**, L. Goux** and G. Kar**, *Liverpool John Moores Univ., UK and **imec, Belgium

Comprehensive experimental and simulation evidence of the filamentary-type switching and V_{th} relaxation mechanism associated with defect charging/discharging in Ge_xSe_{1-x} ovonic threshold switching (OTS) selector is reported. For the first time, area independence of conduction current at both on/off states, Weibull distribution of time-to-switch-on/off (t-on/off), Vth relaxation and its dependence on time, bias and temperature, which is in good agreement with our first-principles simulations in density functional theory, provide strong support for filament modulation by defect delocalzation/localization that is responsible for volatile switching.

SESSION 19

III-V & 2D [Shunju I]

Thursday, June 13, 16:00-17:40

Chairpersons: Y. Shiratori, NTT Corp.
P. Grudowski, NXP

T19-1 - 16:00
GaN HEMTs with Breakdown Voltage of 2200 V Realized on a 200 mm GaN-on-Insulator(GNOI)-on-Si Wafer, Z. LIU*, H. Xie*, K. H. Lee*, C. S. Tan**, G. I. Ng** and E. A. Fitzgerald***, *Singapore-MIT Alliance for Research and Technology (SMART), **Nanyang Technological Univ., Singapore and ***Massachusetts Institute of Technology, USA

GaN-on-Si has revealed its great potential for next-generation power electronics applications, however, there remains a challenge in increasing the breakdown voltage (BV_{off}) due to the limit of the GaN epilayer thickness on large size wafers. In this work we propose a GaN-on-Insulator (GNOI)-on-Si structure to address this issue. A 200 mm GNOI-on-Si wafer was prepared through removing the original Si substrate of a GaN-on-Si wafer and bonding onto a fresh SiO_2/Si substrate. HEMTs were fabricated with measured BV_{off} much larger than those on GaN-on-Si. Record high BV_{off} up to 2200 V and high figure-of-merit (FOM) $BV_{off}^2/R_{on,sp}$ up to 1.87 GW/cm2 have been achieved in the HEMTs on a 200 mm GNOI-on-Si wafer with a thin GaN epilayer of 3.2 μm.

T19-2 - 16:25
First Demonstration of 40-nm Channel Length Top-Gate WS_2 pFET Using Channel Area-Selective CVD Growth Directly on SiO_x/Si Substrate, C. C. Cheng*, Y.-Y. Chung***, M.-Y. Li*, C.-T. Lin***, C.-F. Li***, J.-H. Chen**, T.-Y. Lai**, K.-S. Li**, J.-M. Shieh**, S.-K. Su*, H.-L. Chiang*, T.-C. Chen*, L.-J. Li*, H.-S. Wong* and C.-H. Chien***, *Taiwan Semiconductor Manufacturing Company, Corporation Research, **Taiwan Semiconductor Research Institute, National Applied Research Laboratories and ***Institute of Electronics, National Chiao Tung Univ., Taiwan

Area-selective channel material growth for 2D transistors is more desirable for volume manufacturing than exfoliation or wet/dry transfer after large area growth. We demonstrate the first top-gate WS_2 p-channel field-effect transistors (p-FETs) fabricated on SiO_x/Si substrate using channel area-selective CVD growth. Smooth and uniform WS_2 comprising approximately 6 layers was formed by area-selective CVD growth in which a patterned tungsten-source/drain served as the seed for WS_2 growth. For a 40 nm gate length transistor, the device has impressive electrical characteristics: on/off ratio of ~10^6, a S.S. of ~97 mV/dec., and nearly zero DIBL

T19-3 - 16:50
Reassessing Ingaas for Logic: Mobility Extraction in Sub-10nm Fin-Width FinFETs, X. Cai*, A. Vardi*, J. Grajal** and J. del Alamo*, *Massachusetts Institute of Technology, USA and **Universidad Politecnica de Madrid, Spain

We study the performance degradation of InGaAs FinFETs as they scale to sub-10 nm fin width. This is often attributed to degradation in intrinsic transport parameters. High frequency measurements, however, indicate increasingly severe oxide trapping as the fin width narrows. This is confirmed by pulsed-IV measurements. A new mobility extraction method using concurrent S-parameter and DC-IV measurements avoids the impact of oxide trapping and reveals promising mobility in thin-channel InGaAs planar MOSFETs and narrow-width FinFETs. Our study suggests that performance degradation of InGaAs FinFETs is largely an extrinsic phenomenon that can be engineered around and that the potential performance of deeply-scaled InGaAs FinFETs is significantly underestimated.

T19-4 - 17:15
Monolithic Integration of GaAs//InGaAs Photodetectors for Multicolor Detection, D.-M. Geum*, S. H. Kim***, S. K. Kim**, S. S. Kang****, J. H. Kyhm****, J. D.Song**, W. J. Choi** and E. Yoon*, *Seoul National Univ., **Korea Institute of Science and Technology (KIST), ***KAIST and ****Dongguk Univ., Korea

Multicolor photodetectors (PDs) by using bulk p-i-n based visible GaAs and near-infrared (IR) InGaAs PD was successfully fabricated via monolithic integration by wafer bonding and epitaxial lift-off. It showed high-performance individual operation comparable to that of bulk PDs with tight vertical alignment on a single substrate for future high-resolution multicolor PDs. At the same time, it covered a broad wavelength range from visible to IR.

Friday Forum

Enabling Technologies for Autonomous Driving [Suzaku I, II, III]

Friday , June 14, 9:00-15:35

Organizers: T. Tanaka, Tohoku Univ.
K. Benaissa, Texas Instruments Inc.
Y. Oike, Sony Corp.
R. Kapusta, Analog Devices, Inc.

Moderator: K. Nakamura, Analog Devices, Inc.

9:00 Opening

9:10 Inertial and Depth Sensors for Autonomous Vehicles, R. Kapusta, Analog Devices, Inc.

The pathway to achieving full autonomy begins with a cross-functional, system-level approach that surrounds the vehicle with a real-time, 360-degree safety shield. This shield is created by fusing data from high-performance inertial sensors, RADAR, and LIDAR with other sensor outputs, which ultimately gives the vehicle its ability to accurately perceive the road around it. While RADAR and LiDAR remain a premium feature in autonomous vehicles currently, they must become a standard fitment to address safety concerns.
In this talk, we will look at the sensor framework for the fully autonomous vehicle. The need for significantly improved performance and response time will be explored, along with opportunities to exploit the complementary nature of various sensors through fusion of their outputs.

9:55 Safety and Security at the Heart of Autonomous Driving, K. Khouri, NXP Semiconductors

Automotive safety and security are not only pivotal to market acceptance of autonomous vehicles, but a required rite of passage for any automotive supplier. At NXP, safety and security are part of our DNA: we have deep knowhow on these subjects and our safety & security culture is deeply embedded within the company. This means that at every stage of the design and development process, we are implementing industry best practices, complemented by NXP's unique experience and knowhow in safety & security to deliver state-of-the-art security and safety solutions. Making it easier for our customers to comply with industry-wide requirements and standards for safety and security by delivering documentation, tools and support.

10:40 Break

11:00 Electronics Technologies Evolve Automobiles!?, N. Kawahara, DENSO Corp.

Automotive electronics have been evolving and creating new control systems to realize safer and more eco-friendly vehicles. Many automotive functions are changing from mechanical to electronic control. By changing the control systems, the number of electronic parts such as sensors, electronic circuits, and actuators has been drastically increasing. And this trend will continue in the future to evolve automobiles. MEMS technologies, along with the packaging, electronic circuit, and software technologies, will become more important in the future vehicle equipped with many advanced sensors. Undoubtedly, the control system becomes more advanced with each improvement in the sensing speed or sensor accuracy.
In the presentation, the future trend of automobiles and Electronics will be discussed.

11:45 Automotive Image Sensor for Autonomous Vehicle and Adaptive Driver Assistance System,
H. Matsumoto, Sony Semiconductor Solutions Corp.

Human vision is the most essential sensor to drive vehicle. Instead of human eyes, CMOS image sensor is the best sensing device to recognize objects and environment around the vehicle. Image sensors are also used in various use cases such as driver and passenger monitor in cabin of vehicle. For these use cases, some special functionalities and specification are needed. In this session the requirements for automotive image sensor will be discussed such as high dynamic range, flicker mitigation and low noise. In the last part the key technology to utilize image sensor, such as image recognition and computer vision will be discussed.

12:30 Lunch

13:30 The Advent of the GPU in AI/Supercomputing and its Application to Autonomous Driving, T. Baji, NVIDIA Corp.

In the old good days, CPU performance increased almost 1.5 times / year thanks to the Moor's Law. However by the year 2010, due to the leakage current and too complex CPU architecture, this rate becomes 1.1 times / year. On the other hand, parallel processing dedicated GPU continues to grow its performance with the rate of 1.5 times / year, and even with the Moor's Law ending, it still continues to grow its performance by built-in accelerators. Now GPU is the most widely used accelerator in AI and Supercomputing. This GPU architecture is also applied to the most advanced autonomous driving SoC Xavier.
In this talk, GPU technologies which realize this high performance, the autonomous driving platform based on this GPU and Xavier SoC, and the end-to end system solution that enables its functional safety and reliability will be introduced.

14:15 Envisioning Smart Mobility Society in the Connected Future, T. Imai, Toyota Motor Corp.

The automotive industry is changing faster today than it has in 100 years and must reconsider what our society and customers expect from us – as automotive companies. It is not only a shift from a car manufacturing & sales company to a mobility company but also a convergence of electrification, connectivity and artificial intelligence. With these exciting advances, it is our mission to provide new mobility society.
The main objectives of this session are: (1) the current state of vehicle connectivity, showing connected vehicles in Japan and how to utilize big data, and (2) our vision of the smart mobility society of the future, which is the key to realize seamless and comfortable transportation through connected vehicles with the Vehicle Control Interface and the Mobility Service Platform (MSPF).

15:05 Panel Discussion

15:35 Closing

Friday Evening Event [Taizo-in]

Friday, June 14, 16:15-19:35