2019 SYMPOSIA ON VLSI TECHNOLOGY & CIRCUITS

Semiconductor industry's premier event on advances in microelectronics technology & circuits

RIHGA Royal Hotel
KYOTO
June 9-14, 2019


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2019 VLSI SYMPOSIA THEME

Pushing the Limits of Semiconductors for United and Connected World

The 2019 Symposia on VLSI Technology and Circuits feature a fully overlapped program to highlight recent semiconductor advances for a united and connected world. The Symposia start on Sunday, June 9th with three Sunday workshops, followed by short courses, demo and focus sessions, panel discussions, and a Friday forum, in addition to many exciting contributed papers.

SYMPOSIUM ON VLSI TECHNOLOGY

June 11

Managing Moore's Inflection: DARPA's Electronics Resurgence Initiative
-William Chappell, Office Director, MTO, DARPA

June 12

Si Platform for Developing Spin-based Quantum Computing
-Seigo Tarucha, Professor, The Univ. of Tokyo / RIKEN Center for Emergent Matter Science

PLENARY PRESENTATIONS

Tuesday and Wednesday morning, June 11 and 12

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June 11

Augmented Human (TBD)
-Masahiko Inami, Professor, The Univ. of Tokyo

June 12

TBD

EVENING PANEL DISCUSSION

Tuesday evening, June 11

What will the foundries of the future do?
Moderator: TBD
Panelists: Top technology and business experts from foundries and fabless companies, as well as from academia.

Conventional process node scaling has been extremely successful for many decades, but the challenges below 5 nm may require us to question our assumptions about the fabs of the future if we want the semiconductor industry to thrive in the next decade:
In this panel, we will discuss technology challenges and opportunities as well as new deliverable values to market, in order to provide perspective on the fabs of the future.

TECHNOLOGY FOCUS SESSIONS

Tuesday, June 11

- Quantum Computing
- 3D Integration and Packaging

JOINT PROGRAM HIGHLIGHTS

JOINT EVENING PANEL DISCUSSION

Monday evening, June 10

The economics (and future) of our industry, new business model, what can fab provide?

- Moderator: Kofi Makinwa, TU Delft
- Affiliations of expected panelists: Experts from economics, venture capital, education, journalism

We are approaching the end of Moore's Law. What happens when technology scaling stops? This conference is a key forum for the technical issues, but beyond those questions, there are questions of economics and business models. This panel will bring experts in these areas to discuss.

JOINT FOCUS SESSIONS

Wednesday, June 12 & Thursday, June 13

Joint Circuits and Technology Focus Sessions will be offered in the following special topics of joint interest:

- Technology & System for AI
- The Future of Memory
- Design and Technology for Scaling Extension

DEMO SESSION

Monday evening, June 10

Unique opportunity to learn more about some of the most impactful new devices and circuits through:

- System-level demos that showcasing key applications for circuit-level innovations
- Table-top real-time demonstration of record device performance
- Visual illustration of technological concepts and analyses
- Opportunity for in-depth discussion with authors of demo papers

LUNCHEON

Thursday, June 13

Developing Visual Systems for Entertainment and Art, Yuya Hanai, Rhizomatiks

JOINT RECEPTION

Monday, June 10

JOINT BANQUET

Wednesday, June 12

EVENING PANEL DISCUSSION

Tuesday evening, June 11

Technology We Will See Coming Out of the Tokyo Olympics and Beyond
Moderator: Koichi Hamashita, AKM
Panelists: Jonathan Jensen/Intel, Michael Pate/Google, Yukihiro Kato/Denso, Masayuki Mizuno/NEC, Yasunori Kimura/Fujitsu, Pat O'Connor/Microsoft

The world will see many new and exciting technologies at the upcoming Olympic Games. The panel will give us a look behind these technologies and the innovative circuits that make them possible. (Note that this panel is not affiliated with the Tokyo Olympics)

SHORT COURSE 1

CMOS Technology Enablers for Pushing the Limits of Semiconductors: Materials to Packaging

Monday, June 10

This short course highlights the key technologies that will push semiconductor performance forward through materials, advanced devices, design, materials and packaging.

1. Breaking the Limitations of FinFET Scaling, Mark Liu, Intel
2. Emerging Interconnect Technologies for Nanoelectronics, Krishna Saraswat, Stanford
3. Advanced Process Technologies Required for Future Scaling and Devices, Robert Clark, TEL
4. DTCO in 2019: The Precious Metal Stack and the Route to Better Designs, Brian Cline, ARM
5. 3D Integration for More Moore and More than Moore, Chih-Hang Tung, TSMC
6. Recent STT-MRAM Technology: From Lab to Fab, Yoonjong Song, Samsung
7. Emerging FETs, Sayeef Salahuddin, UCB
8. 3D NAND Flash, Ryota Katsumata, Toshiba Memory

SHORT COURSE 2

Advanced 5G Circuits, Systems and Applications

Monday, June 10

The course demystifies recent advances in 5G wireless circuit technologies covering transceivers, PLL, Filter, MIMO beam forming, as well as system architectures and applications.

1. 5G Real and Future, Takehiro Nakamura, NTT Docomo
2. CMOS mmWave RFIC Transceiver for 5G Base Station Applications, Sung-Gi Yang, Samsung
3. 5G ICs for Handset, Hyung-Jin Lee, Intel
4. Low Phase Noise Clock Source for 5G, Jae-Hyouk Choi, UNIST
5. Acoustic Filter for 5G Smartphones, Hiroyuki Nakamura, Skyworks
6. Integration Technology for mm-wave Module, Kaoru Sudo, Murata
7. MIMO Beam Forming Circuit and Algorithm of 5G, Hua Wang, Georgia Tech. Univ.
8. Analog-beam Forming TRx Ics in Massive Production, Built-in-test, Brian Floyd, NCSU

SHORT COURSE 3

Opportunities and Challenges at the Intersection of Security and AI.

Monday, June 10

As AI enjoys rapid progress in recent years, its security implications are also attracting increased attention. This short course surveys the technology, architecture, and circuit foundations behind AI and security, and provides an outlook on their interactions.

1. Introduction to Artificial Intelligence & Security, Rob Aitken, ARM
2. Hardware Requirements and Challenges for AI, Hoi-Jun Yoo, KAIST
3. AI Computing Architecture and Hardware, Jeff Burns, IBM
4. Nonvolatile Circuit for AI, Meng-Fan Chang, National Tsing-Hua University
5. RRAM Fabric for Neuromorphic Computing Applications, Wei Lu, Univ. of Michigan
6. Hardware Security -- Attack and Countermeasure --, Naofumi Homma, Tohoku University
7. Crypto Accelerator, TRNG, Sanu Mathew, Intel
8. EMI Information Security, Yuichi Hayashi, Nara Institute of Science and Technology

SATELLITE WORKSHOPS

Silicon Nanoelectronics Workshop
Sunday, June 9 & Monday, June 10

Spintronics Workshop on LSI
Sunday, June 9

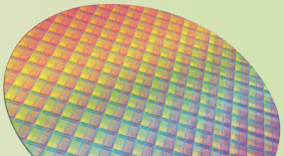
SUNDAY WORKSHOPS NEW!!

Sunday evening, June 9

WS1: Impact of Atomic Layer Processing and Selective Area Patterning on Device Fabrication and Performance
WS2: Two Dimensional Materials and Applications
WS3: Low thermal budget dopant activation for sequential-3D integration

FRIDAY FORUM

Enabling Technologies for Autonomous Driving
Friday, June 14



For complete conference and registration information, visit: **http://www.vlsisymposium.org/**

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